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Current Concerns Regarding Solid State Drive Reliability

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DfR Solutions, LLC

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Outline

- Critical Issues in Solid State Drive Reliability
  - Single (SEU) and multi (MEU) event upsets
    - Neutron and alpha particle-induced failures
  - Other forms of IC degradation
    - Failure: dielectric breakdown (TDDB), electro-migration (EM)
    - Drift: negative bias temperature inversion (NBTI), hot carrier injection (HCI)
  - Advanced packaging issues
    - Off-die interconnect reliability

- Emphasis on:
  - Failure mechanisms
  - Scaling effects to deep sub-micron feature sizes

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Solid State Memory: Technology Roadmap

	Embedded DRAM	SRAM	NOR Flash	NAND Flash
Cell	1T1C	6T	1T	1T
Feature size, F (nm)	90 25	65 13	90 18	90 18
Cell area (F^2)	12 12	140 140	10 10	5 5
Read time (ns)	1 0.2	0.3 0.07	10 2	50 10
Write/erase time	0.7 ns 0.2 ns	0.3 ns 0.07 ns	1 us/10 ms 1 us/10 ms	1/0.1 ms 1/0.1 ms
Retention time	64 ms 64 ms	V duration V duration	> 10 yrs > 10 yrs	> 10 yrs > 10 yrs
Write cycles	> 3e16 > 3e16	> 3e16 > 3e16	> 1e5 > 1e5	> 1e5 > 1e5

Timeline
BLUE: 2007
RED: 2022

Emerging technologies: trapping charge, FeRAM, MRAM, PCM

ITRS: *Emerging Research Devices*, 2007

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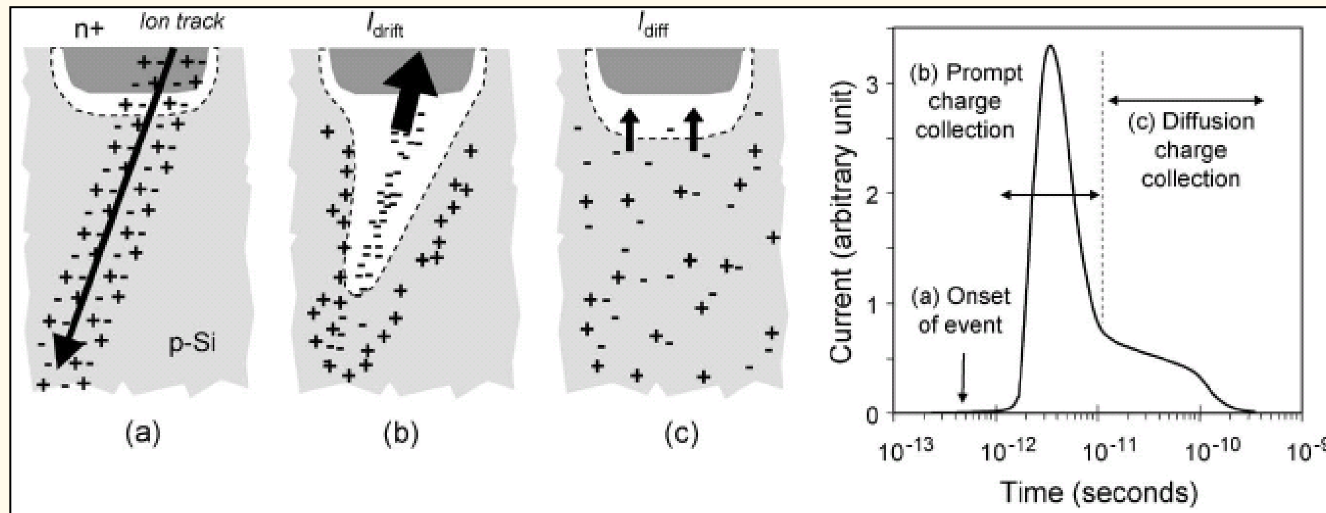
Single & Multi-Event Upsets

- Single event
  - Ionization impacts a single cell/register/latch/flip-flop, causing change of state
  - Typical for low energy strikes; more common than multi-event
- Multi-event
  - Ionization impact (cascades) affecting multiple cell states
  - Typical for high energy strikes, increasingly common as cell sizes shrink
- "Soft" errors: removed during rewrite of bit, *unless critical cells hit*



R.C. Baumann (TI), *IEEE Trans on Dev & Matl Rel*, 5(3), 2005

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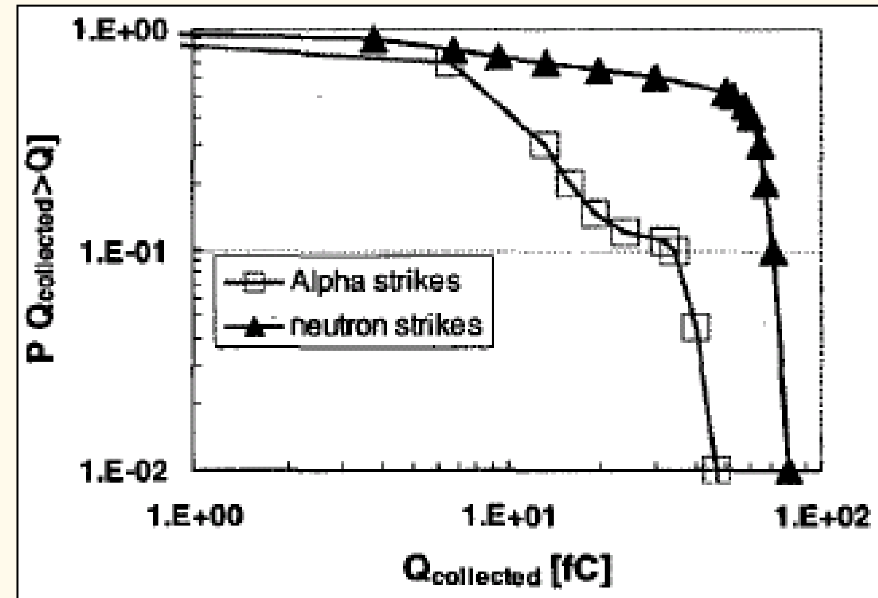
Single & Multi-Event Upsets: Mechanisms

- **α particles**
  - Due to ^{238}U, ^{235}U & ^{232}Th in packaging materials
  - Interact with e^- to form ionization wake
  - Reduced by improvements in material purity
- **^{10}B**
  - Present in boron-doped glass (BPSG) dielectric layers
  - React with neutrons to form α + ^{7}Li
  - BPSG progressively phased out
- **Neutrons**
  - High & low energy cosmic rays
  - Ionization by inelastic collisions
  - *Largest contributor to SEU/MEU*



For small volumes/low critical charge levels, SE/ME rate dictated by strike rate

S. Hareland *et al.* (Intel), *Symp on VLSI Tech*, 2001

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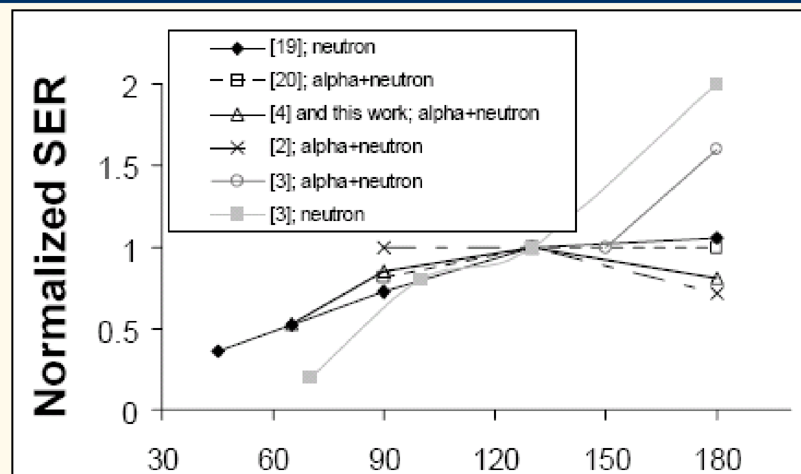
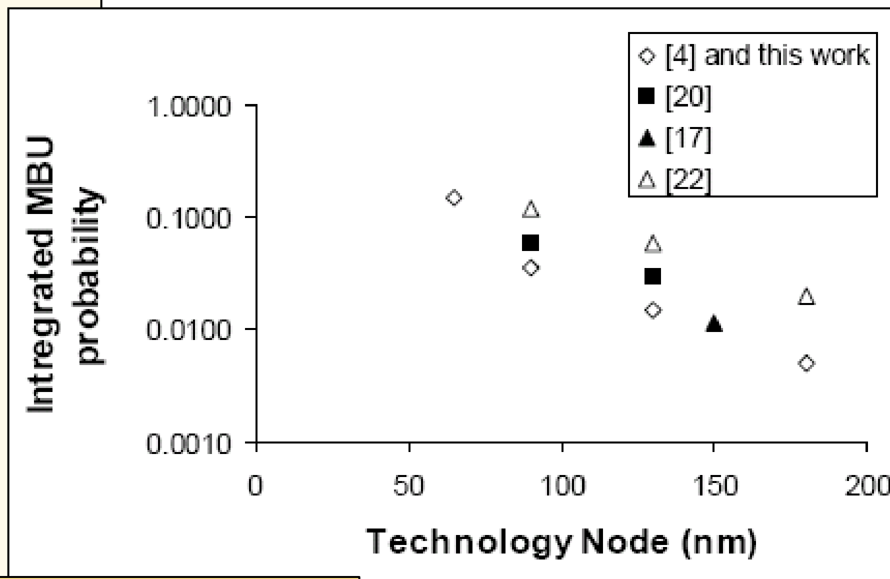
Scaling Effects: SEU vs. MEU

- Single event upset
  - Mitigation schemes have improved SEU rate (SER) with each cycle
- Multi-event upset
  - Rapidly increasing node density → logarithmically increasing multi-event rate





N. Seifert *et al.* (Intel, Stanford, Vanderbilt), *IEEE 44th Ann Int'l Rel Physics Symp*, 2006

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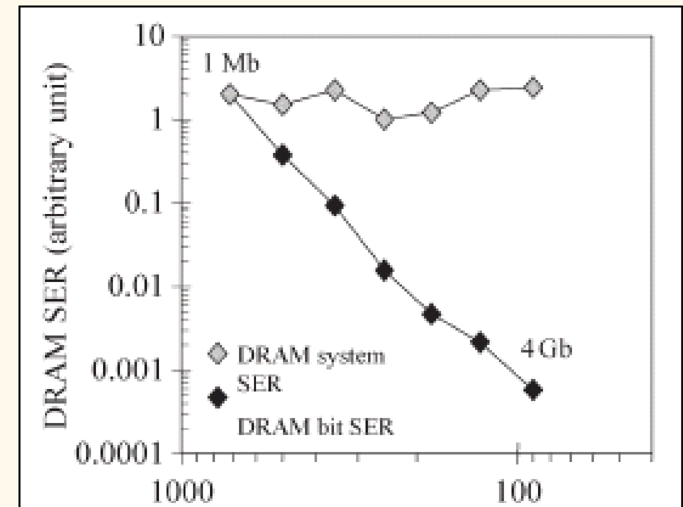
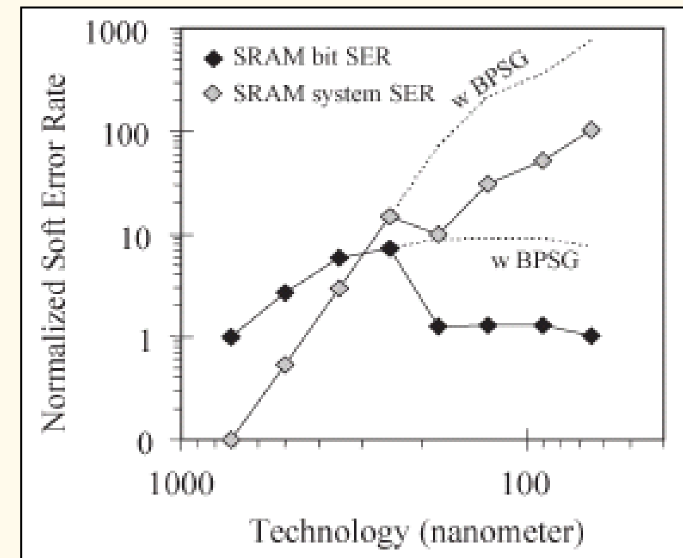
Scaling Effects: DRAM & SRAM Systems

- DRAM
  - Continuous improvement in bit SER with each technology cycle
  - Substantial increase in bits/system → essentially constant SER



- SRAM
  - Elimination of BPSG layers (^{10}B source) → decreasing bit SER
  - Substantial increase in density and SRAM % in processors → steadily increasing system SER



R.C. Baumann (TI), *IEEE Trans on Dev & Matl Rel*, 5(3), 2005

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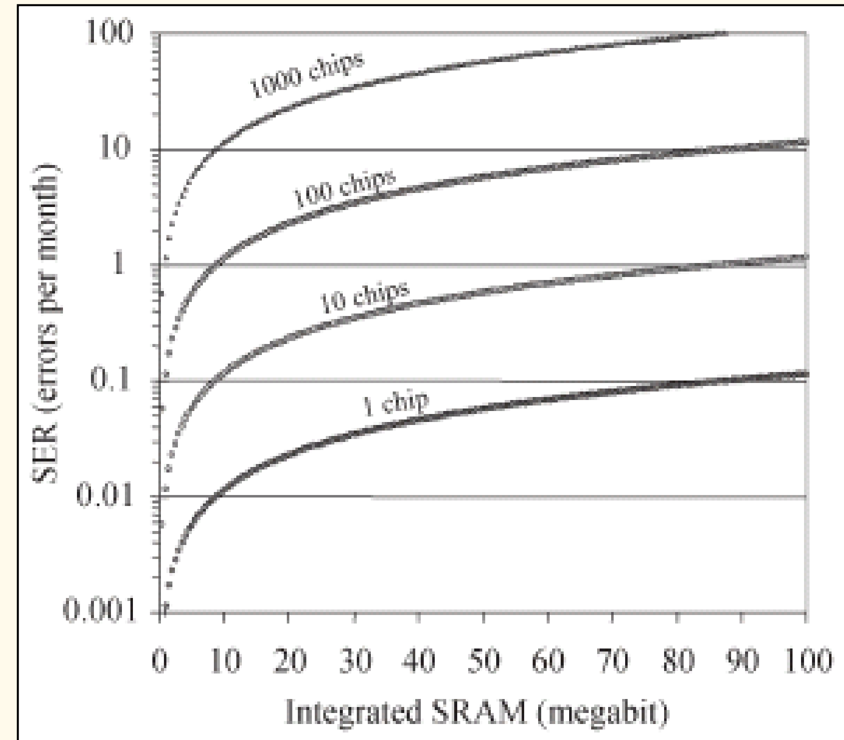
Scaling Effects: Single vs. Multi-Chip

- Single chip/low complexity systems
  - Example: cell phones & other portable electronics
  - SEU error rate likely acceptable for intermittent use unless critical areas exposed
- Multi-chip/high reliability systems
  - Example: enterprise servers
  - SEU error rate unacceptably high for contiuous use/safety critical applications (**up to 50,000 FITs!**)
  - SEU/MEU likely dominant failure mechanism



Software/hardware mitigation must be dictated by system complexity and reliability requirements

R.C. Baumann (TI), *IEEE Trans on Dev & Matl Rel*, 5(3), 2005

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IC Degradation Mechanisms

- Failure Mechanisms
  - Time-dependent dielectric breakdown (TDDB)
    - Large conductance increase immediately prior to failure
  - Electro-migration (EM)
    - Shorts & opens due to current-assisted atomic diffusion and subsequent void growth
  - Others
    - Stress migration (diffusion of carriers & defects) – weak scaling effects
    - CTE mismatch (thermal cycling-induced cracking) – very weak scaling

- Drift Mechanisms
  - Negative bias temperature inversion (NBTI): low E fields, high T
  - Hot carrier injection (HCI): high E fields, low T
  - Both cause increased V_{th} and decreased channel mobility, transconductance, and drain saturation current

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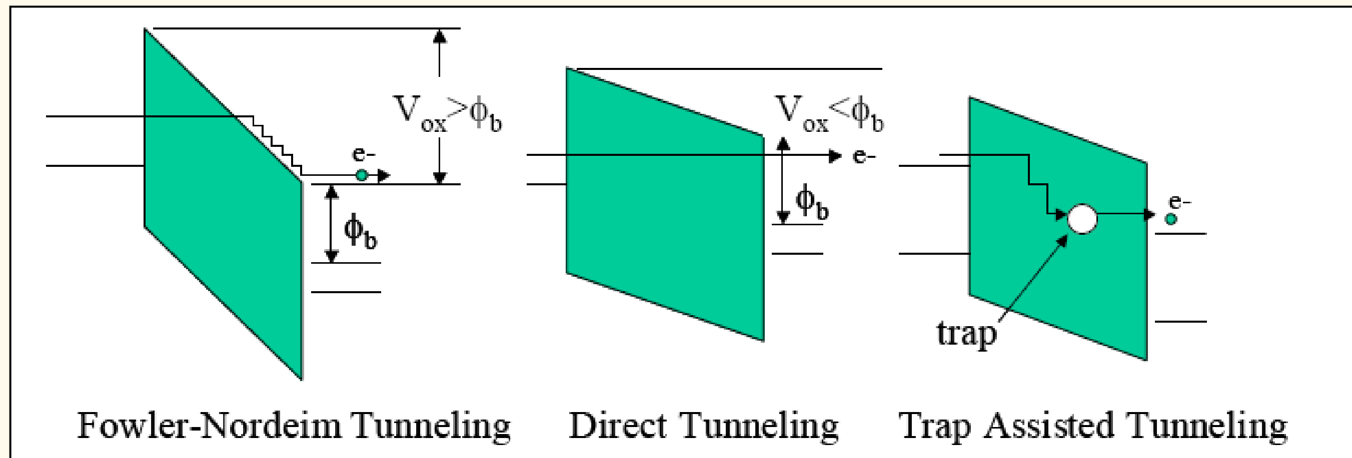
TDDB: Defect Generation

- IC scaling leads to increased E_{ox} across dielectric
- Fowler-Nordheim tunneling (thick layer, > 10 nm)
  - e^- tunnels through oxide barrier into conduction band of oxide
- Direct tunneling (thin layer)
- Trap-assisted tunneling
  - e^- tunnels into traps in oxide, and then into Si



J.B. Bernstein *et al.* (CALCE, AVSI), 2008

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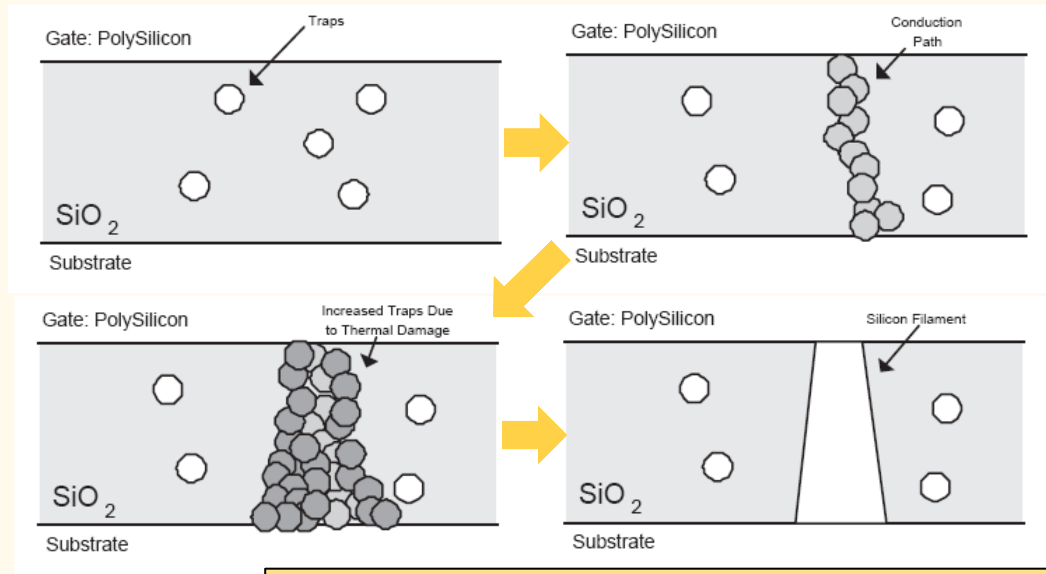
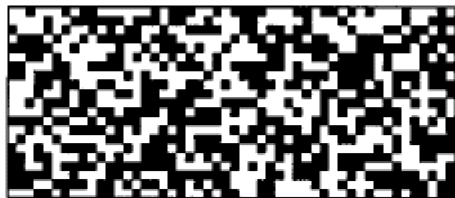
TDDB Failure Model: Percolation

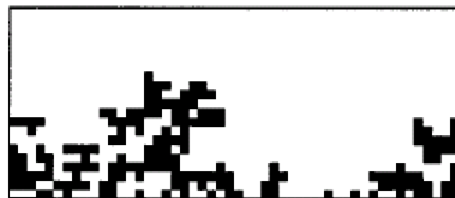
- Thick film
  - Defect population proportional to E_{ox}
- Thin film
  - Defect population proportional to V_g



Schematic: J.B. Bernstein *et al.* (CALCE, AVSI), 2008



50% defect population



Continuous pathways

Probability increases as:

- Thickness decreases
- Area (W, L) increases

2D Simulation: J.H. Stathis (IBM), *IEEE Trans on Dev & Matl Rel*, 1(1), 2005

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TDDB: Time to Failure Models

Thick film models

- Fowler-Nordheim model: $$t_f = t_o \cdot \exp\left(\frac{A}{E_{ox}}\right) \cdot \exp\left(\frac{E_a}{k_b T}\right)$$
- Thermo-chemical model: $$t_f = t_o \cdot \exp\left(-AE_{ox}\right) \cdot \exp\left(\frac{E_a}{k_b T}\right)$$
- Significant divergence for fields below 9 MV/cm

Thin film model: $$t_f = A \cdot \left(\frac{F}{W \cdot L}\right)^{\frac{1}{\beta}} \cdot V_g^{a'+b'T} \cdot \exp\left(\frac{a(V)}{T} + \frac{b(V)}{T^2}\right)$$

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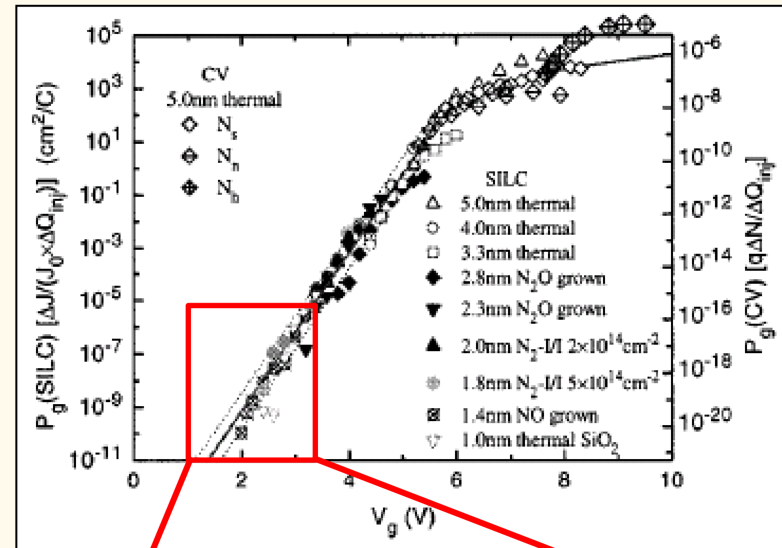
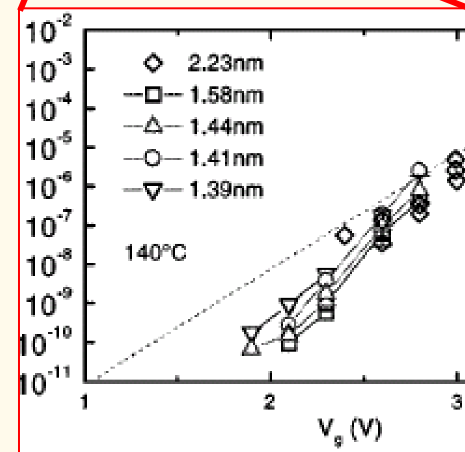
TDDB: Scaling Effects

- Two (three?) dominant regions
  - Impact ionization/anode hole injection > 5V
  - Trap creation/H+ release ~2V < x < 5V
  - Change in behavior below ~2V unclear
- Extrapolation within trap creation regime justified
- Extrapolation to below 2.5V will likely lead to pessimistic estimates of failure rates and hence overly conservative designs

Unaccelerated testing required to accurately capture time to breakdown for ultra-thin oxides





J.H. Stathis (IBM), *IEEE Trans on Dev & Matl Rel*, 1(1), 2005

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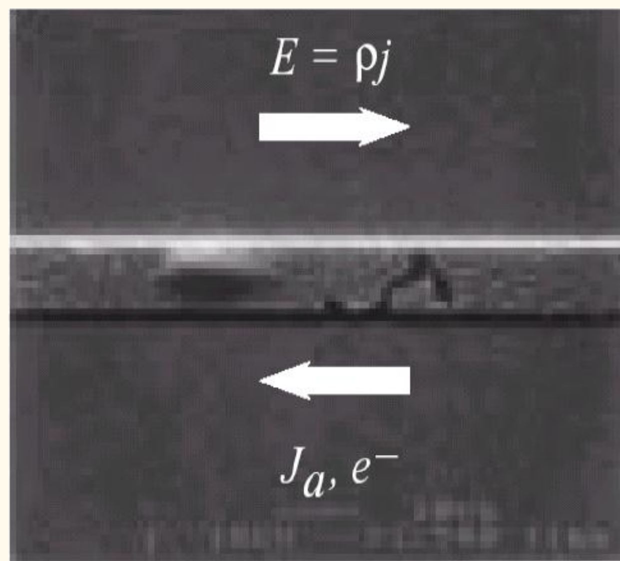
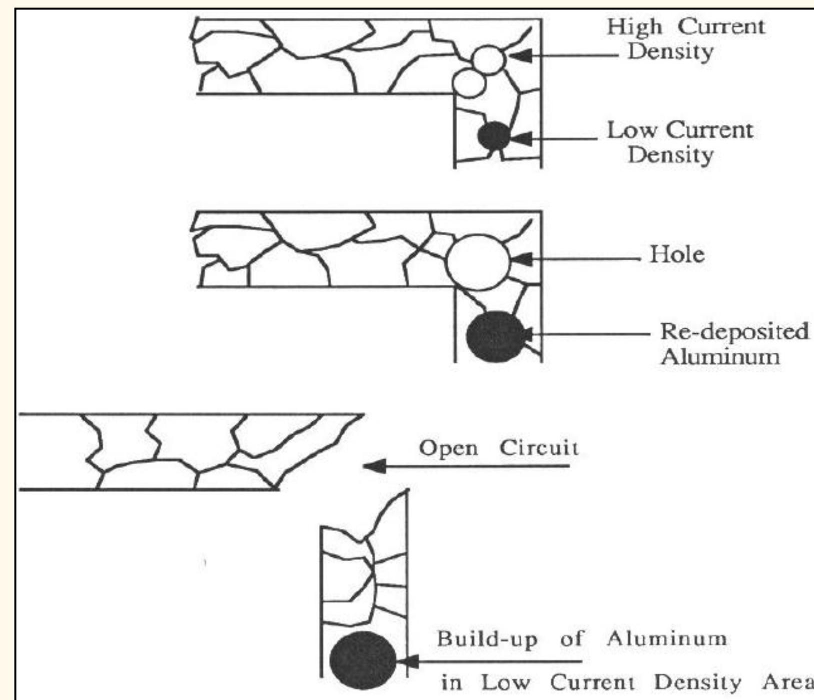
Electro-Migration

- At high current densities, momentum transfer occurs between electrons and metal atoms: "electron wind"
- Atomic diffusion along direction of current

Accumulation
Hillocks
Shorts



Depletion
Voids
Opens



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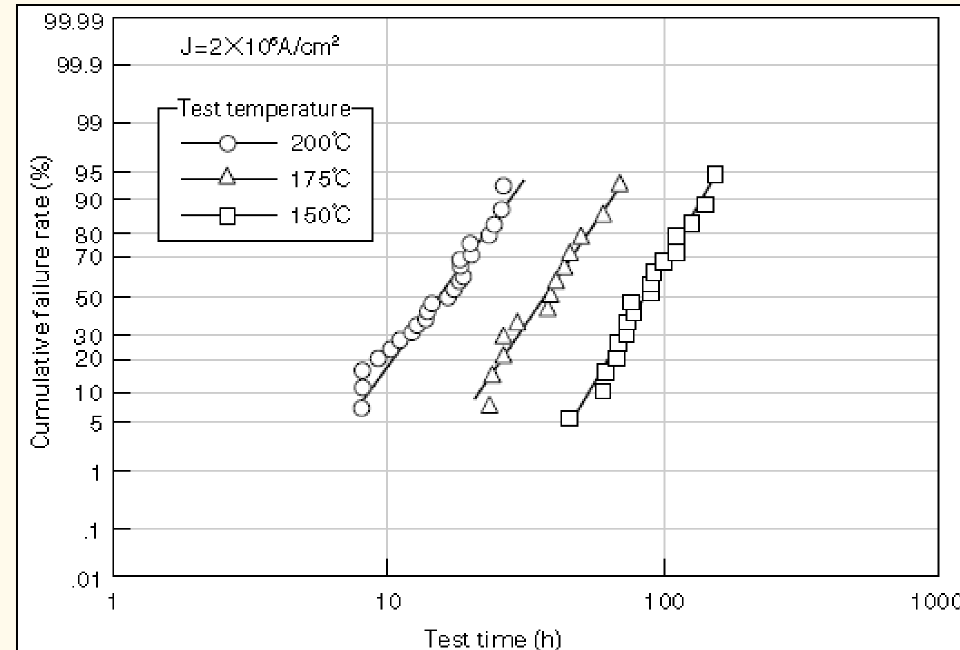
Electro-Migration: Models & Data

- Time-to-failure model: $$t_f = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k_b T}\right)$$
- EM is limiting factor for Al lines below 0.18 um
- Cu: 100X longer lifetime



Sony Products – Failure Mechanisms

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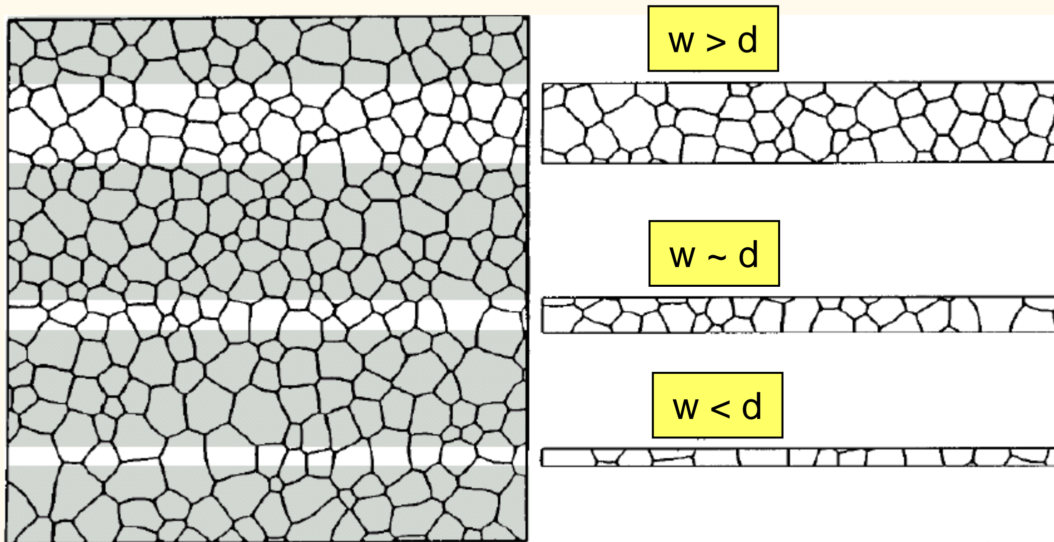
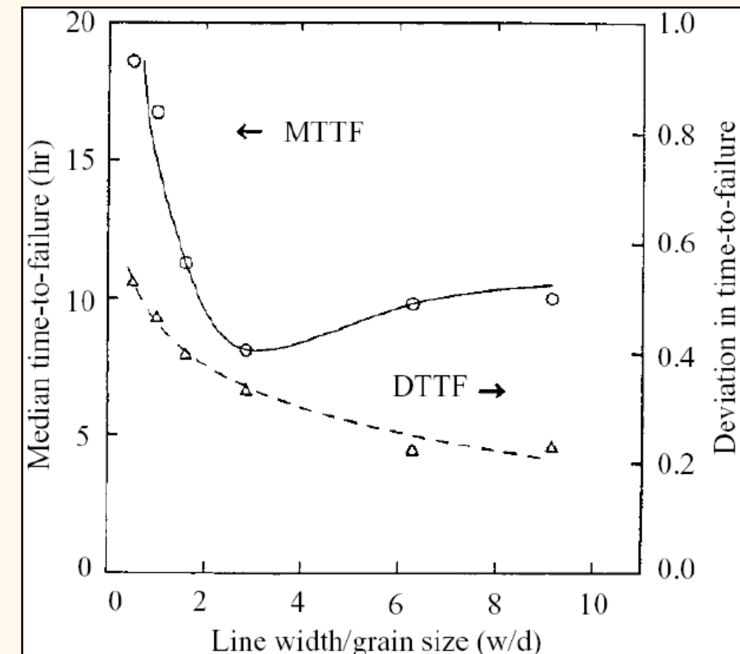
Electro-Migration: Scaling Effects

- Metal atom diffusion fastest along grain boundaries
- Variation in lifetime of lines due to grain boundary orientation and geometric defects
- Lowest lifetime for w ~ 2-3d (line grain size)





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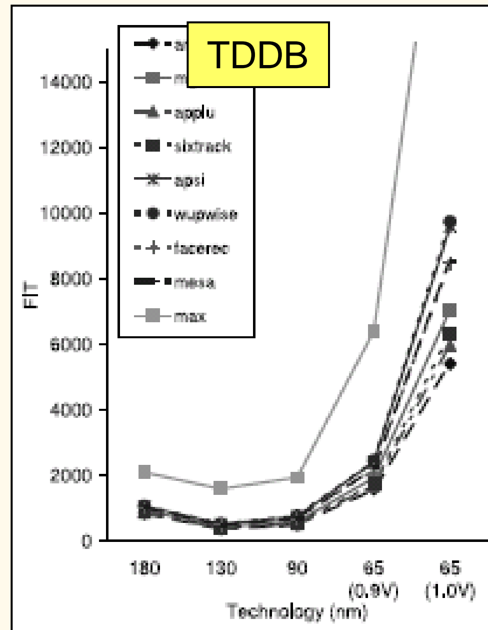
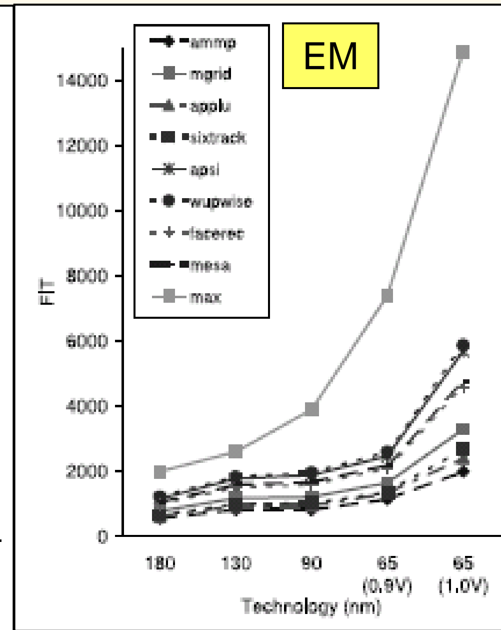
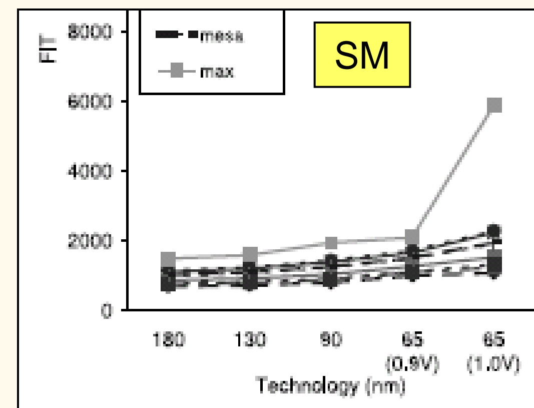
TDDB vs. EM: Relative Scaling

- RAMP simulation results for multiple structures on model processor chip
- TDDB dominant contributor to overall FIT rate at low feature sizes
- EM FIT rate slightly lower





- Stress migration effects increase only slightly with tech cycle
- Thermal cycling also considered: negligible trend



J. Srinivasan *et al.* (UIUC & IBM), *Intl Conf on Dep Sys & Networks*, 2004

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Negative Bias Temperature Instability

- Failure mechanism
  - Occurs mainly in p-MOSFETs stressed with negative V at high T
    - E_{ox} < 6 MV/cm, T=100-250ºC
  - Exacerbated by combined electric field and temperature, rather than by either stress alone
- Time to failure models:

$$t_f = C \cdot E_{ox}^{-n} \cdot \exp\left(\frac{E_a}{k_b T}\right)$$

$$t_f = D \cdot \exp\left(-\beta V_g\right) \cdot \exp\left(\frac{E_a}{k_b T}\right)$$

- Expected scaling:
  - Increasingly severe for ultra-thin oxides at low E_{ox}

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Hot Carrier Injection

- Failure mechanism:
  - Channel carriers from source of MOSFET accelerate due to high E
  - Impact ionization in drain causes holes and electrons to accelerate into interface
  - Carriers that overcome surface energy create interface states & oxide charges (holes ~ 100-1000X more effective than electrons)
- Time to failure model: $t_f = A \cdot \left(\frac{I_{sub}}{W} \right)^{-n} \cdot \exp\left(\frac{E_a}{k_b T} \right)$
  - W: interfacial width
  - E_a: -0.20 to -0.06 eV (more prevalent at *lower* temp)
- Expected scaling:
  - Very little data in the literature
  - Increased effects at shorter channel lengths due to higher trap densities, but less significant than NBTI

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Advanced Packaging

Component Packaging Requirements

- Higher frequencies and data transfer rates
  - Lower resistance-capacitance (RC) constants
- Lower voltage, but higher current
  - Joule heating is I^2R
- Higher densities
  - More inside less
- Tradeoff between high T_g vs. low T_g underfills
  - Solder wearout vs. brittle low-K dielectrics

Changes result in less robust package designs

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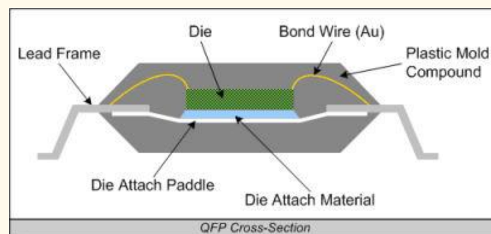
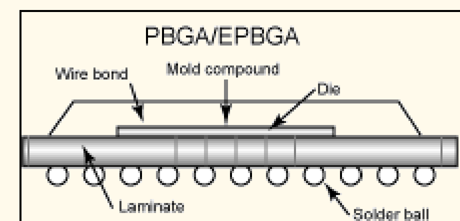
Solder Wearout in Advanced Packaging

- Elimination of leaded devices
  - Provides lower RC and higher package densities
  - Reduces compliance

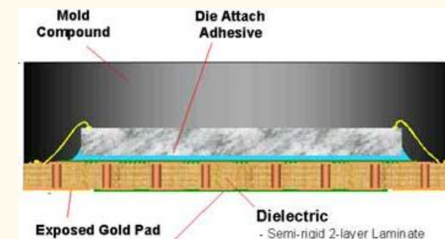
Cycles to failure
-40 to 125°C



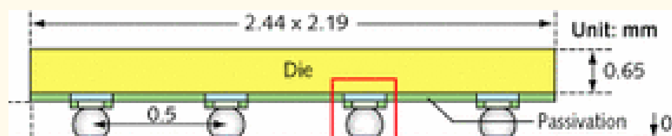
QFP: >10,000



BGA: 3,000 to 8,000



QFN: 1,000 to 3,000



CSP / Flip Chip: <1,000

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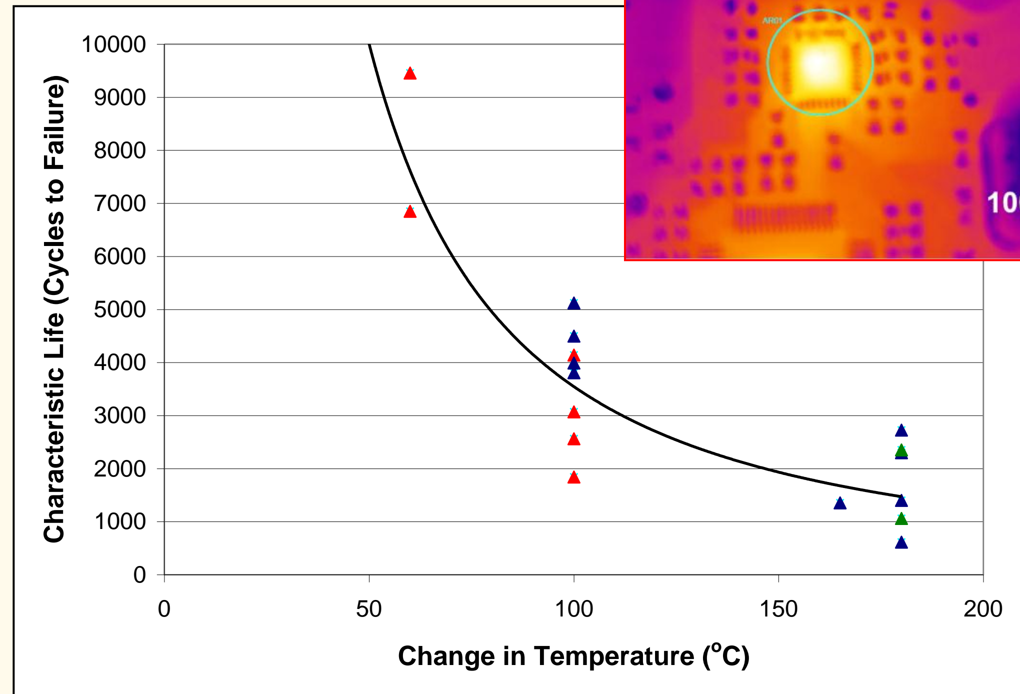
Solder Wearout (cont.)

- Lower voltage, higher currents = higher junction temperatures
  - Increases in change in temperature (ΔT)

$$t_f = \Delta T^n$$

n = 2 (SnPb)
n = 2.3 (SnNiCu)
n = 2.7 (SnAgCu)



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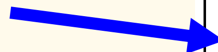
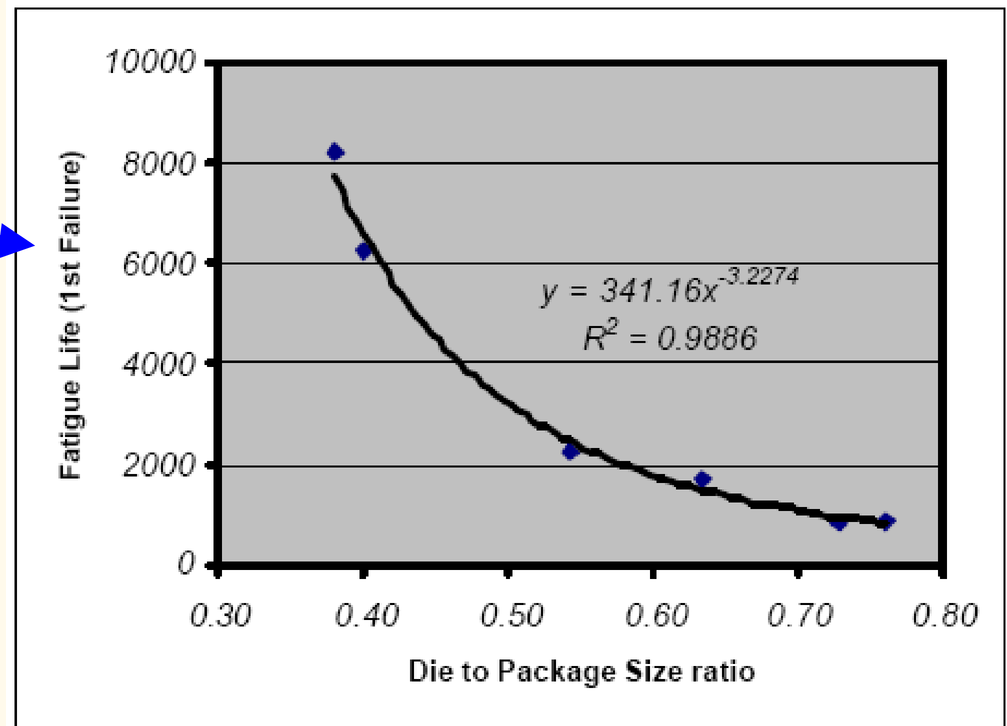
Solder Wearout (cont.)

- Design change: more silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)

- This example is only for one-dimension



- Increasing use of 3-dimensional package will drive fatigue life even lower



BOARD LEVEL ASSEMBLY AND RELIABILITY CONSIDERATIONS FOR QFN TYPE PACKAGES, Ahmer Syed and WonJoon Kang, Amkor Technology.

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Current Status

Statement from a major OEM of telecom architecture:

We have recently observed solder joint failure in memory components subjected to 400 cycles during our -20°C to 80°C product qualification test

We are greatly concerned about the potential implications regarding long-term reliability

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Solder Wearout Testing

- Industry approach has been unsatisfactory
- Primary focus for temperature cycling is JESD22-A104C
  - Testing is performed on unassembled device (off-board)
  - No assessment of 2nd level interconnect robustness
- Board level temperature cycling testing is not standardized
  - Some re-perform JESD22-A104C
    - 0°C–100°C to -65°C–150°C; # of cycles not specified
  - Some test based on IPC 9701A
    - 0°C–100°C to -55°C–125°C; cycles range from 200 to 6,000
  - Some rely on contract packaging manufacturers
  - Some test to spec (zero failures); some test to failure

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Industry Response

- Part manufacturers are reducing severity of 2nd level interconnect testing
  - Fewer perform -40 to 125°C; more often 0 to 100°C
  - Fewer cycles (1000 down to 500)

- Approach acceptable to primary market (computer, mobile phone)
  - Limited lifetime; benign environments
  - Temp cycling may not be required for product qual

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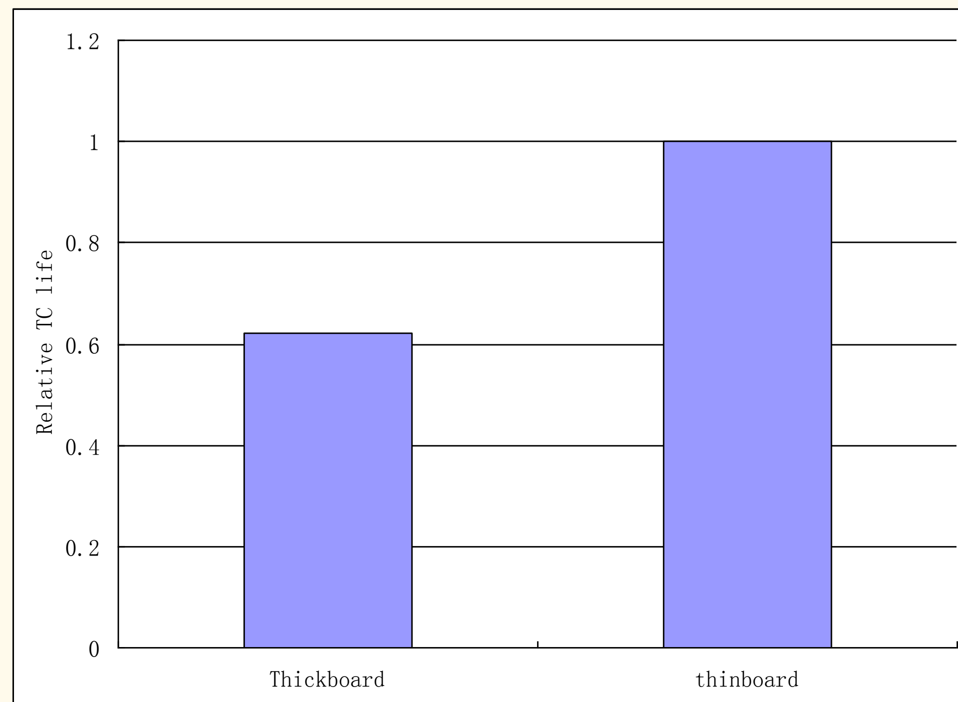
Industry Response (cont.)

- Part manufacturers have moved to thinner test boards
  - From 0.6 mm to 1.0 mm (JEDEC JESD22-B111)



- Can increase time to failure by 2x to 3x compared to standard 1.6 to 3.2 mm PCBs

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Conclusions

- There are numerous challenges ahead for successful implementation of SSD in high-reliability, long-term applications
- Drivers for improved performance and capability increase the likelihood of wearout
- Opportunities for knowledge gap between part manufacturers, SSD OEMs, and end-users

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