Design for Reliability & Sourcing of Printed Circuit Boards

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DfR Course Abstract

• Designing printed boards and assemblies today is more difficult than ever before because of the increased lead free process temperature requirements and associated changes required in manufacturing. Not only has the density of the electronic assembly increased, but many changes are taking place throughout the entire supply chain regarding the use of hazardous materials and the requirements for recycling. Much of the change is due to the European Union (EU) Directives regarding these issues. The RoHS and REACH directives have caused many suppliers to the industry to rethink their materials and processes. Thus, everyone designing or producing electronics has been or will be affected.
Instructor 1 Biography

- Cheryl Tulkoff has over 22 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She holds leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years and is also an ASQ Certified Reliability Engineer.

- She has a strong passion for pre-college STEM (Science, Technology, Engineering, and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.
Instructor 2 Biography

- Dr. Viktor Tiederle has over 29 years of experience in interconnection technology for microelectronic devices. He has worked in nearly all areas from development to production with the emphasis on quality and reliability. He started with his work in thick film technology and soldering techniques in SMD ceramics in the early 1980’s. Later he worked in wire bonding technique as well as in adhesive technology and developing micromechanical devices for automotive applications. Since more than 10 years he is responsible for many projects within the automotive as well as other industrial segments, for example in photovoltaic.

- Viktor earned his Diploma of Physics at the Technical University of Munich and Stuttgart. After some years of industrial work he received his Dr.-Eng. degree with a studying Design of Experiments used for wire bonding technique in several applications.

- Viktor works in several working groups in the automotive industry for qualifying components for the use in such hazard environments.
Course Outline

MODULE 1: INTRODUCTIONS
• Intro to Design for Reliability
• DfR & Physics of Failure

MODULE 2: COMPONENTS
• Selection
• Critical Components
• Moisture Sensitivity Level
• Temperature Sensitivity Level
• Electrostatic Discharge
• Plating Material
• Miscellaneous
• Lifetime
• Derating & Uprating

MODULE 3: MECHANISMS & PHYSICS OF FAILURE

MODULE 4: PRINTED CIRCUIT BOARDS
  o Surface Finishes
  o Cracking & Delamination
  o Laminate Selection
  o PTH Barrel Cracking
  o CAF
  o Strain/Flexure Issues & Pad Cratering
  o Cleanliness
  o Electrochemical Migration

MODULE 5: Printed Circuit Board Sourcing

MODULE 6: Focus on DfR in Manufacturing
Design for Reliability (DfR) Defined

- **DfR**: A process for ensuring the reliability of a product or system during the design stage before physical prototype.

- **Reliability**: The measure of a product’s ability to
  - ...perform the specified function
  - ...at the customer (with their use environment)
  - ...over the desired lifetime
Why Design for Reliability (DfR)?

• The **foundation** of a reliable product is a robust design
  – Provides margin
  – Mitigates risk from defects
  – Satisfies the customer
Why DfR?

Architectural Design for Reliability, R. Cranwell and R. Hunter, Sandia Labs, 1997
Why DfR? (continued)

Reduce Costs by Improving Reliability Upfront

Cost Of Unreliability
2x More

1 x

100 x

1000 x

CONCEPT

DESIGN

VALIDATION

PRODUCTION

- Ideas/Sketches
- Engineering/Design
- Specs/Drawings
- Lost Market Share
- Verification/Testing
- Lost Production
- Warranty/Recall
- Prototype Parts
Who Controls Hardware Design?

Electrical Designer
• Component selection
  – Bill of materials (BOM)
  – Approved vendor list (AVL)

Mechanical Designer
• PCB Layout
• Other aspects of electronic packaging

Both parties play a critical role in minimizing hardware mistakes during new product development.
When Do Mistakes Occur?

• Insufficient exchange of information between electrical design and mechanical design

• Poor understanding of supplier limitations

• Customer expectations (reliability, lifetime, use environment) are not incorporated into the new product development (NPD) process

“You don’t know what you don’t know”
Reality of Design for Reliability (DfR)

• Ensuring reliability of electronic designs is becoming increasingly difficult
  – Increasing complexity of electronic circuits
  – Increasing power requirements
  – Introduction of new component and material technologies
  – Introduction of less robust components

• Results in multiple potential drivers for failure
Reality (continued)

• Predicting reliability is becoming problematic
  – Standard MTBF calculations can tend to be inaccurate
  – A physics-of-failure (PoF) approach can be time-intensive and not always definitive (limited insight into performance during operating life)
Limitations of Current DfR

• Too broad in focus (not electronics focused)

• Too much emphasis on techniques (e.g., FMEA and FTA) and not answers
  – FMEA/FTA rarely identify DfR issues because of limited focus on the failure mechanism

• Overreliance on MTBF calculations and standardized product testing

• Incorporation of HALT and failure analysis (HALT is test, not DfR; failure analysis is too late)
  – Frustration with ‘test-in reliability’, even HALT, has been part of the recent focus on DfR
DfR and Physics of Failure (PoF)

• Due to some of the limitations of classic DfR, there has been an increasing interest in PoF (also known as: Reliability Physics)

• **PoF Definition**: The use of science (physics, chemistry, etc.) to capture an understanding of failure mechanisms and evaluate useful life under actual operating conditions
Why PoF is Now Important

Electronics: Today and the Future
Electronics: 1960s, 1970s, 1980s

Time

Failure Rate

No wearout!

Wearout!
PoF and Wearout

• What is susceptible to wearout in electronic designs?
  – Ceramic Capacitors (oxygen vacancy migration)
  – Memory Devices (limited write cycles, read times)
  – Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)
  – Resistors (if improperly derated)
  – Silver-Based Platings (if exposed to corrosive environments)
  – Relays and other Electromechanical Components
  – Light Emitting Diodes (LEDs) and Laser Diodes
  – Connectors (if improperly specified and designed)
  – Tin Whiskers
  – Integrated Circuits (EM, TDDB, HCI, NBTI)
  – Interconnects (Creep, Fatigue)
    • Plated through holes
    • Solder joints
Ceramic chip capacitors with high capacitance / volume (C/V) ratios
  – Can fail in **less than one year** when operated at rated voltage and temperature

**Wearout (Ceramic Capacitors)**
Wearout (Integrated Circuits)

Known trends for TDDB, EM and HCI degradation

(ref: extrapolated from ITRS roadmap)
It is becoming more challenging to achieve very high reliability for products made with advanced technologies (90nm and smaller).

"failure rate increases as we scale to smaller technologies…hard failures will present a significant and increasing challenge in future technology generations."

Pradip Bose, Jude A. Rivers, et al., IBM T.J. Watson Research Center

Increasing need to predict failure behavior before incorporating new technology in long-life systems.

Figure adapted from industry published data, 2008
IC Testing Falls Short

• Limited degree of mechanism-appropriate testing
  – Only at transition to new technology nodes
  – Mechanism-specific coupons (not real devices)
  – Test data is hidden from end-users

• Questionable JEDEC tests are promoted to OEMs
  – Limited duration (1000 hrs) hides wearout behavior
  – Use of simple activation energy, with incorrect assumption that all mechanisms are thermally activated, can result in overestimation of FIT by 100X or more
Solder Joint (SJ) Wearout

- Elimination of leaded devices
  - Provides lower RC and higher package densities
  - Reduces compliance

Cycles to failure
-40 to 125°C

- QFP: >10,000
- BGA: 3,000 to 8,000
- CSP / Flip Chip: <1,000
- QFN: 1,000 to 3,000
SJ Wearout (cont.)

- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)

![Graph showing fatigue life vs. die to package size ratio]

\[ y = 341.16x^{-3.2274} \]
\[ R^2 = 0.9886 \]
Industry Testing of SJ Wearout

- **JEDEC**
  - Specification body for component manufacturers

- **JEDEC JESD4747H, February 2011**
  - Guidelines for new component qualification
  - Requires **2300** cycles of 0 to 100C
  - Testing is often done on **thin** boards

- **IPC**
  - Specification body for electronic OEMs

- **IPC 9701A, February 2006**
  - Recommends **6000** cycles of 0 to 100C
  - Test boards should be **similar thickness** as actual design
Industry and PoF

• VITA 51.2: Physics of Failure Reliability Predictions 2011
  – Established by the standard bodies responsible for VME technology (open system architecture of real-time, modular embedded computing)
  – VITA 51.2 provides rules and recommendations for the application of Physics of Failure (PoF) methods to reliability prediction of electronics at the board, packaging and component levels. It is a compilation in good faith, of existing physics of failure models selected by consensus of the working group of best practices in industry.


• FAA and Boeing expected to require PoF for IC wearout
Implementing DfR / PoF

• Many organizations have developed DfR Teams to speed implementation
  – Success is dependent upon team composition and gating functions

• Challenges: Classic design teams consist of electrical and mechanical engineers trained in the ‘science of success’
  – PoF requires the right elements of personnel and tools
DfR / PoF Team

• Component engineer

• Mechanical / Materials engineer

• Electrical engineer

• Thermal engineer
  – Depending upon power requirements

• Reliability engineer?
  – Depends. Many classic reliability engineers provide **NO** value in the DfR / PoF process due to over-emphasis on statistical techniques and environmental testing
Component Selection

• The process of creating the bill of materials (BOM) during the ‘virtual’ design process
  – Before physical layout

• For some companies, this is during the creation of the approved vendor list (AVL)
  – Design-independent
Component Selection (continued)

• As technology progresses, functional performance has become a limited aspect of the part selection process

• Other concerns are increasingly taking center stage
  – Moisture sensitivity level (MSL)
  – Temperature sensitivity level
  – Electrostatic discharge (ESD) classification
  – Manufacturability (Design for Assembly)
  – Plating material
  – Lifetime / Long-term reliability
    • Sometimes Physics of Failure is required
Critical Components

• Most small to mid-size organizations do not have the resources to perform a thorough part selection assessment on every part
  – Does not excuse performing this activity
  – Requires focusing on components critical to the design

• Critical Components: A narrowed list of components of most concern to the OEM
  – Sensitivity of the circuit to component performance
  – Number of components within the circuit
  – Output from FMEA / FTA
  – Past experiences
  – Complexity of the component
  – Industry-wide experiences
Critical Components (Industry Experience)

- **Optoelectronics**
  - High volume controls not always in place
  - Wearout can initiate far before 20 years
- **Low volume or custom parts**
  - Part is no longer a commodity item
- **Memory devices**
  - Non-volatile memory has limited data retention time and write cycles
- **Parts with mechanical movements (switches, relays, potentiostats, fans)**
  - Depending on environment, wear out can initiate far before 20 years
- **Surface mount ceramic capacitors**
  - Assembly issues
Critical Components (continued)

• New technologies or state-of-the-art
  – At the limit of the manufacturer’s capabilities
  – MEMS, 45-nm technology, green materials, etc.

• Electronic modules
  – Part is a miniature assembly (no longer a commodity item)

• Power components

• Fuses
  – Susceptible to quality issues

• Electrolytic capacitors
  – Depending on environment, wear out can initiate far before 20 years
Popcorning

- Moisture can be absorbed by polymeric material during transportation, storage and handling
  - Epoxy encapsulant
  - Die attach
  - Printed substrate
- Trapped moisture can experience sudden liquid-gas phase transition during reflow
  - Sudden volume increase due to vaporization
- Cracking and delamination – sometimes accompanied by popping sound
- Driven by package design, materials, storage conditions and reflow parameters
MSL Issues and Actions (continued)

• Most ‘standard’ components have a maximum MSL 3
• Components with MSL 4 and higher
  – Large ball grid array (BGA) packages
  – Encapsulated magnetic components (chokes, transformers, etc.)
  – Optical components (transmitters, transceivers, sensors, etc.)
  – Modules (DC-DC converters, GPS, etc.)
• MSL classification scheme in J-STD-020D is only relevant to SMT packages with integrated circuits
  – Does not cover passives (IPC-9503) or wave soldering (JESD22A111)
  – If not defined by component manufacturer, requires additional characterization
Moisture Sensitivity Level (MSL)

- Popcorning controlled through moisture sensitivity levels (MSL)
  - Defined by IPC/JEDEC documents J-STD-020D and J-STD-033B

- Higher profile in the industry due to transition to Pb-free and more aggressive packaging
  - Higher die/package ratios
  - Multiple die (i.e., stacked die)
  - Larger components

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<td>1 year</td>
</tr>
<tr>
<td>2a</td>
<td>4 weeks</td>
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<td>72 hours</td>
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<td>48 hours</td>
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<tr>
<td>5a</td>
<td>24 hours</td>
</tr>
<tr>
<td>6</td>
<td>Time on Label (TOL)</td>
</tr>
</tbody>
</table>
MSL: Typical Issues and Action Items

- Identify your maximum MSL
  - Driven by contract manufacturer (CM) capability and OEM risk aversion
  - Majority limit between MSL3 and MSL4 (survey of the MSD Council of SMTA, 2004)
    - High volume, low mix: tends towards MSL4
    - Low volume, high mix: tends towards MSL3
- Not all datasheets list MSL
  - Can be buried in reference or quality documents
- Ensure that listed MSL conforms to latest version of J-STD-020
Aluminum and Tantalum Polymer Capacitors

Aluminum Polymer Capacitor ↑

Tantalum Polymer Capacitor ✅
Popcorning in Tantalum/Polymer Capacitors

- Pb-free reflow is hotter
  - Increased susceptibility to popcorning
  - Tantalum/polymer capacitors are the primary risk

- Approach to labeling can be inconsistent
  - Aluminum Polymer are rated MSL 3 (SnPb)
  - Tantalum Polymer are stored in moisture proof bags (no MSL rating)
  - Approach to Tantalum is inconsistent (some packaged with dessicant; some not)

- Material issues
  - Aluminum Polymer are rated MSL 3 for eutectic (could be higher for Pb-free)
  - Sensitive conductive-polymer technology may prevent extensive changes

- Solutions
  - Confirm Pb-free MSL on incoming plastic encapsulated capacitors (PECs)
  - More rigorous inspection of PECs during initial build
Temperature Sensitivity

• Limits on process temperatures provided by component manufacturer
  – Components of concern with SnPb (220°C peak) included RF devices and some optoelectronic components

• Broader issue due to introduction of Pb-free processes (260°C peak)
  – Initially limited: SnPb reflow sensitive components, SMT connectors, ceramic capacitors, SMT electrolytic capacitors

• Primary issue for some OEMs
  – Current component packaging technology is insufficiently robust
  – Numerous components in a telecom / enterprise design now have peak temperatures below 260°C
Component Selection for ESD

- Industry movement to decreasing feature sizes and high frequency technology
  - 90nm → 65nm → 45nm
  - GaAs / SiGe desirable at high GHz

- Increasing ESD risks
  - More parts are ESD susceptible
  - ESD sensitivity is increasing (is Class 0 still sufficient?)
Design for ESD Prevention: What Do You Need to Do?

- ESD Protection is necessary at the IC, component package and system level
  - Different approaches are needed to achieve reliable protection
- Designing for ESD impacts both the product design and the manufacturing process controls
- What technologies are available to assure a reliable ESD protected product?
  - At the IC level
  - At the component package level
  - At the system level
Good General Design Practices for ESD Prevention

• Know the ESD rating for each part, and select parts (where possible) for the best ESD rating
  – Identify all ESD Sensitive Parts on drawings
  – Mark Locations of ESD Sensitive parts on the Board with the ESD symbol

• Consider the entire System (Design) as ESD Sensitive

• Use ESD Protection on all susceptible parts (not just System I/Os)
  – Box or System I/O
    • ESD Rating < Class 2 IEC 1000-4-2 (4000V) MANDATORY
  – Internal Components (not exposed to outside connectors)
    • ANSI/ESDA/JEDEC JS-001-2011, Human Body Model (HBM) - Component Level
      – ESD Rating <= Class 1 MANDATORY
      – ESD Rating < Class 2 WHEREEVER POSSIBLE
DfR and Tin Whiskers

• The first step is to focus DfR on **critical components**

• Critical components are based upon three pieces of knowledge
  – The overwhelming majority of tin-plated electronic parts are matte tin over copper
  – Matte tin over copper produces whiskers of a finite length
  – Whiskers tend to only break off during handling
Where are the Scary Whiskers?

• When do really long whiskers occur?
  – Usually bright tin and/or plating over a substrate material other than copper (brass, bronze, steel, etc.)

NASA (Leidecker): 18 mm over +10 years

DfR (Fischer): +2 mm over 6 months

Tin (bright?) over steel

Tin (matte?) over brass
Critical Components

• Spacings of less than 500 microns
  – Parts with 0.8 mm lead pitch or less
  – 0201 chip components
  – Metal can housing

• Contact points (connector flex circuitry)
  – Stress gradients could change maximum length

• Welds (electrolytic capacitors)
  – Stress gradients could change maximum length

• Note: Some organizations specify the critical spacing as 350 microns
  – 0.65 mm pitch or less
How to Mitigate?

• There are three basic approaches to mitigation
  • Data Gathering and Monitoring
  • Part Manufacturer Mitigation
    – Steps offered by your suppliers
  • Equipment Manufacturer (OEM) Mitigation
    – Steps you have to perform yourself
Data Gathering and Monitoring

- Driven by iNEMI and JEDEC (JESD22A121A, JESD201A, JP002)
- Industry recommended qualification tests
  - Ambient (30C/60%RH, 4000 hrs)
  - Elevated (55C/85%RH, 4000 hrs)
  - Cyclic (-40 to 85C, 1500 cycles)
  - Shorter test times for consumer products
- Use manufacturer’s data, require third-party testing, or perform your own
  - Visual inspection should be performed properly
    - http://nepp.nasa.gov/whisker/background/index.htm#q6
- Few to no military/avionics manufacturers are using this approach
Part Manufacturer Mitigation

• Nickel underplate between the tin plating and the copper leadframe
  – Some question about effectiveness (IBM vs. TI)
  – Some question about minimum thickness
    • iNEMI (article) recommends 2 microns
    • ATIS requires 2 microns
    • PC manufacturer requires 1.2 microns
    • JP-002 March 2006 requires 0.5 microns
  – Might not help for ceramic substrate due to CTE mismatch
• Anneal for 1 hour at 150°C within 24 hours of plating
  – This is the approach for Freescale
• Fusing (melting of tin through dipping in a hot oil bath)
  – Excellent field history; must be performed soon after plating
• Minimum plating thickness
  – Some question about minimum thickness
    • Telecom manufacturer requires 10 microns
    • JP-002 March 2006 recommends 7 microns minimum, 10 microns nominal
Part Manufacturer Mitigation (continued)

- Some component manufacturers claim proprietary whisker-free plating formulation
  - Be skeptical; require Statistical Process Control
- Tin bismuth alloy finishes
  - Mitigation not definitive
  - Low melting point of SnPbBi ternary might pose problems in mixed assemblies
    - Some experimental evidence suggests SnPb-plating and SnBi solder is a greater risk
- Request palladium (Pd) plating – NiPdAu
  - Increasingly offered as an option, even to low volume customers (medical, industrial controls, etc.)
  - Most manufacturers have moved to Pd as a standard plating for fine-pitch components
### Leadframe Platings

Palladium and SnBi are seeing an increasing market share due to concerns with tin whiskering.

<table>
<thead>
<tr>
<th>Company</th>
<th>Package</th>
<th>Plating</th>
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</thead>
<tbody>
<tr>
<td>Intel</td>
<td>QFP / TSOP</td>
<td>Sn</td>
</tr>
<tr>
<td>Samsung</td>
<td>QFP / TSOP</td>
<td>NiPdAu</td>
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<tr>
<td>Texas Instruments</td>
<td>QFP / TSOP</td>
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<td>Toshiba</td>
<td>TSOP (Discretes)</td>
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<td></td>
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<td>NiPdAu or SnAg or SnBi</td>
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Ni-Pd-Au Finish, Cypress Semiconductor
OEM Mitigation

• Four Options
  – Procurement, Re-packaging, Post-plate or dip, Conformal coat

• Procurement / Design
  – Select only components with SnPb or Pd plating
  – May require complete change in circuit design if alternative component required
  – Rarely performed (functionality trumps reliability)

• Subcontract packaging or Re-packaging
  – SnPb or Pd plated leadframes
  – Rarely performed (cost, risk of damage)
Tin Whiskering – Conformal Coating

• Potential to provide a dual barrier
• Prevention or delay of whiskering
  – Some indication of a delay in whiskering (Rollins / Minter)
  – Short tin whiskers will eventually penetrate all current conformal coatings
  – No definitive trend in regards to coating properties
• Buckling
  – Based on calculations (Leidecker, NASA)
  – Not experimentally proven
• Limitations
  – Insufficient coverage at leads (gravity)
  – Problems with conformal coat may outweigh possible risk avoidance
• Current status:
  – Development of whisker-resistant coating
  – Assessment of single vs. double coating
Component Selection
(Misc)
Ceramic Capacitors (Cyclic Voltage)

- Reports of field failures of MLCC in AC or pulsed DC voltage
- Piezoelectric effect
  - Variant voltage will vary internal stresses, potentially inducing fatigue behavior
  - With high frequency ripple current, capacitor can vibrate (resonate).
- Fatigued specimens can contain scattered microcracks
  - Decrease in capacitance; increase in leakage current
- Concern at hundreds of kHz
  - Decreases with increasing capacitance, X7R -> Y5V
  - Avoid or use AC-rated capacitors

Sang-Joo Kim and Qing Jiangy, Microcracking and electric fatigue of polycrystalline ferroelectric ceramics, Smart Mater. Struct. 5 (1996)

Nippon Chemi-con, CAT.No.E1002I

Resistors (High Resistance)

- Board surfaces can be susceptible to periodic SIR drops
  - Especially with no-clean
  - Duration as short as 1 min
  - Down to 1 MegaOhm
  - Fine pitch, high voltage especially susceptible
- Can interfere with high resistance resistors
  - Especially chip resistors
  - Intermittent in nature
- Avoid values > 500 kOhms if used for sensing or calibration
  - Consider lower values in series
  - Use guard banding or cutouts
Sulfide Corrosion of Thick Film Resistors

- Sulfur dioxide (SO$_2$) and hydrogen sulfide (H$_2$SO$_4$) in environment
  - Sources: Black rubber, industrial pollution
  - Attacks silver material under passivation/termination
  - Creates nonconductive silver sulfide
- Drivers
  - Cracking/separation of coating/termination
    - Poor manufacturing
    - Thermal shock
  - Potting or conformal coating
    - Seems to act as a ‘sponge’
    - Holds SO$_2$ molecules in place
- Electrical opens within 1-4 years
- Avoidance
  - Orient parallel to solder wave
    - Entrance side can experience thermal shock
  - Avoid hand soldering/rework
  - Sulfur-resistant PdAg material (KOA)
Tantalum and Polymeric Capacitors

• Tantalum capacitors are selected for volumetric efficiency

• Older technology can be susceptible to ignition
  – Requires aggressive derating (50% or greater)
  – Sensitive to higher temperatures (>85C) and certain circuits

• Newer, polymeric capacitors are available
  – Significant reduction in ESR
  – Less derating
  – No risk of ignition

<table>
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<th>Ta-Poly KO (37 Batches)</th>
<th>Alum-Poly – AO (78 Batches)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 PPM FR % V Rated</td>
<td>68%</td>
<td>114%</td>
<td>235%</td>
</tr>
<tr>
<td>@50% V Rated FR (PPM)</td>
<td>9</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>@80% V Rated FR (PPM)</td>
<td>458</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>@90% V Rated FR (PPM)</td>
<td>1,700</td>
<td>19</td>
<td>0</td>
</tr>
<tr>
<td>@100% V Rated FR (PPM)</td>
<td>2,943</td>
<td>255</td>
<td>0</td>
</tr>
</tbody>
</table>
Electrolytic Capacitors

• Voltage
  – Maintain a minimum of 25-33% of rated voltage (maintains the dielectric)

• Temperature
  – Maintain adequate distance from ‘hot’ components
    • Power resistors, IGBTs, etc.
    • Seems to accelerate time to failure and can induce explosive rupturing
  – 105°C rated capacitors can be an issue at lower temperatures (below -40°C)
    • ESR increases 500X; capacitance decreases 80-90%

• Ripple Current
  – Up to 100% or greater of rated ripple current
  – Need to calculate/measure case temperature rise
  – Equivalency on bill of materials is often not maintained

• Equivalent Series Resistance (ESR)
  – Often not specified on the component data sheet
Separable Connectors

• Separable Connectors
  – One of the most common failure sites
  – First thing maintenance checks (plug / unplug)

• Hardware Design Rules
  – Blind insertion increases risk of damage or mismating (consider flex or rigid-flex)
  – All connectors should be keyed
    • Prevents reversal of I/O pins
  – Use positively retained connectors
  – Avoid use of sockets

• Specify material and thickness
Separable Connectors [Gold (Au)]

- Connections and environments
  - Hi-speed digital or critical connections
  - Low voltage (< 5V), low current (< 10mA)
  - Corrosive environment (gases such as H₂S, SO₂, Cl₂)
  - Risk of micromotion (< 2.5 µm)

- Material specifications
  - Be-Cu or P-bronze base pins
  - Nickel underplate (250 min)
  - Soft gold (Au) plating
  - 10 min (single insertion); 30 min (50 insertions); 70 min (hi-rel)
  - Porosity spec
  - No gold flash

- Contact specifications
  - 50-100 grams contact force
  - Minimum of 2 contacts; 4 preferred
  - Adequate contact wipe – 0.010” min.
  - No mating with tin plating
Separable Connectors [Tin (Sn)]

• Connections and environment
  – Power connections
  – Benign

• Tin plating design specification
  – 100 grams-force, 100 microinches (Tin Commandments)
DfR (Miscellaneous)

• Components taller then 1 inch
  – Use of staking compound to adhere to board
Component Selection (Lifetime)
Component Lifetime

• What parts are susceptible to long-term degradation in electronic designs?
  – **Ceramic Capacitors** (oxygen vacancy migration)
  – Memory Devices (limited write cycles, read times)
  – **Electrolytic Capacitors** (electrolyte evaporation, dielectric dissolution)
  – Resistors (if improperly derated)
  – Silver-Based Platings (if exposed to corrosive environments)*
  – Relays and other Electromechanical Components
  – **Light Emitting Diodes (LEDs)** and Laser Diodes
  – Connectors (if improperly specified and designed)*
  – Tin Whiskers*
  – **Integrated Circuits** (EM, TDDB, HCI, NBTI)
  – **Interconnects** (Creep, Fatigue)
    • Plated through holes
    • Solder joints

*Already discussed
Lifetime Example: Memory Devices

- Limited lifetime based on read-write cycles and retention time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum Guarantee</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Endurance</td>
<td>100,000</td>
<td>Data changes per bit</td>
</tr>
<tr>
<td>Store cycles</td>
<td>1,000,000</td>
<td>Store cycles</td>
</tr>
<tr>
<td>Data retention</td>
<td>100</td>
<td>Years</td>
</tr>
</tbody>
</table>

- Some memory devices provide data retention time for different operating temperatures (20 years at 125°C and 10 years at 150°C).
Light and Laser Diode Wearout

- Increasing importance with adoption of optical communications and LCD backlight
- Standard model for on-die wearout is:

  \[ t_f = A(J)^n \exp\left(\frac{E_a}{kT}\right) \]

- where A is a constant, J is the current density, n is an exponent
  - \( n = 1.5 - 2 \) for a large number of different LED structures
  - \( n = 6 - 7 \) for laser diodes with facet passivation
- Expression applies for units run in automatic current control (ACC), or constant current.
  - Units run at constant output power (APC), power substitutes current density (n may be higher)
  - Some models will combine power and current density
- Note: Model does not apply to die attach fatigue
  - A risk in high power, cyclic applications
Light and Laser Diode Wearout

• Estimated lifetime is not always provided

• When lifetime is provided, it is MTBF at room temp.
  – Time to 5% failure can be half the time
  – Time to failure at 40C can be half the time
  – 50K hrs can turn into 12.5K hrs

• Lifetime is not always be equivalent to failure
  – 50% reduction in intensity
Lifetime Example: Relays/Switches

• Relays are an electromechanical switch
• Minimum of four I/Os
  – Control voltage
  – Signal voltage
• What are the major concerns in regards to relay reliability?
  – Number of cycles to failure
  – Long-term non-use
  – Power dissipation and contact resistance (heating and voltage drops)
Relays/Switches (continued)

• Selection of appropriate plating
  – Idle for long periods of time: Gold contacts
  – Numerous cycles: AgCd contacts
• Sealed packages if cleaning operations
• Use of protective devices
  – Diode, resistor, capacitor, varistor, etc.
  – Prevents arcing during switching (accelerates degradation)
  – Must be nearby
• Temperature rise
  – Wide range of contact resistance in specifications
• Ensure margin between design life requirements and manufacturer’s specifications
Wearout of Relays/Switches

- **Catalog Life = 100,000 Cycles**
- **Mean Time Between Failures = 102,900**
- **Characteristic Life = 113,545**
Derating and Uprating
Component Ratings

• Definition
  – A specification provided by component manufacturers that guides the user as to the appropriate range of stresses over which the component is guaranteed to function

• Typical parameters
  – Voltage
  – Current
  – Power
  – Temperature

---

MSP430FG43x
MIXED SIGNAL MICROCONTROLLER

 absolute maximum ratings over operating free-air temperature (unless otherwise noted)!

| Voltage applied at \( V_{DD} \) | \(-0.3 \) V to \( V_{DD} \) |
| Voltage applied to any pin (see Note 1) | \(-3.3 \) V to \( V_{CC} \) |
| Diode current at any device terminal | \( \pm 2 \) mA |

Storage temperature, \( T_{SS} \) (unprogrammed device) | \(-55 \) °C to \( 150 \) °C |

(operated device) | \(-40 \) °C to \( 85 \) °C |

\( 1 \) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to \( V_{SS} \). The IGBT's base-bias voltage, \( V_{BIAS} \), is allowed to exceed the absolute maximum rating. The voltage is applied to the IGBT's bias pin when blocking the IGBT's base.

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IGBT MODULE (U series)
600V / 100A / PIM

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Features:
- Low Standby
- Compact Package
- F.C. Board Mount Module
- Converter Drive Voltage snubber Circuit

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Maximum ratings and characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Base voltage</td>
<td>( V_{CC} )</td>
<td>( V )</td>
<td>600</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector-base voltage</td>
<td>( V_{BB} )</td>
<td>( V )</td>
<td>250</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector current</td>
<td>( I_{CC} )</td>
<td>( A )</td>
<td>100</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector power dissipation</td>
<td>( P_{CC} )</td>
<td>( W )</td>
<td>250</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector current</td>
<td>( I_{CC} )</td>
<td>( A )</td>
<td>100</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector power dissipation</td>
<td>( P_{CC} )</td>
<td>( W )</td>
<td>250</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector current</td>
<td>( I_{CC} )</td>
<td>( A )</td>
<td>100</td>
<td>±30 %</td>
</tr>
<tr>
<td>Collector power dissipation</td>
<td>( P_{CC} )</td>
<td>( W )</td>
<td>250</td>
<td>±30 %</td>
</tr>
</tbody>
</table>

---

smythpackaging
Derating

• Derating is the practice of limiting stress on electronic parts to levels below the manufacturer’s specified ratings
  – Guidelines can vary based upon environment ("severe, protected, normal" or "space, aircraft, ground")
  – One of the most common design for reliability (DfR) methods

• Goals of derating
  – Maintain critical parameters during operation (i.e., functionality)
  – Provide a margin of safety from deviant lots
  – Achieve desired operating life (i.e., reliability)

• Sources of derating guidelines
  – Governmental organizations and 3rd parties
  – OEM’s
  – Component manufacturers

• Derating is assessed through component stress analysis
## Derating Guidelines (Examples)

<table>
<thead>
<tr>
<th>Part Type</th>
<th>Derating parameters</th>
<th>Severe</th>
<th>Benign</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminium electrolytic caps</td>
<td>Voltage (% max rated)</td>
<td>70%</td>
<td>80%</td>
</tr>
<tr>
<td></td>
<td>Temperature (°C)</td>
<td>$T_{\text{max}} - 20^\circ\text{C}$</td>
<td>$T_{\text{max}} - 20^\circ\text{C}$</td>
</tr>
<tr>
<td>Ceramic capacitors</td>
<td>Voltage (% max rated)</td>
<td>60%</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>Temperature (°C)</td>
<td>$T_{\text{max}} - 10^\circ\text{C}$</td>
<td>$T_{\text{max}} - 10^\circ\text{C}$</td>
</tr>
<tr>
<td>Solid tantalum capacitors</td>
<td>Voltage (% max rated)</td>
<td>70%</td>
<td>80%</td>
</tr>
<tr>
<td></td>
<td>Temperature (°C)</td>
<td>$T_{\text{max}} - 20^\circ\text{C}$</td>
<td>$T_{\text{max}} - 20^\circ\text{C}$</td>
</tr>
<tr>
<td></td>
<td>Reverse voltage (% max fwd)</td>
<td>2%</td>
<td>2%</td>
</tr>
<tr>
<td>Signal diodes</td>
<td>Forward current (% max rated)</td>
<td>90%</td>
<td>&lt;100%</td>
</tr>
<tr>
<td></td>
<td>Reverse voltage (% max rated)</td>
<td>70%</td>
<td>80%</td>
</tr>
<tr>
<td></td>
<td>Max. junction temperature</td>
<td>95°C</td>
<td>115°C</td>
</tr>
<tr>
<td>Chip resistors</td>
<td>Power dissipation(% max rated)</td>
<td>50%</td>
<td>70%</td>
</tr>
<tr>
<td>Digital MOS and bipolar ICs</td>
<td>Fanout (% max rated)</td>
<td>90%</td>
<td>&lt;100%</td>
</tr>
<tr>
<td></td>
<td>Frequency (% max rated)</td>
<td>90%</td>
<td>&lt;100%</td>
</tr>
<tr>
<td></td>
<td>Output current (% max rated)</td>
<td>90%</td>
<td>&lt;100%</td>
</tr>
<tr>
<td></td>
<td>Max. junction temperature</td>
<td>95°C</td>
<td>115°C</td>
</tr>
<tr>
<td>Linear MOS and bipolar ICs</td>
<td>Frequency (% max rated)</td>
<td>90%</td>
<td>&lt;100%</td>
</tr>
<tr>
<td></td>
<td>Output current (% max rated)</td>
<td>90%</td>
<td>&lt;100%</td>
</tr>
<tr>
<td></td>
<td>Max. junction temperature</td>
<td>95°C</td>
<td>115°C</td>
</tr>
</tbody>
</table>
Criticality of Component Stress Analysis

• Failure to perform component stress analysis can result in higher warranty costs, potential recalls
  – Eventual costs can be in the millions of dollars

• Perspective from Chief Technologist at major Original Design Manufacturer (ODM)

  “…based on our experience, we believe a significant number of field returns, and the majority of no-trouble-founds (NTFs), are related to overstressed components.”
Derating Failures

• Where are the derating mistakes?
  • Problem #1: Designers do not derate
    – Failure to perform component stress analysis
  • Problem #2: Derating does not have a practical or scientific foundation
    – Extraordinary measures are taken when inappropriate
    – Derating is excessive: ‘The more, the better’ rule
Failure to Derate

• Analog / Power Designs
  – Derating is typically overlooked during transient events
  – Especially turn-on, turn-off

• Digital
  – Excessive number of components and connections tends to limit attempts to perform component stress analysis
The Foundation of Derating

• To be effective, derating must have a practical and scientific foundation
  – Problem: Manufacturer’s ratings are not always based on a practical and scientific foundation

• Manufacturers’ viewpoint
  – Ratings are based on specific design rules based on materials, process, and reliability testing

• The reality
  – Ratings can be driven by tradition and market forces as much as science

• Best practice
  – Based on data from field returns
  – Based on test to failure qualification (especially for new suppliers)
Scientific Approach to Derating (Ta Caps)

High Impedance Circuits

- Self healing in Ta capacitors involves leakage paths in the MnO$_2$ being healed by the transformation to the higher resistance compound Mn$_2$O$_3$

- Process requires enough current to allow internal temperatures to reach 500°C

- Small amounts of current (< 50 uA) will prevent self healing
  - Leads to degradation and potential component failure

- Avoid use in circuits with impedances greater than 100 kΩ
Derating Decision Tree

• **Step 1**: Derating guidelines should be based on component performance, not ratings
  – Test to failure approach (i.e., HALT of components)
  – Quantifies life cycle cost tradeoffs
  – For smaller OEMs, limit this practice to critical components
OEM was concerned with voltage rating of tantalum capacitors after 2 reflows and use on low resistance line

Performed step stress surge test (SSST)

Derived voltage derating based on a sub-ppm failure rate
Derating Decision Tree (continued)

• **Step 2**: Derating guidelines should be based on recommendations from the component manufacturer
  – They built it; they should know it
  – Don’t trust the manufacturer? Use someone else

• **Step 3**: Derating guidelines should be based on customer requirements

• **Step 4**: Derating guidelines should be based on industry-accepted specification/standard

*Be flexible, not absolute*
Robustness - Components

- **Concerns**
  - Potential for latent defects after exposure to Pb-free reflow temperatures
  - $215^\circ C - 220^\circ C$ peak $\rightarrow$ $240^\circ C - 260^\circ C$ peak

- **Drivers**
  - Initial observations of deformed or damaged components
  - Failure of component manufacturers to update specifications

- **Components of particular interest**
  - Aluminum electrolytic capacitors
  - Ceramic chip capacitors
  - Surface mount connectors
  - Specialty components (RF, optoelectronic, etc.)
Ceramic Capacitors (Thermal Shock Cracks)

- Due to excessive change in temperature
  - Reflow, cleaning, wave solder, rework
  - Inability of capacitor to relieve stresses during transient conditions.
- Maximum tensile stress occurs near end of termination
  - Determined through transient thermal analyses
  - Model results validated through sectioning of ceramic capacitors exposed to thermal shock conditions
- Three manifestations
  - Visually detectable (rare)
  - Electrically detectable
  - Microcrack (worst-case)
Thermal Shock Crack: Visually Detectable
Thermal Shock Crack: Micro Crack

- Variations in voltage or temperature will drive crack propagation
- Induces a different failure mode
  - Increase in electrical resistance or decrease capacitance
Actions: Design

- Orient terminations parallel to wave solder
- Avoid certain dimensions and materials (wave soldering)
  - Maximum case size for SnPb: 1210
  - Maximum case size for SAC305: 0805
  - Maximum thickness: 1.2 mm
  - C0G, X7R preferred
- Adequate spacing from hand soldering operations
- Use manufacturer’s recommended bond pad dimensions or smaller (wave soldering)
  - Smaller bond pads reduce rate of thermal transfer
Actions: Manufacturing

- Solder reflow
  - Room temperature to preheat (max 2-3°C/sec)
  - Preheat to at least 150°C
  - Preheat to maximum temperature (max 4-5°C/sec)
  - Cooling (max 2-3°C/sec)
    - In conflict with profile from J-STD-020C (6°C/sec)
    - Make sure assembly is less than 60°C before cleaning

- Wave soldering
  - Maintain belt speeds to a maximum of 1.2 to 1.5 meters/minute

- Touch up
  - Eliminate
Module 3: Mechanisms and Physics of Failure (PoF)
Examples: Desired Lifetime

- Low-End Consumer Products (Toys, etc.)
  - Do they ever work?
- Cell Phones: 18 to 36 months
- Laptop Computers: 24 to 36 months
- Desktop Computers: 24 to 60 months
- Medical (External): 5 to 10 years
- Medical (Internal): 7 years
- High-End Servers: 7 to 10 years
- Industrial Controls: 7 to 15 years
- Appliances: 7 to 15 years
- Automotive: 10 to 15 years (warranty)
- Avionics (Civil): 10 to 20 years
- Avionics (Military): 10 to 30 years
- Telecommunications: 10 to 30 years
Identify Field Environment

- **Approach 1:** Use of industry/military specifications
  - MIL-STD-810,
  - MIL-HDBK-310,
  - SAE J1211,
  - IPC-SM-785,
  - Telcordia GR3108,
  - IEC 60721-3, etc.

- **Advantages**
  - No additional cost!
  - Sometimes very comprehensive
  - Agreement throughout the industry
  - Missing information? Consider standards from other industries

- **Disadvantages**
  - Most more than 20 years old
  - Always less or greater than actual (by how much, unknown)
Field Environment (continued)

• Approach 2: Based on actual measurements of similar products in similar environments
  – Determine average and realistic worst-case
  – Identify all failure-inducing loads
  – Include all environments
    • Manufacturing
    • Transportation
    • Storage
    • Field
Failure Inducing Loads

- Temperature Cycling
  - Tmax, Tmin, dwell, ramp times
- Sustained Temperature
  - T and exposure time
- Humidity
  - Controlled, condensation
- Corrosion
  - Salt, corrosive gases (Cl₂, etc.)
- Power cycling
  - Duty cycles, power dissipation
- Electrical Loads
  - Voltage, current, current density
  - Static and transient
- Electrical Noise
- Mechanical Bending (Static and Cyclic)
  - Board-level strain
- Random Vibration
  - PSD, exposure time, kurtosis
- Harmonic Vibration
  - G and frequency
- Mechanical shock
  - G, wave form, # of events
Field Environment (Best Practice)

• Use standards when…
  – Certain aspects of your environment are common
  – No access to use environment

• Measure when…
  – Certain aspects of your environment are unique
  – Strong relationship with customer

• Do not mistake test specifications for the actual use environment
  – Common mistake with vibration loads
PoF and Wearout

- What is susceptible to long-term degradation in electronic designs?
  - Ceramic Capacitors (dielectric breakdown)
  - Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)
  - Resistors (if improperly derated)
  - Silver-Based Platings (if exposed to corrosive environments)
  - Relays and other Electromechanical Components (wearout models not well developed)
  - Connectors (if improperly specified and designed)
  - Tin Whiskers
  - Integrated Circuits (next generation feature size)
  - Interconnects (Creep, Fatigue)
    - Plated through holes
    - Solder joints
PoF Example: Silver and Sulfur

- Immersion silver (ImAg) introduced in the 1990’s as the ‘universal finish’

- Benefits
  - Excellent flatness, low cost, long-term storage

- Problem
  - Sulfur reacts with silver
  - Induces creeping corrosion
ImAg (Creeping Corrosion)

- Failures observed within months
  - Sulfur-based gases attacked exposed immersion silver
  - Non-directional migration (creeping corrosion)

- Occurred primarily in environments with high sulfur levels
  - Rubber manufacturing
  - Gasoline refineries
  - Waste treatment plants
Findings

• Analysis identified copper as the creeping element (not silver)

• Cross-sections identified corrosion sites near areas with no or minimal immersion silver
  – Galvanic reaction was initiating and accelerating corrosion behavior

• What went wrong?
PoF and Testing

• Failure #1
  – Test coupons were not representative of actual product
  – No solder mask defined pads, no plated through holes

• Failure #2
  – Industry test environments are limited to 70%RH (chamber limitations)
  – Actual use environment can be more severe

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Temp (°C)</th>
<th>RH (%)</th>
<th>H₂S (ppb)</th>
<th>Cl₂ (ppb)</th>
<th>NO₂ (ppb)</th>
<th>SO₂ (ppb)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Indoor</td>
<td>30±1</td>
<td>70±2</td>
<td>10±1.5</td>
<td>10±1.5</td>
<td>200±30</td>
<td>100±15</td>
</tr>
<tr>
<td>Outdoor</td>
<td>30±1</td>
<td>70±2</td>
<td>100±15</td>
<td>20±3</td>
<td>200±30</td>
<td>200±30</td>
</tr>
</tbody>
</table>
PoF and Immersion Silver

• The Final Failure?

• Acknowledging the reactivity of silver with sulfur and moving beyond ‘test to spec’ to truly capture potential risks
  – The ‘physics’ was not well enough understood before the new material was released
Alternatives to PoF

• Step 1: Rules of Thumb
• Step 2: Best Practice
  – Follow part selection guidelines
• Step 3: Norris-Landsberg
Rules of Thumb (Constant Temperature)

• Electrolytic Capacitor lifetime becomes an issue when ambient temperatures begin to exceed 40°C on a constant basis
  – 85°C/2000 hour ratings tend to be insufficient for more than 5 year life

• Many companies limit solder joint temperature to a maximum of 75°C – 85°C
  – Some limit IC junction temperature to a similar range
Rules of Thumb (Temperature Cycling)

• In nominal environments, solder joint wearout is unlikely
  – Low power, diurnal cycling
  – Δ25C, 1 cycle per day
  – Lifetime of less than 10 years

• Greater concerns in more severe environments
  – Diurnal heat sources with sufficient fluctuation (Δ40C)
  – Diurnal power dissipation of Δ40C and greater
  – Power cycling greater than 4 cycles/day (mini-cycling)
Rules of Thumb (Temp Cycling)(cont.)

• If a solder joint fatigue is a concern, manage package styles
  – MELF parts (SMA and SMB available)
  – Crystals on ceramic substrates (especially large ones)
  – Chip resistors greater than 1812 or capacitors greater than 2225
  – Large memory devices (44, 56, 66 I/O) with Alloy 42 leadframes
  – Large I/O (≥ 44) quad flat pack no-lead (QFN)
Rules of Thumb (Vibration)

• Maintain high board natural frequency
  – Two to three times greater than low frequency peaks (>250-300 Hz)
  – Use of attachments, stiffer rail guides

• When peaks in the power spectral density (PSD) curve exceeds 0.01 G²/Hz
  – Lower threshold for higher frequency peaks
Vibration (continued)

• Failures primarily occur when peak loads occur at similar frequencies as the natural frequency of the product / design

• Natural frequencies
  – Larger boards, simply supported: 60 – 150 Hz
  – Smaller boards, wedge locked: 200 – 500 Hz
  – Gold wire bonds: 2k – 4kHz
  – Aluminum wire bonds: >10kHz
Norris-Lanzberg (SnPb)

\[ AF = \frac{N_o}{N_t} = \left( \frac{f_o}{f_t} \right)^{1/3} \left( \frac{\Delta T_t}{\Delta T_o} \right)^2 \exp \left[ 1414 \left( \frac{1}{T_{\text{max,o}}} - \frac{1}{T_{\text{max,t}}} \right) \right] \]

- \( f \) is cycling frequency, \( DT \) is change in temperature, and \( T_{\text{max}} \) is the maximum temperature
  - “o” refers to operating environment and “t” refers to test environment
- Provides comparison of test results to field reliability
  - Usable if the component manufacturer provides accelerated life testing (ALT) results for 2nd level interconnects
  - Warning: Component manufacturers can cheat (use very thin boards)
- Can not provide an absolute prediction
Norris-Lanzberg (SAC)

\[ AF = \frac{N_0}{N_t} = \left( \frac{\Delta T_t}{\Delta T_o} \right)^{2.65} \left( \frac{t_t}{t_o} \right)^{0.136} \exp \left\{ 2185 \left( \frac{1}{T_{\text{max},o}} - \frac{1}{T_{\text{max},t}} \right) \right\} \]

- \( t \) is the hot-side dwell time, \( DT \) is change in temperature, and \( T_{\text{max}} \) is the maximum temperature
  - “o” refers to operating environment and “t” refers to test environment
- Not yet widely accepted
  - Found to be inaccurate within some datasets

---

Long-Term Reliability

• Rules of Thumb, Best Practices, and Norris-Landzberg are not always sufficient
  – Good first pass

• When the risk is too high, physics of failure (PoF) calculations are irreplaceable
PoF Example: SnAgCu Life Model

- Modified Engelmaier
  - Semi-empirical analytical approach
  - Energy based fatigue

- Determine the strain range (Dg)
  \[ \Delta \gamma = C \frac{L_D}{h_s} \Delta \alpha \Delta T \]

- C is a correction factor that is a function of dwell time and temperature, \( L_D \) is diagonal distance, \( \alpha \) is CTE, \( DT \) is temperature cycle, \( h \) is solder joint height
PoF Example – SAC Model (cont.)

- Determine the shear force applied to the solder joint

\[
(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left( \frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left( \frac{2 - \nu}{9 \cdot G_b a} \right) \right)
\]

- \( F \) is shear force, \( L \) is length, \( E \) is elastic modulus, \( A \) is the area, \( h \) is thickness, \( G \) is shear modulus, and \( a \) is edge length of bond pad

- Subscripts: 1 is component, 2 is board, s is solder joint, c is bond pad, and b is board

- Takes into consideration foundation stiffness and both shear and axial loads
PoF Example – SAC Model (cont.)

• Determine the strain energy dissipated by the solder joint

\[ \Delta W = 0.5 \cdot \Delta \gamma \cdot \frac{F}{A_s} \]

• Calculate cycles-to-failure \((N_{50})\), using energy based fatigue models for SAC developed by Syed – Amkor

\[ N_f = \left(0.0019 \cdot \Delta W\right)^{-1} \]
Validation – Chip Resistors

Cycles to Failure (Experimental)

Cycles to Failure (Predicted)
PoF Example – SAC Reliability (cont.)

- How to ensure 10 year life in a realistic worst-case field environment for industrial controls?
  - American Southwest (Phoenix)
  - Dominated by diurnal cycling

<table>
<thead>
<tr>
<th>Month</th>
<th>Cycles/Year</th>
<th>Ramp</th>
<th>Dwell</th>
<th>Max. Temp (°C)</th>
<th>Min. Temp. (°C)</th>
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</thead>
<tbody>
<tr>
<td>March+November</td>
<td>60</td>
<td>6 hrs</td>
<td>6 hrs</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>April+October</td>
<td>60</td>
<td>6 hrs</td>
<td>6 hrs</td>
<td>30</td>
<td>15</td>
</tr>
<tr>
<td>May+September</td>
<td>60</td>
<td>6 hrs</td>
<td>6 hrs</td>
<td>35</td>
<td>20</td>
</tr>
<tr>
<td>June+July+August</td>
<td>90</td>
<td>6 hrs</td>
<td>6 hrs</td>
<td>40</td>
<td>25</td>
</tr>
</tbody>
</table>

+10°C at max temperature due to solar loading
PoF Example – SAC Reliability (cont.)

- Total damage in desert environment over 10 years: 0.02604

- Total damage in one cycle of -40°C to 85°C test environment: 0.00012

- Total cycles at -40°C to 85°C to replicate 10 yrs in desert: 222 cycles

At 1 cycle/hour, approximately 1 day of test equals 1 year in the field
Module 4: Printed Circuit Boards

Surface Finishes
PCB Surface Finishes

- **Definition**: A coating located at the outermost layer and exposed copper of a PCB.
  - Protects copper from oxidation that inhibits soldering
  - Dissolves into the solder upon reflow or wave soldering.
  - SnPb HASL (Hot Air Solder Leveling) being replaced by other finished due to technology and RoHS-Pb-free trends.

- **Options (no clear winner)**
  - Electroless nickel/immersion gold (ENIG)
  - Immersion tin (ImSn)
  - Immersion silver (ImAg)
  - Organic solderability preservative (OSP)
  - Pb-free HASL
  - Others (ENEPIG, other palladium, nano finishes etc.)

- **Most platings, except for Pb-free HASL, has been around for several years**
Pb-Free HASL

• Increasing Pb-free solderability plating of choice
• Primary material is Ni-modified SnCu (SN100CL)
  – Initial installations of SAC being replaced
  – Only Vicor recently identified as using SAC HASL (Electronic Design, Nov 2007)
  – Co-modified SnCu also being offered (claim of 80 installations [Metallic Resources])

• Selection driven by
  – Storage
  – Reliability
  – Solderability
  – Planarity
  – Copper Dissolution
Pb-Free HASL: Ni-modified SnCu

• Patented by Nihon Superior in March 1998
  – Claimed: Sn / 0.1-2.0% Cu / 0.002-1% Ni / 0-1% Ge
  – Actual: Sn / 0.7% Cu / 0.05% Ni / 0.006% Ge

• Role of constituents
  – Cu creates a eutectic alloy with lower melt temp (227°C vs. 232°C), forms intermetallics for strength, and reduces copper dissolution
  – Ni suppresses formation of b-Sn dendrites, controls intermetallic growth, grain refiner
  – Ge prevents oxide formation (dross inhibitor), grain refiner

Note: Current debate if Sn0.9Cu or Sn0.7Cu is eutectic
Pb-free HASL: Storage

• PCBs with SnPb HASL have storage times of 1 to 4 years
  – Driven by intermetallic growth and oxide formation

• SN100CL demonstrates similar behavior
  – Intermetallic growth is suppressed through Ni-addition
  – Oxide formation process is dominated by Sn element (similar to SnPb)

• Limited storage times for alternative Pb-free platings (OSP, Immersion Tin, Immersion Silver)
Pb-Free HASL: Reliability

• Contract manufacturers (CMs) and OEMs have reported issues with electrochemistry-based solderability platings
  – ENIG: Black Pad, Solder Embrittlement
  – ImAg: Sulfur Corrosion, Microvoiding

• Some OEMs have moved to OSP and Pb-free HASL due to their ‘simpler’ processes
Pb-Free HASL: Solderability

- Industry adage: Nothing solders like solder

- Discussions with CMs and OEMs seem to indicate satisfaction with Pb-free HASL performance
  - Additional independent, quantitative data should be gathered

- Improved solderability could improve hole fill

http://www.daleba.co.uk/download%20section%20lead%20free.pdf

http://www.circuitree.com/articleFeatureArticle/BNP_GUID_9-5-2006_A_100000000000000243033
Pb-Free HASL: Planarity

- Recommended minimum thickness
  - 100 min (4 microns)
  - Lower minimums can result in exposed intermetallic

- Primary issue is thickness variability
  - Greatest variation is among different pad designs
  - 100 min over small pads (BGA bond pads); over 1000 min over large pads

- Can be controlled through air knife pressure, pot temperatures, and nickel content
Pb-Free HASL: Planarity (cont.)

- **Air knives**
  - Pb-free HASL requires lower air pressure to blow off excess solder

- **Pot Temperatures**
  - SnPb: 240C to 260C
  - SN100CL: 255C to 270C (air knife temp of 280C)

- **Ni content**
  - Variation can influence fluidity
    - Minimum levels critical for planarity
  - Some miscommunication as to critical concentrations

Sweatman and Nishimura (IPC APEX 2006)
Pb-Free HASL: Copper Dissolution

- To be discussed in detail in solder module
- Presence of nickel is believed to slow the copper dissolution process
  - SAC HASL removes ~5 um
  - SNC HASL removes ~1 um

After 6 Passes over Wave Soldering Machine
105°C Preheat, 256°C Solder Temperature, 4 seconds contact time

www.p-m-services.co.uk/rohs2007.htm
www.pb-free.org/02_G.Sikorcin.pdf
Pb-Free HASL: Additional Concerns

• Risk of thermal damage, including warpage and influence on long term reliability (PTH fatigue, CAF robustness)
  – No incidents of cracking / delamination / excessive warpage reported to DfR to date
  – Short exposure time (3 to 5 seconds) and minimal temp. differential (+5°C above SnPb) may limit this effect

• Compatibility with thick (>0.135”) boards
  – Limited experimental data (these products are not currently Pb-free)

• Mixing of SNC with SAC
  – Initial testing indicates no long-term reliability issues (JGPP)
Electroless Nickel/Immersion Gold (ENIG)

- Two material system
  - Specified by IPC-4552

- Electroless Nickel (w/P)
  - 3 – 6 microns (120 – 240 microinches)
  - Some companies spec a broader 1 – 8 microns

- Immersion Gold
  - Minimum of 0.05 microns (2 microinches)
  - Self-limiting (typically does not exceed 0.25 microns)

- Benefits
  - Excellent flatness, long-term storage, robust for multiple reflow cycles, alternate connections (wirebond, separable connector)
ENIG (Primary Issue)

- **Solder Embrittlement**
  - Not always black pad
- **Not explained to the satisfaction of most OEMs**
- **Numerous drivers**
  - Phosphorus content
    - High levels = weak, phosphorus-rich region after soldering
    - Low levels = hyper-corrosion (black pad)
  - Cleaning parameters
  - Gold plating parameters
  - Bond pad designs
  - Reflow parameters?
- **Results in a severe drop in mechanical strength**
  - Difficult to screen
  - Can be random (e.g., 1 pad out of 300)
- **Board fabricators need to be on top of numerous quality procedures to prevent defects.**
Other ENIG Failure Mechanisms

- Insufficient nickel thickness
  - Potential diffusion of copper through the nickel underplate
  - Can reduce storage time and number of reflow cycles

- Bond pad adhesion
  - Problem with corner balls on very large BGAs (>300 I/O)

- Reduced plated through hole reliability (stress concentrators)

- Dewetting

- Crevice corrosion (trapped residues)

- Poor performance under mechanical shock / drop
ENIG & Mechanical Shock

- Boards with ENIG finishes have less shock endurance.
  - Not always consistent
- Plating is an important driver
  - SnNi vs. SnCu intermetallics
- Crossover into board failure
  - Very strain-rate dependent

<table>
<thead>
<tr>
<th>PQFP (28x28mm, 208 I/O)</th>
<th>Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pb-Free on ENIG</td>
<td>2/6</td>
</tr>
<tr>
<td>Pb-Free on OSP</td>
<td>2/6</td>
</tr>
<tr>
<td>SnPb on OSP</td>
<td>0/6</td>
</tr>
</tbody>
</table>

Chai, ECTC 2005

Chong, ECTC 2005
Immersion Tin (ImSn)

- **Single material system**
  - Defined by IPC-4554

- **Immersion Tin**
  - Standard thickness: 1 micron (40 microinches)
  - Some companies spec up to 1.5 microns (65 microinches)

- **Benefits**
  - Excellent flatness, low cost, excellent bare test pad probing

- **Not as popular a choice**
  - Environmental and health concerns regarding thiourea (known carcinogen).
  - Not good for designs with small or micro vias – etchant gets entrapped during PCB processing and “erupts” during SMT soldering
Sulfide Corrosion and Migration of Immersion Silver

- Failures observed within months
  - Sulfur-based gases attack exposed immersion silver
  - Non-directional migration (creepage corrosion)

- Occurring primarily in environments with high sulfur levels. Not recommended for these applications.
  - Rubber manufacturing
  - Waste treatment plants
  - Petroleum refineries
  - Coal-generation power plants,
  - Paper mills
  - Sewage/waste-water treatment
  - Landfills
  - Large-scale farms
  - Modeling clay
Organic Solderability Preservative (OSP)

- **Single material system**
  - Specified by IPC-4555
- **Thickness**
- **Benefits**
  - Very low cost, flatness, reworkable
- **Issues**
  - Short shelf life (6-12 months)
  - Limited number of refloows
  - Some concerns about compatibility with low activity, no-clean fluxes
  - Transparency prevents visual inspection
  - Poor hole fill
  - Test pads must be soldered – prepare for probing through no clean materials if they are used.
OSP & Hole Fill

- Fill is driven by capillary action

- Important parameters
  - Hole diameter, hole aspect ratio, wetting force, thermal relief
  - Solder will only fill as along as its molten (key point)
  - OSP has lower wetting force
    - Risk of insufficient hole fill
    - Can lead to single-sided architecture

- Solutions?
  - Changing board solderability plating
  - Increasing top-side preheat
  - Increasing solder pot temperature (some go as high as 280°C)
  - Changing your wave solder alloy

P. Biocca, Kester
Module 4: Printed Circuit Boards

Robustness Concerns
Cracking and Delamination
Printed Board Robustness Concerns

- Increased Warpage
- Solder Mask Discoloration
- Blistering
- Pad Cratering
- Delamination
- Land Separation
- PTH Cracks
Printed Board Damage

- Predicting printed board damage can be difficult
  - Driven by size (larger boards tend to experience higher temperatures)
  - Driven by thickness (thicker boards experience more thermal stress)
  - Driven by material (lower Tg tends to be more susceptible)
  - Driven by design (higher density, higher aspect ratios)
  - Driven by number of reflows
- No universally accepted industry model
Printed Board Damage: Industry Response

• Concerns with printed board damage have almost entirely been addressed through material changes or process modifications
  – Not aware of any OEMs initiating design rules or restrictions

• Specific actions driven by board size and peak temperature requirements
# PCB Robustness: Laminate Material Selection

<table>
<thead>
<tr>
<th>Board thickness</th>
<th>IR-240~250°C</th>
<th>Board thickness</th>
<th>IR-260°C</th>
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<tbody>
<tr>
<td>≤60mil</td>
<td>Tg140 Dicy</td>
<td>≤60mil</td>
<td>Tg150 Dicy</td>
</tr>
<tr>
<td></td>
<td>All HF materials OK</td>
<td></td>
<td>HF - middle and high Tg materials OK</td>
</tr>
<tr>
<td>60~73mil</td>
<td>Tg150 Dicy</td>
<td>60~73mil</td>
<td>Tg170 Dicy</td>
</tr>
<tr>
<td></td>
<td>NP150, TU622-5</td>
<td>All HF materials OK</td>
<td>HF -middle and high Tg materials OK</td>
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<tr>
<td></td>
<td>All HF materials OK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>73~93mil</td>
<td>Tg170 Dicy, NP150G-HF</td>
<td>73~93mil</td>
<td>Tg150 Phenolic + Filler</td>
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<tr>
<td></td>
<td>HF –middle and high Tg materials OK</td>
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<td>IS400, IT150M, TU722-5, GA150</td>
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<td>HF –middle and high Tg materials OK</td>
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<tr>
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<td>Tg150 Phenolic + Filler</td>
<td>93~130mil</td>
<td>Phenolic Tg170</td>
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<td>IS410, IT180, PLC-FR-370 Turbo, TU722-7</td>
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<tr>
<td></td>
<td>Tg 150</td>
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<td>HF –middle and high Tg materials OK</td>
</tr>
<tr>
<td></td>
<td>HF –middle and high Tg materials OK</td>
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<td></td>
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<tr>
<td>121~160mil</td>
<td>Phenolic Tg170</td>
<td>≥131mil</td>
<td>Phenolic Tg170 + Filler</td>
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<td>IS415, 370 HR, 370 MOD, N4000-11</td>
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<td></td>
<td>TU722-7</td>
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<td>HF –high Tg materials OK</td>
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<tr>
<td></td>
<td>HF –high Tg materials OK</td>
<td></td>
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<tr>
<td>≥161mil</td>
<td>Phenolic Tg170 + Filler</td>
<td>≥161mil</td>
<td>TBD – Consult Engineering for specific</td>
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<td>IS415, 370 HR, 370 MOD, N4000-11</td>
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<td>design review</td>
</tr>
<tr>
<td></td>
<td>HF material - TBD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Copper thickness = 2OZ use material listed on column 260 °C
2. Copper thickness >= 3OZ use Phenolic base material or High Tg Halogen free materials only
3. **Twice lamination product use Phenolic material or High Tg Halogen free materials only (includes HDI)**
4. Follow customer requirement if customer has his own material requirement
5. DE people have to confirm the IR reflow Temperature profile

---

**J. Beers, Gold Circuits**
Printed Board Damage: Prevention

- Thermal properties of laminate material are primarily defined by four parameters
  - Out of plane coefficient of thermal expansion (Z-CTE)
  - Glass transition temperature (Tg)
  - Time to delamination (T260, T280, T288)
  - Temperature of decomposition (Td)

- Each parameter captures a different material behavior
  - Higher number slash sheets (> 100) within IPC-4101 define these parameters to specific material categories
Thermal Parameters of Laminate

- **Out of plane CTE (below Tg or Z-axis: 50° to 260° C)**
  - CTE for SnPb is 50ppm - 90ppm (50C to 260C rarely considered)
  - Pb-free: 30ppm - 65ppm or 2.5 – 3.5%

- **Glass transition temperature (IPC-TM-650, )**
  - Characterizes complex material transformation (increase in CTE, decrease in modulus)
  - Tg of 110° to 170° C for SnPb
  - Pb-free: 150° C to 190° C

- **Time to delamination (IPC-TM-650, 2.4.24.1)**
  - Characterizes interfacial adhesion
  - T-260 for SnPb is 5-10 minutes
  - Pb-free: T-280 of 5-10 minutes or T-288 of 3-6 minutes

- **Temperature of decomposition (IPC-TM-650, 2.3.40)**
  - Characterizes breakdown of epoxy material
  - Td of 300° C for SnPb
  - Pb-free: Td of 320° C
PCB Robustness: Material Selection

- The appropriate material selection is driven by the failure mechanism one is trying to prevent
  - Cracking and delamination
  - Plated through fatigue
  - Conductive anodic filament formation
PCB Delamination

• Fiber/resin interface delamination occurs as a result of stresses generated under thermal cycling due to a large CTE mismatch between the glass fiber and the epoxy resin (1 vs. 12 ppm/°C)

• Delamination can be prevented/resisted by selecting resin with lower CTE’s and optimizing the glass surface finish.

• Studies have shown that the bond between fiber and resin is strongly dependent upon the fiber finish
Delamination / Cracking: Observations

• Morphology and location of the cracking and delamination can vary
  – Even within the same board

• Failure morphology and locations
  – Within the middle and edge of the PCB
  – Within prepgs and/or laminate
  – Within the weave, along the weave, or at the copper/epoxy interface (adhesive and cohesive)
Additional Observations

- **Drivers**
  - Higher peak temperatures
  - Increasing PCB thickness
  - Decreasing via-to-via pitch
  - Increasing foil thickness (1-oz to 2-oz)
  - Presence of internal pads
  - Sequential lamination

- **Limited information**
  - Controlled depth drilling

- **Extensive debate about root-cause**
  - Non-optimized process
  - Intrinsic limit to PCB capability
  - Moisture absorption

Rothschild, IPC APEX 2007
Delamination / Cracking: Root-Cause

• Non-Optimized Process
  – Some PCB suppliers have demonstrated improvement through modifications to lamination process or oxide chemistry
  – Some observations of lot-to-lot variability

• Limit to PCB Capability
  – Difficult to overcome adhesion vs. thermal performance tradeoff (dicy vs. phenolic)
  – High stresses developed during Pb-free exceed material strength of standard board material

• Moisture Absorption
Cracking and Moisture Absorption

- **Does moisture play a role?**
  - No
    - DfR found delamination primarily around the edge and away from PTH sites after MSL testing.
    - IBM found minimal differences after a 24 hr bake of coupons with heavy copper (>2 oz).
    - Delamination / cracking observed in board stored for short (<2 weeks) periods of time.
  - Yes
    - DfR customer found improvement after 48 hrs at 125C.
    - A number of companies now require 5 – 24 hour bake before reflow.
    - IBM found improvement with coupons with nominal copper.
    - DfR observed more rapid degradation of boards exposed to moisture, even after multiple refloows.
    - Some customers specifying maximum moisture absorption.

- **Where does the moisture come from?**
Cracking and Moisture (cont.)

- Storage of prepregs and laminates
- Drilling process
  - Moisture is absorbed by the side walls (microcracks?)
  - Trapped after plating
- Storage of PCBs at PCB manufacturer
- Storage of PCBs at CCA manufacturer
PCB Trace Peeling

• Delamination of trace from surface of the board

• Sources of increased stress
  – Excessive temperatures during high temperature processes
  – Insufficient curing of resin
  – Insufficient curing of solder mask

• Sources of decreased strength
  – Improper preparation of copper foil
  – Excessive undercut
PCB Robustness: Qualifying Printed Boards

- This activity may provide greatest return on investment
- Use appropriate number of refows or wave
  - In-circuit testing (ICT) combined with construction analysis (cracks can be latent defect)
  - 6X Solder Float (at 288C) may not be directly applicable
- Note: higher Tg / phenolic is not necessarily better
  - Lower adhesion to copper (greater likelihood of delamination)
  - Greater risk of drilling issues
  - Potential for pad cratering
- Higher reflow and wave solder temperatures may induce solder mask delamination
  - Especially for marginal materials and processes
  - More aggressive flux formulations may also play a role
  - Need to re-emphasize IPC SM-840 qualification procedures
Material Selection - Laminate

• Higher reflow and wave solder temperatures may induce delamination
  – Especially for marginal materials and processes
    • Not all RoHS compliant laminates are Pb-free process capable!
    • Specify your laminate by name – not type or “equivalent”
  – Role of proper packaging and storage
    • PCBs should remain in sealed packaging until assembly
      – Reseal partially opened bricks
      – Package PCBs in brick counts which closely emulate run quantities
    • PCBs should be stored in temperature and humidity controlled conditions
    • Bake when needed
    • Packaging in MBB (moisture barrier bags) with HIC (humidity indicator cards) may be needed for some laminates

• Need to re-emphasize IPC SM-840 & other qualification procedures
Module 4: PCB Robustness

PTH Barrel Cracking

Conductive Anodic Filaments (CAF)
Plated Through Holes (PTH)

- Voids
  - Can cause large stress concentrations, resulting in crack initiation.
  - The location of the voids can provide crucial information in identifying the defective process
    - Around the glass bundles
    - In the area of the resin
    - At the inner layer interconnects (aka, wedge voids)
    - Center or edges of the PTH

- Etch pits
  - Due to either insufficient tin resist deposition or improper outer-layer etching process and rework.
  - Cause large stress concentrations locally, increasing likelihood of crack initiation
  - Large etch pits can result in an electrical open
Plated Through Hole (PTH) Fatigue

- **Overstress cracking**
  - CTE mismatch places PTH in compression
  - Pressure applied during "bed-of-nails" can compress PTH
  - In-circuit testing (ICT) rarely performed at operating temperatures

- **Fatigue**
  - Circumferential cracking of the copper plating that forms the PTH wall
  - Driven by differential expansion between the copper plating (~17 ppm) and the out-of-plane CTE of the printed board (~70 ppm)
  - Industry-accepted failure model: IPC-TR-579
PTH Fatigue: Pb-Free
PTH and Pb-Free (continued)

• Findings
  – Limited Z-axis expansion and optimized copper plating prevents degradation

• Industry response
  – Movement to Tg of 150 - 170°C
  – Z-axis expansion between 2.5 to 3.5%
PCB Conductive Anodic Filaments (CAF)

- CAF also referred to as metallic electro-migration
- Electro-chemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field
- CAF can cause current leakage, intermittent electrical shorts, and dielectric breakdown between conductors in printed wiring boards
CAF: Examples

A: A Cross-Section
CAF: Examples
Module 4: PCB Robustness

Strain Flexure Issues & Pad Cratering
Electro-Chemical Migration (ECM)
Cleanliness
SAC Solder is More Vulnerable to Strain

Sources of strain can be ICT, stuffing through-hole components, shipping/handling, mounting to a chassis, or shock events.

NEMI study showed SAC is more Sensitive to bend stress.

Sources of strain can be ICT, stuffing through-hole components, shipping/handling, mounting to a chassis, or shock events.
ICT Strain: Fixture & Process Analysis

- Review/perform ICT strain evaluation at fixture mfg and in process: 500 us, IPC 9701 and 9704 specs, critical for QFN, CSP, and BGA

- To reduce the pressures exerted on a PCB, the first and simplest solution is to reduce the probes forces, when this is possible.
- Secondly, the positioning of the fingers/stoppers must be optimized to control the probe forces. But this is often very difficult to achieve. Mechanically, the stoppers must be located exactly under the pressure fingers to avoid the creation of shear points
Strain & Flexure: Pad Cratering

- Cracking initiating within the laminate during a dynamic mechanical event
  - In circuit testing (ICT), board depanelization, connector insertion, shock and vibration, etc.

G. Shade, Intel (2006)
Pad Cratering

• Drivers
  – Finer pitch components
  – More brittle laminates
  – Stiffer solders (SAC vs. SnPb)
  – Presence of a large heat sink

• Difficult to detect using standard procedures
  – X-ray, dye-n-pry, ball shear, and ball pull
Solutions to Pad Cratering

- Board Redesign
  - Solder mask defined vs. non-solder mask defined

- Limitations on board flexure
  - 500 microstrain max, Component, location, and PCB thickness dependent

- More compliant solder
  - SAC305 is relatively rigid, SAC105 and SNC are possible alternatives

- New acceptance criteria for laminate materials
  - Intel-led industry effort
  - Attempting to characterize laminate material using high-speed ball pull and shear testing, Results inconclusive to-date
Laminate Acceptance Criteria

• Intel-led industry effort
  – Attempting to characterize laminate material using high-speed ball pull and shear testing
  – Results inconclusive to-date

• Alternative approach
  – Require reporting of fracture toughness and elastic modulus
Electro-Chemical Migration: Details

• Insidious failure mechanism
  – Self-healing: leads to large number of no-trouble-found (NTF)
  – Can occur at nominal voltages (5 V) and room conditions (25°C, 60%RH)

• Due to the presence of contaminants on the surface of the board
  – Strongest drivers are halides (chlorides and bromides)
  – Weak organic acids (WOAs) and polyglycols can also lead to drops in the surface insulation resistance

• Primarily controlled through controls on cleanliness
  – Minimal differentiation between existing Pb-free solders, SAC and SnCu, and SnPb
  – Other Pb-free alloys may be more susceptible (e.g., SnZn)
PCB Cleanliness: Moving Forward

• Extensive effort to update PCB Cleanliness Standards
• IPC-5702: Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (2007)
• IPC-5703: Guidelines for Printed Board Fabricators in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (Draft)
• IPC-5704: Cleanliness Requirements for Unpopulated Printed Boards (2010)
Nominal Ionic Levels

• Bare printed circuit boards (PCBs)
  – Chloride: 0.2 to 1 µg/inch$^2$ (average of 0.5 to 1)
  – Bromide: 1.0 to 5 µg/inch$^2$ (average of 3 to 4)

• Assembled board (PCBA)
  – Chloride: 0.2 to 1 µg/inch$^2$ (average of 0.5 to 1)
  – Bromide: 2.5 to 7 µg/inch$^2$ (average of 5 to 7)
  – Weak organic acids: 50 to 150 µg/inch$^2$ (average of 120)

• Higher levels
  – Corrosion/ECM issues at levels above 2 (typically 5 to 10)
  – Corrosion/ECM issues at levels above 10 (typically 15 to 25)
  – Corrosion/ECM issues at levels above 200 (typically 400)

• General rule
  – Dependent upon board materials and complexity
Control Cleanliness Concerns

• Incoming PCB Cleanliness
  – Cleanliness testing performed using ROSE (resistivity of solvent extracted) or Omega-Meter method (ionic cleanliness, NaCl equivalent)

• Consider cleanliness requirements in terms of IC (ion chromatography) test for PCBs using WS flux
  – Don’t use ROSE or Omegameter test as single option (at all? Risk from dirty IPA)
  – Inspection method with accept/reject limit
  – Sampling criteria

• Control cleanliness throughout the process from start to finish.
BTC, CSP & Low Profile Cleanliness Issues (Bottom Termination Components, Chip Scale Components)

• Low or no standoff parts are particularly vulnerable to cleanliness / residual flux problems
  – Difficult to clean under
  – Short paths from lead to lead or lead to via
  – Can result in leakage resistance, shorts, corrosion, electrochemical migration, dendritic growth
Recommendations – Process Qualification

• Validate compatibility of all new process materials using SIR testing.
• Continue spot check testing of cleanliness using ion chromatography under low profile SMT parts.
PCB Sourcing & Supply Chain Best Practices
PCBs as Critical Components

• PCBs should be considered critical components or a critical commodity.
• Without stringent controls in place for PCB supplier selection, qualification, and management, long term product quality and reliability is simply not achievable.
• This section will cover some common best practices and recommendations for management of your PCB suppliers.
PCB Best Practices: Commodity Team

- Existence of a PCB Commodity Team with at least one representative from each of the following areas:
  - Design
  - Manufacturing
  - Purchasing
  - Quality/Reliability
- The team should meet on a monthly basis
  - Discuss new products and technology requirements in the development pipeline.
- Pricing, delivery, & quality performance issues with approved PCB suppliers should also be reviewed.
- The team also identifies new suppliers and creates supplier selection and monitoring criteria.
PCB Best Practices: Selection Criteria

• Established PCB supplier selection criteria in place. The criteria should be unique to your business, but some generally used criteria are:
  – Time in business
  – Revenue
  – Growth
  – Employee Turnover
  – Training Program
  – Certified to the standards you require (IPC, MIL-SPEC, ISO, etc.)
  – Capable of producing the technology you need as part of their mainstream capabilities (don’t exist in their process “niches” where they claim capability but have less than ~ 15% of their volume built there.)
  – Have quality and problem solving methodologies in place
  – Have a technology roadmap
  – Have a continuous improvement program in place
PCB Best Practices: Qualification Criteria

- Rigorous qualification criteria including:
  - On site visits by someone knowledgeable in PCB fabrication techniques.
    - An onsite visit to the facility which will produce your PCBs is vital.
      - The site visit is your best opportunity to review process controls, quality monitoring and analytical techniques, storage and handling practices and conformance to generally acceptable manufacturing practices.
      - It is also the best way to meet and establish relationships with the people responsible for manufacturing your product.
  - Sample builds of an actual part you will produce which are evaluated by the PCB supplier
    - Also independently evaluated by you or a representative
    - To the standards that you require.
PCB Best Practices: Supplier Tiering

• Use supplier tiering (Low, Middle, High) strategies if you have a diverse product line with products that range from simpler to complex.
  – This allows for strategic tailoring to save cost and to maximize supplier quality to your product design. Match supplier qualifications to the complexity of your product. Typical criteria for tiering suppliers include:
    • Finest line width
    • Finest conductor spacing,
    • Smallest drilled hole and via size
    • Impedance control requirement
    • Specialty laminate needed (Rogers, flex, mixed)
    • Use of HDI, micro vias, blind or buried vias.

• Minimize use of suppliers who have to outsource critical areas of construction. Again, do not exist in the margins of their process capabilities.
PCB Best Practices: Relationships

- Relationship Management. Ideally, you choose a strategy that allows you to partner with your PCB suppliers for success. This is especially critical if you have low volumes, low spend, or high technology and reliability requirements for your PCBs. Some good practices include:
  - Monthly conference calls with your PCB commodity team and each PCB supplier. The PCB supplier team should have members equivalent to your team members.
  - QBRs (quarterly business reviews) which review spend, quality, and performance metrics, and also include “state of the business updates” which address any known changes like factory expansion, move, or relocation, critical staffing changes, new equipment/capability installation etc.
    - The sharing is done from both sides with you sharing any data which you think would help strengthen the business relationship – business growth, new product and quoting opportunities, etc. At least twice per year, the QBRs should be joint onsite meetings which alternate between your site and the supplier factory site. The factory supplier site QBR visit can double as the annual on site visit and audit that you perform.
  - Semi-Annual “Lunch and Learns” or technical presentations performed onsite at your facility by your supplier. All suppliers perform education and outreach on their processes and capabilities. They can educate your technical community on PCB design for manufacturing, quality, reliability, and low cost factors. They can also educate your technical community on pitfalls, defects, and newly available technology. This is usually performed free of charge to you. They’ll often pay for lunch for attendees as well in order to encourage attendance.
PCB Best Practices: Supplier Scorecards

- Supplier Scorecards are in place and performed quarterly and yearly on a rolling basis. Typical metrics include:
  - On Time Delivery
  - PPM Defect Rates
  - Communication – speed, accuracy, channels, responsiveness to quotes
  - Quality Excursions / Root Cause Corrective Action Process Resolution
  - SCARs (Supplier Corrective Action Requests) Reporting
  - Discussion of any recalls, notifications, scrap events exceeding a certain dollar amount
PCB Best Practices: Cont. Quality Monitoring

• Continuous Quality Monitoring is in place. Consider requiring and reviewing the following:
  – Top 3 PCB factory defects monitoring and reporting
  – Process control and improvement plans for the top 3 defects
  – Yield and scrap reporting for your products
  – Feedback on issues facing the industry
  – Reliability testing performed (HATS, IST, solder float, etc.)


• Your PCB suppliers may be part of this activity already. Ask if they participate and if you can get a copy of their results.
PCB Best Practices: Prototype Development

- **Prototype Development**
  - Ideally, all of your PCBs for a given product should come from the same factory from start to finish – prototype (feasibility), pre-release production (testability & reliability), to released production (manufacturability).
  - Each factory move introduces an element of risk
    - Product must go through setup and optimization specific to the factory and equipment contained there.
  - All PCBs intended for quality and reliability testing should come from the actual PCB production facility.
Summary

• To avoid design mistakes, be aware that functionality is just the beginning

• Be aware of industry best practices

• Maximize knowledge of your design as early in the product development process as possible

• Practice design for excellence (DfX)
  – Design for manufacturability
  – Design for sourcing
  – Design for reliability
Conclusion

• Design for Reliability is a valuable process for lowering cost, reducing time-to-market, and improving customer satisfaction

• PoF is a powerful tool that can leverage the value of DfR activities

• Successful DfR / PoF implementation requires the right combination of personnel and tools and time limitations
Partner for Reliability, Quality and Validation

DfR – Design for Reliability –
focus on production processes

Dr. Viktor Tiederle
Instructor Biography

• Dr. Viktor Tiederle has over 29 years of experience in interconnection technology for microelectronic devices. He has worked in nearly all areas from development to production with the emphasis on quality and reliability. He started with his work in thick film technology and soldering techniques in SMD ceramics in the early 1980’s. Later we worked in wire bonding technique as well as in adhesive technology and developing micromechanical devices for automotive applications. Since more than 10 years he is responsible for many projects within the automotive as well as other industrial segments, for example in photovoltaic.

• Viktor earned his Diploma of Physics at the Technical University of Munich and Stuttgart. After some years of industrial work he received his Dr.-Ing. degree with a studying Design of Experiments used for wire bonding technique in several applications.

• Viktor works in several working groups in the automotive industry for qualifying components for the use in such hazard environments.
Reliability in production processes – Content

- 0 – Frame conditions
- 1 – Establishing processes
- 2 – Design of experiments
- 3 – Monitoring
  - Capability
  - Design Index
  - Outlier
Reliable mass production – How?!

Definition of processes

1. Selection
   - Process known?
   - Sensitive variables known?
   - Running with optimum parameters?

2. Introduction
   - Capability study done?
     - Machine cmk
     - Process cpk
     - Design Index DI

3. Verification
   - Monitoring established?
     - Watching cpk
     - Outlier detection

4. Production

Investigation with DoE
Reliable mass production

Target
- High quality and high reliability
- During total production time
- Reaching low level of rejects during production and operation
- Successful start up of production processes

Procedure
Step 1: Design of Experiments (DoE[1])
Step 3: Detecting potential field failures

[1] SPC: statistical process control
[3] DI: Design index
Reliable mass production

Introduction of processes
Key questions
- How can the process be optimized?
- What are the key parameters?
- Which parameters should we use for SPC\(^1\)?
- Are there any unknown parameters?
- What happens if quality in materials and components are changing?

Recommendation: Running design of experiments (DoE)

Constrains
- Well established processes running with long time experience
- Time frame need for rapid start of production
- Very complex approach mostly not possible with “EXCEL” approach

\[1\] SPC: statistical process control
Step 1 / Abstract description of a process

\[ Z_j = f(E_i) + g(S_i) \]

Product process

Parameter (input factor) \( E_i \)

Result (Target parameter) \( Z_j \)

Goal: description of process knowing the best variable for optimization despite of disturbing and missing parameters

i: input
j: output
Step 1 / Task (example for 1 dimension)

![Graph showing different types of dependence between a factor and a value.]

- **Factor [units]**
- **Value [units]**

**Measured value**
- Statistical spread

**No dependence**

- Linear negative dependence
- Linear positive dependence
- Quadratic dependence
Step 1 / Procedure

- Process to be investigated?
- Parameters (factors which are to be varied)
- Limits (go to edge of the process)
- Experimental plan (using algorithms to reduce quantity of parameters)
- Performing the experiment
- Calculation of results
  - Dependence of parameters
  - Results for optimized parameters
  - Prediction

Example
- Reflow soldering process
- Parameters:
  - Reflow Oven Atmosphere Profile
  - Solder paste Type Delivery
  - Mask type
- Given from running process (only for this example)
Step 1 / Example for use in process optimization

- Task: Introduction of new solder paste in PCB assembly process

- Parameters: Reflow Oven, Atmosphere, Profile, Solder paste Type, Delivery, Mask type

- Limits and Experimental plan

<table>
<thead>
<tr>
<th>Oven</th>
<th>Solder paste</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Oven</td>
<td>Profile</td>
<td>Type</td>
<td>delivery</td>
<td>Mask type</td>
</tr>
<tr>
<td>Jun</td>
<td>Normal</td>
<td>old</td>
<td>A</td>
<td>glass</td>
</tr>
<tr>
<td>Jul</td>
<td>Normal</td>
<td>new</td>
<td>A</td>
<td>glass</td>
</tr>
<tr>
<td>Aug</td>
<td>Normal</td>
<td>new</td>
<td>B</td>
<td>glass</td>
</tr>
<tr>
<td>Sep</td>
<td>Normal</td>
<td>new</td>
<td>B</td>
<td>cartridge</td>
</tr>
<tr>
<td>Okt</td>
<td>Nitrogen</td>
<td>new</td>
<td>B</td>
<td>glass</td>
</tr>
<tr>
<td>Nov</td>
<td>Nitrogen</td>
<td>new</td>
<td>B</td>
<td>glass</td>
</tr>
</tbody>
</table>
Step 1 / Example for use in process optimization

- Results

![Graph showing failure [ppm per solder joint] from Jun to Nov. The graph indicates trends for different types of solder joint failures, including tombstone, solder bridge, not soldered, Total solder failure, and other failure. The graph shows peaks and troughs for each category, with a question mark indicating a reason for the variations.]
Step 1 / Dependence for tombstone

Pareto Graph for Mulreg SOLDERPASTE_MR, Model TOMBSTONE
Main Effects on Response TOMBSTONE

Factors

LI: "glass" to "cartridge" 21
L: "B" to "A" 18
P: "new" to "old" 17
O: Nitrogen to normal 4

Estimated Main Effects

Additional information:

Data not complete
Model contains not all input factors
Step 1 / Dependence for solder bridge

Additional information:

Model describes the data nearly complete
that means: there are no other input factors
Step 1 / optimization and prediction

- **Optimized**
  - Parameter Delivery: glass
  - Mask type: small
  - Profile: new

- Prediction separately for both types of solder paste

<table>
<thead>
<tr>
<th>Solder paste</th>
<th>Nitrogen</th>
<th>Normal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>29 ppm equals 3.8% PCB failure</td>
<td>43 ppm</td>
</tr>
<tr>
<td>B</td>
<td>11 ppm equals 1.4% PCB failure</td>
<td>25 ppm</td>
</tr>
</tbody>
</table>
Reliable mass production – How?!

Definition of processes

- Selection
- Introduction
- Verification
- Production

Step 2

Capability study done?
- Machine cmk
- Process cpk
- Design Index DI
Step 2 / Definition capability & design index

Capability Index

Assumption upper limit closer

\[ C_{pk} = \left( \frac{USL - \bar{x}}{3s} \right) > 1.66 \]

\[ DI = \left( \frac{USL - M}{B - M} \right) > 1 \]

- \( C_{pk} \): Capability index
- \( \bar{x} \): Mean value
- \( USL \): Upper specification limit
- \( s \): Standard deviation
- \( DI \): Design index
- \( M \): Mean value – single test
- \( A \): Min (\( x_{mi} + x_{iCL} + 3s \))
- \( B \): Max (\( x_{mi} + x_{iCL} + 3s \))
- \( USL \): Upper specification limit
- \( x_{iCL} \): Confidence range of mean

\[ M = \frac{1}{2} (A + B) \]
Step 2 / Example capability & design index

- Measurement at RT
- Different results at LT and HT

- \( C_{LT} = 2.27 \)
- \( C_{RT} = 2.23 \)
  \( DI = 1.39 \)
- \( C_{HT} = 2.45 \)
Step 2 / Example design index

- Variation
  - Temperature
  - Voltage
- Within the limits
- DI = 1.59

- Variation
  - Temperature
  - Voltage
- Partly outside of limits
- DI = 0.82
Reliable mass production – How?!

Definition of processes

Selection → Introduction → Verification → Production

Step 3

Monitoring established?
Watching cpk
Outlier detection
Step 3 / Identification potential field failure

- **Method**
  - Failures in the field are products with „not normal“ behavior
  - „Normal“ behavior: measurement with normal distribution
  - Measurements outside the normal distribution ➔ potential failures

- **Task**
  - Search for outliers

- **Procedure**
  - Using data of testing within production (e.g. in-circuit test)
  - Statistical calculation using the data
  - Verification (checked by developing specialist)
  - Repair / scrap
Step 3 - Task

Judgment using standard data from mass production

- Distribution process, product
- Drift behavior product
- Identification of not normal properties product

A) suspicious, but within distribution (2 & 1 value)
B) suspicious, outside of distribution ➔ outlier

Legend:
- Spec-max
- PAT / max
- Worst Case / max
- Worst Case / min
- PAT / min
- Spec-min
- Gauss
- DDJ
Step 3 / Procedure

- Collecting data (from test, process, . . . .)
- Statistical calculation
  - robust mean
  - robust standard deviation

\[
\bar{x}_{rob} = Median(Daten)
\]

\[
\sigma_{rob} = \left(\frac{Q3 - Q1}{1,35}\right)^{61}
\]

\[
Q1 = Quartile(Daten; 1)
\]

\[
Q3 = Quartile(Daten; 3)
\]

- Identification of outlier
- Investigation of identified products
- During start-up better results with additional measurements at limits of temperature
Step 3 – Robust mean / example

Data

<table>
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<tr>
<th>Bauelement</th>
<th>Parameter</th>
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</tr>
</tbody>
</table>

Calculation with “robust” algorithm

Calculation with “arithmetic” algorithm
Step 3 – Example / Outlier

- Measurements with normal distribution (approximately)
- 2 measurements outside of calculated limits
- Special investigation necessary: high potential of failure?
  No delivery!
Step 3 – Example / local – global aspect of calculation

- Outlier not detectable with global approach
- Reason: Variation of different lots?
Step 3 – Strange behavior

- Reason: measurement at limit of resolution (quantification)
- Outlier
Step 3 – Identification potential field failure / example

- All measurements within specification limits
- Capability index okay (2,11)
- 3 „not normal“ values
Conclusion

- Reliability is one of the key issues now and in the future

- Established tool are to improved to fulfill the further needs

- Knowledge of processes is the basis to have reliable products

- Existing data should be used more to improve the processes
  (as shown to detect outliers)
Contact information

Key Facts

- Founded in 2005 in College Park, MD
- 20+ Employees
  - Multiple US locations
- Offerings
  - Research, Lab Services, Consulting, Software
- 300+ customers, including:
  - Dell, HP, Apple, Microsoft, IBM, Ericsson, Cisco Systems, Verizon, Huawei, Polycom, AMD, and Nvidia

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