Reliability Modeling of Electronics for Co-Designed System Applications
Agenda

• Introduction
• High Reliability Applications
• Common Issues
• Lifetime Expectations
• Failure Mechanisms
• Virtual Qualification Approach
• Automated Design Analysis Solution
High Reliability Systems are Prevalent in Several Market Segments

- Switching Power Supply
- Solar Power Modules
- Automotive Power Modules
- IGBT
- Thermoelectric Modules
- Street Lighting
What Do they All Have in Common?

• High Temperature Environments
• Possible Vibration and Shock Environments
• Temperature and Power Cycling Environments
• Very High Current Flows and Thermal Transfer Requirements
• A variety of materials forming the product
  – Substrate tiles bonded to copper baseplate
Stringent Environmental Conditions

- Being used at varying temperatures or temperature extremes
- Having a temperature range of -55°C to 125°C
- Being used in an application having a medium to high shock, pressure, vibration, or moisture environment
- Being stored for later usage (over 10 years)
- Having an application life span of 10 to 25 years
Example Life Expectancies

• IGBT – Rail application – 30 years (Each module 100FIT)
• Power Module – Automotive Application – 20 years
  – 10W/cm²
  – DBC Substrate bonded to heatsink
  – Vibration, shock, humidity, salt spray
  – Cost
• Solar Power Inverters-25 years
• Street Lighting – 15-20 years
Failure Mechanisms

- Thermo-mechanical fatigue induced failures
  - CTE mismatch
  - Temperature swings
- Bond Wire Fatigue
  - Shear Stresses between bond pad and wire
  - Repeated flexure of the wire
  - Lift off (fast temperature cycling effect)
  - Heel Cracking
- Die Attach Fatigue
- Solder Fatigue
  - Voids
- Device Burn Out
- Automotive- degradation of power
  - Solder Fatigue
  - Bond wire failure (lift off due to fast temperature cycling)
- Structural Integrity – ceramic substrate to heat sink in thermal cycling
- IGBTs – solder joint fatigue, wirebond liftoff, substrate fracture, conductor delamination
How Can We Resolve these Issues During the Design Phase of a Product?

• Utilize an Automated Design Analysis Approach Because:
  – Mil-HBK-217 actuarial in nature
  – Physics based algorithms are too time consuming
  – Need to shorten NPI cycles and reduce costs
  – Increased computing power
  – Better way to communicate
PoF: the Complexity Roadblock

\[ \tau_{HCI} \propto \exp\left(\frac{b_{HCI}}{V_D}\right) \cdot \exp\left(\frac{E_{aHCI}}{kT}\right) \]

\[ T_f \propto \exp\left(\frac{-0.51eV}{kT}\right) \times \exp(-0.063%RH) \]

\[ N_t^{-0.6}D_t^{0.75} + 0.9 \frac{S_a}{E} \left[ \frac{\exp(D_t)}{0.36} \right]^{0.1785 \log_{10}\frac{10^3}{N_t}} - \Delta \varepsilon = 0 \]

\[ \tau_{TDDB} \propto \exp[-b_{TDDB} \cdot V_G] \cdot \exp\left[\frac{E_{aTDDB}}{kT}\right] \]

\[ \frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{K_B} \left(\frac{1}{T_1} \cdot \frac{1}{T_2}\right) \]

\[ \tau_{NBTL} \propto \exp[-b_{NBTL} \cdot V_G] \cdot \exp\left[\frac{E_{aNBTL}}{kT}\right] \]

\[ (\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left( \frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A G_s} + \frac{h_c}{A G_c} + \left( \frac{2 - \nu}{9 \cdot G_b a} \right) \right) \]
Common Failure Modes

• Wire Bonds

Wire bonding has been the most common interconnect for IC packages for over 50 years. The most common materials are gold, aluminum, and more recently copper. The most common bond pad material is aluminum.

Wire bonds tend to fail if exposed to elevated temperatures (intermetallic formation), exposure to elevated temperature and humidity (corrosion) and exposure to temperature cycling (low cycle fatigue).
Common Failure Modes: PCBs

- Printed Wiring Boards have several failure modes that are detrimental to reliable operation. Failures in PCBs can be driven by:
  - Size (larger boards tend to experience higher temperatures)
  - Thickness (thicker boards experience more thermal stress)
  - Material (lower Tg tends to be more susceptible)
  - Design (higher density, higher aspect ratios)
  - Number of reflow exposures
Common Failure Modes: PCBs

Conductive anodic filament (CAF), also referred to as metallic electromigration, is an electrochemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field. CAF can cause current leakage, intermittent electrical shorts and dielectric breakdown between conductors in printed wiring boards.

Plated Through Hole Failure Mechanisms: voids (left), etch pits (center) and barrel cracking from fatigue (right)

PTH voids can cause large stress concentrations, resulting in crack initiation.

Etch pits are due to either insufficient tin resist deposition or improper outer-layer etching process and rework.

Overstress cracking can occur in the PTH due to a Coefficient of Thermal Expansion (CTE) mismatch which places the PTH in compression.
Common Failure Modes: Solder Fatigue

- Thermo-Mechanical Fatigue of solder joints is one of the primary wear-out mechanisms in electronic products. This is especially true in products used outside of commercial/consumer environments where a longer lifetime is required and more severe operating conditions exist. The analysis assesses the fatigue of the solder joints as a function of the stresses applied during its lifetime and provides insight into whether joints are susceptible to failure.
Automated Design Analysis

- Easy to Utilize
- Easy to Locate commands
- Industry Terminology
  - Parts List
  - Stack-up
  - Pick and Place
  - ODB++
  - GERBER

There are several high levels steps involved in performing an automated design analysis. They are:
- Define Reliability Goals
- Define Environments
- Add Circuit Cards
- Import Files
- Generate Inputs
- Perform Analysis
- Interpret Results
Reliability Goals
Ambient Environment

Handles Very Complex Environments
Input Design Files
Input: Parts List

- Color coding of data origin
- Minimizes data entry through intelligent parsing and embedded package and materials database
Inputs: Stack-Up

- Automatically generates stackup and copper percent (%)
- Embedded database with almost 400 laminate materials with 48 different properties
• Eight different analyses can be performed. They are:

  – CAF – Conductive Anodic Filament Formation
  – Plated Through Hole Fatigue
  – Solder Joint Fatigue
  – Finite Element Simulations
  – ICT Impact
  – DFMEA
  – Vibration Fatigue - Natural Frequencies
  – Mechanical Shock
Results: Automated Mesh Generation

- Identifies optimum mesh density based on board size
- Expert user no longer required; model time reduced by 90%
3D Output

The analysis can also establish 3D models by creating a mesh structure and the model from the data input to the analysis.
In-Circuit Test Evaluation

- Uses embedded FEA engine to compute board deflection and strain cause by ICT fixture
- Uses ODB++ data including net list to create board level DFMEA
- Includes customizable spreadsheets for export
Results: Five Different Outputs
Natural Frequencies

Natural Frequencies Identified (1\textsuperscript{st}-upper left), (2\textsuperscript{nd}-upper right), (3\textsuperscript{rd} -lower left) and 4\textsuperscript{th} – lower right)
In addition, the analysis can provide data regarding the strains applied to the circuit board as a function of the vibration stress levels. The left illustrates this data in the XX direction and YY in the right image.
Comparison of Sn/Pb (left) and SAC305 (right) with respect to solder fatigue
Product Test Plans

- Product test plans, also known as design verification, product qualification, and accelerated life testing (though, these are not the same thing), are critical to the successful launch of a new product or new technology into the marketplace.
- These test plans require sufficient stresses to bring out real design deficiencies or defects, but not excessive levels that induce non-representative product failure.
- Tests must be rapid enough to meet tight schedules, but not so accelerated as to produce excessive stresses.
- Every test must provide value and must demonstrate correlation to the eventual use environment (which includes screening, storage, transportation/shipping, installation, and operation).
Thank You!

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