Understanding and Mitigating EOS/ESD in Electronics

Conference on Best Practices in Electronics Design and Manufacturing

Date: March 9, 2016
What is ESD?

- Electrostatic Discharge, or ESD, is a single-event, rapid transfer of electrostatic charge between two objects, usually resulting when two objects at different electric potentials come into direct contact with each other.

- ESD can also occur when a high electrostatic field develops between two objects in close proximity.

- ESD is one of the major causes of device failures in the semiconductor industry.
ESD Models

- There are three (3) predominant ESD models for integrated circuits (ICs):
  1) the Human Body Model (HBM)
  2) the Charged Device Model (CDM)
  3) the Machine Model (MM)
ESD Models

- The HBM simulates the ESD event when a person charged either to a positive or negative potential touches an IC that is at another potential.

- The CDM simulates the ESD event wherein a device charges to a certain potential, and then gets into contact with a conductive surface at a different potential.

- The MM simulates the ESD event that occurs when a part of an equipment or tool comes into contact with a device at a different potential.
  - HBM and CDM are considered to be more 'real world' models than the MM.
Design for ESD Prevention: What Do You Need to Do?

- ESD Protection is necessary at the IC, component package and system level
  - Different approaches are needed to achieve reliable protection
- Designing for ESD impacts both the product design and the manufacturing process controls
- What technologies are available to assure a reliable ESD protected product?
  - At the IC level
  - At the component package level
  - At the system level
Component Failure Mechanisms: ESD

- Objects moving with respect to each other transfer charge
  - Amount depends on materials, speed, proximity
  - Dissipation depends on conduction paths
- Extremely large voltages possible
  - Dry environment
  - Materials with easily stripped electrons
  - No discharge path
- Human perception > 5 kV
  - Circuits long since destroyed

<table>
<thead>
<tr>
<th>Event</th>
<th>Relative Humidity</th>
</tr>
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<tbody>
<tr>
<td>Walking across a vinyl floor</td>
<td>12,000</td>
</tr>
<tr>
<td>Motion of bench employee</td>
<td>6,000</td>
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<tr>
<td>Removing DIPS from a plastic tube</td>
<td>2,000</td>
</tr>
<tr>
<td>Packing PWBs in foam line box</td>
<td>21,000</td>
</tr>
</tbody>
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Voltages associated with ESD
Component Failure Mechanisms: ESD

- Two primary failure mechanisms:
  - Electric field-induced
    - Silicon dioxide breakdown $\sim 7 \times 10^8$ V/m
    - 60Å oxide destroyed at $\sim 4.2$V
    - Shorts gate permanently
    - Fields could push carriers into insulators
      - May just degrade performance
  - Thermal destruction
    - Any resistance in path subject to local intense heating
      - Contacts, vias, and junctions
      - Weakest link goes first
    - May also produce “walking wounded”
      - Increased leakage
      - Increased resistance
      - Softened junctions

- All protection techniques fail eventually
  - Class A, B, & C specifications are 1kV, 2kV, & 4kV, respectively

Typically, walking wounded devices catastrophically fail when full loads are applied.
Component Failure Mechanisms: ESD Examples

SEM of P/N junction
Source: Frank, EDFAS, 2004

SEM of metal line damage
Source: Putnam et al., EDFAS, 2004

Light emission of latchup in logic circuitry
Source: Frank, EDFAS, 2004

SEM & AFM of lateral ESD on line
Source: Colvin et al., EDFAS, 2004

SEM: HBM test on NFET
Source: Putnam et al., EDFAS, 2004

SEM of silicide shorts in SOI device
Source: Prejean et al., EDFAS, 2004
Electrostatic Discharge Failure Modes

- Different ESD modes tend to produce different types of failure
- Basic failure modes include:
  - Oxide punch-through
  - Junction burnout
  - Metallization burnout

Images courtesy of Texas Instruments
Design Practices for ESD

- Know the ESD rating for each part, and select parts (where possible) for the best ESD rating
  - Identify all ESD Sensitive Parts on drawings
  - Mark Locations of ESD Sensitive parts on the Board with the ESD symbol
- Consider the entire System (Design) as ESD Sensitive
ESD Design Practices (cont.)

- **Use ESD Protection on all susceptible parts (not just System I/Os)**
  - **Box or System I/O**
    - ESD Rating < Class 2 IEC (4000V) MANDATORY
  - **Internal Components (not exposed to outside connectors)**
    - ESD Rating <= Class 1 ANSI (0-999V) MANDATORY
    - ESD Rating < Class 2 ANSI (2000V) WHEREVER POSSIBLE

- **High Speed, RF and GaAs parts will be particularly sensitive to ESD**
  - GaAs Parts are typically rated as Class 0 (<250V) or Class 1A (<500V) – ONLY THE BEST PROTECTION DESIGN AND HANDLING PROCEDURES WILL PREVENT DAMAGE TO THESE PARTS!

- **Place ESD sensitive components and traces to avoid locations where the board may be handled**

- **Consider ESD as well as RF shielding**

- **Where possible install protective devices before ESD sensitive parts**

- **Avoid Coupled ESD events – Do not route traces to ESD sensitive parts near lines connected to the outside world**
ESD Design Practices (cont.)

- Perform Circuit analysis to insure effectiveness of ESD protection (Class 2 ANSI [2000V] for internal, IEC level 2 [4000V] for I/O)
- Test Boards and Systems for Internal and I/O ESD tolerance
- ESD Protection devices must be connected to a good ground to accommodate up to 30A ESD spikes.
  - If upset of operating circuits is to be avoided, a separate Earth ground should be used
ESD Sensitive Parts (Pin Sensitivity)

- Any pin of a discrete ESD sensitive part (FET, Transistor, etc) may need protection (if not connected to a supply)
  - **Input pins**
    - Can be sensitive since they have little or no built-in ESD protection
    - Especially on high speed devices like GaAs ICs or discretes,
  - **Pins other than inputs (on an ESD sensitive part)**
    - Can also be sensitive because an ESD pulse can affect internal voltage levels
    - Any improperly terminated or unprotected pin can be a conduit for ESD
  - **Supply pins**
    - Provide reference bias connections
    - Should not need additional protection (as long as they are connected to the power supply)
  - **Outputs of logical or functional parts designed with active (usually buffered) output stages**
    - May have clamping diode protection to the supplies and may not need additional protection – check the part ESD rating
Evaluate Potential ESD

- If ESD sensitive parts are used in design, the circuitry connected to device pins should be evaluated
  - Insure that it provides “attenuation” to prevent voltage in excess of the parts ESD rating from developing in case the pin or connected traces are contacted during board handling or system assembly.
- Often the recommended circuit components for operation of the part will provide adequate ESD protection.
  - This should be verified by analysis or simulation and extra protection added as required to limit the voltage seen at the part.
- Assumptions for analysis/simulation
  - 2000V, 1.5K Ohms, 100pf for Internal circuits
  - 4000V, 330 Ohms, 150pf for I/Os
Design for ESD Prevention: ESD IC Device Specifications

- What should you be concerned about?
  - Completely different specification methods for ESD protection of components are commonly used.
  - Designers may need to gather comparable data points from differing graphs and tables.
  - Some differentiators to look for and investigate further are outlined below.

- IEC Rating: Verify that the ESD protection device is guaranteed to meet or exceed specifications in IEC 61000-4-2.

- Contact versus Air Discharge: Verify that identical specifications are being compared. Some devices are documented with high air discharge ratings, which can be incorrectly compared with the normally lower contact discharge ratings. Contact ratings are fairly repeatable, whereas air ratings vary.

- Clamp Voltage: Choose a device with a maximum clamp voltage at a given peak current well below the level that the protected devices can tolerate. The lower, the better.

- Pulse Current: Beware of misleading approximations of peak power capacity. It can usually be improved by specifying a shorter peak duration.
ESD IC Device Specifications

- **Response Time**: Faster-acting devices reduce the width of the pulse transferred, and these devices can help attenuate the peak clamp voltage.

- **Parasitic Capacitance**: Added capacitance degrades I/O signal rise and fall times. On lower-speed signals, this stray capacitance can be lumped into or can displace the need for EMI capacitors.

- **Parasitic Inductance**: Higher impedance in the clamp path (to VDD or ground) can increase the effective system clamp voltage.

- **Multistrike Capability**: Verify that the protection designed-in can survive the expected life of the system. Resultant field failures are difficult to diagnose and can manifest themselves in unexpected functional errors, or even data loss.

- **Integration and Matching**: High-speed differential signals, such as in IEEE 1394, benefit from matched loading on the positive and negative lines of each pair. ESD protection products with multiple devices per package (such as thin-film silicon) can have intrachip device-to-device parasitic impedance matching of less than 0.1%. Unitary packages, however, may vary as much as 30% interchip matching. Printed-circuit-board (PCB) signal routing restrictions may also indicate a need for tight multidevice integration.
Many ESD design rules

Two common types of design rule verification/compliance

- Design Rule Checking (DRC): standard DRC tools with ESD marking layers
  - Example: Mentor Graphics Calibre PERC
    - Rule 1: Primary Protection for I/O Pad
      - For each net in design, IF net is connected to IO Pad THEN check for up HBM diode and down HBM diode IF diode(s) missing THEN ESD Error
    - Rule 2: Secondary Protection for I/O Pad
      - For each net in design, IF net is connected to input buffer and IO Pad THEN check for CDM up diode and CDM down diode check if CDM resistor exists and is correct value IF diode(s) missing or resistor incorrect THEN ESD Error
  - Net-oriented: in-house tools for circuit analysis.
ESD Protective Device Options

- **Passive Networks**
  - Capacitors – Simple, Low cost
  - Band-pass filters – Somewhat more complex, good ESD protection

- **For lower speed devices**
  - Schottky Diodes – Simple, but capacitance loads HF circuits
  - Diode Clamping Arrays – Good for LF circuits and outputs

- **For higher speed devices (requiring low capacitance)**
  - Low capacity protection diodes (<1 pf) – Robust, Good HF compromise
  - Polymer ESD (PESD) Protection devices (<0.25 pf)
    - Excellent HF characteristics, small size 0402, 0603
    - PESDs have limited Pulse life, good parts withstand 100 to 1000 strikes
    - Operating voltage typically 5V, available to 12V
    - Trigger Voltage 100, 150V
Simple Capacitive Protection

- Use to provide ESD protection on bypassed pins for ESD sensitive devices, or at Supply input connections
  - Make sure capacitance (C2) is significantly larger than the Human Body Model (>>150pf) to minimize developed voltage (approx. 28 times or 4000pf for protection of a Device with an ESD sensitivity of 150V)
  - May add a Resistor to bleed off charge (from C2)
  - Use 200V rated Cap (for C2)
Filters

- Band-pass filters can be used for higher frequency applications and can be effective for RF system inputs.
- Very Robust circuit with good protection.

Band-pass Filter 850-2GHz, 50 Ohm Impedance

C1, C2, C3 rated at 100V.
Protection with Clamping Diodes

Protection Diode Array (CM1213-01)

ESD Source

Protected Output

ESD at output is clamped at approximately 14V with 4000V ESD hit through 330 Ohm resistance
PESD (Polymer ESD) plus Inductor

- The Inductor shunts lower frequency energy to ground, removing stress from the PESD.
- Provides better protection than the PESD alone and extends life of the PESD
- The PESD can be used alone for wider bandwidth operation
Summary of ESD Design Guidelines

- Design ESD Protection for External (System) IOs to IEC HBM Class 2 (4000V, 150pf, 330 Ohm) Including:
  - RF or signal inputs
  - Control and System IOs that DO NOT have built in protection to the required limit

- Design ESD Protection for Internal ESD sensitive parts to meet ANSI 20.20 Class 2 (2000V)

- Know the ESD rating of every part used

- Select parts (where possible) to meet ANSI 20.20 ESD level Class 2 or better (2000V)

- Parts rated less than Class 2 should have additional protection circuitry added to protect the board during handling
ESD Design Guidelines (cont.)

- For External (System) Inputs use Robust protection:
  - Band pass filter
  - PESD plus Inductor (for Severe condition use PESD + Filter)
- For Internal ESD Sensitive pins use:
  - Single bypass Cap (where possible)
  - Filter if needed
  - PESD or PESD plus Inductor
- Any Pin of an ESD sensitive part may be at risk If It is NOT:
  - Connected to a supply plane
  - Adequately decoupled to GND (~4000pf @200V)
  - Protected by a “filter” network (simulate for an ESD hit)
- External (System) Output or IO
  - Use low capacitance Clamping diodes (1pf)
  - PESD if required for speed (.25pf)
Failure Analysis Techniques

- Returned parts failure analysis always starts with Non-Destructive Evaluation (NDE)

- Designed to obtain maximum information with minimal risk of damaging or destroying physical evidence

- Emphasize the use of simple tools first

- (Generally) non-destructive techniques:
  - Visual Inspection
  - Electrical Characterization
  - Time Domain Reflectometry (TDR)
  - Acoustic Microscopy
  - X-ray Microscopy
  - Thermal Imaging (Infra-red camera)
  - SQUID Microscopy
Failure Analysis Techniques

- Destructive evaluation techniques
  - Decapsulation
  - Plasma etching
  - Cross-sectioning
  - Thermal imaging (liquid crystal; SQUID and IR also good after decapsulation)
  - Scanning Electron Microscope & Energy Dispersive X-ray Spectroscopy (SEM/EDX)
  - Surface/depth profiling techniques: SIMS-Secondary Ion Mass Spectroscopy, Auger
  - Optical/Electron Beam Induced Current (OBIC/EBIC)
  - FIB - Focused Ion Beam
Examples of Lab Testing

- Electrostatic discharge test – Human body model
- Test method was MIL-STD-883, method 3015.8

Post stress test positive pulse waveform.
Results Electrical

Curve tracing example.

ESD damage was suspected in Part B

Part B was powered at 3.3V and output monitored with a 10K ohm load. It operated at the specified frequency (14.745M Hz) but the waveform was not a square wave as expected.

Curve tracing was done between power (pin 8), output (pin 5) and ground (pin 4). There is a slight difference in traces for the output signal between Part A and Part B.
Trying to distinguish between EOS & ESD

- Often difficult to distinguish between EOS/EOL (electrical overstress and electrical overload) and ESD. Some rules of thumb:
  - ESD damage
    - Small failure sites
    - Not always visible without deprocessing
    - No visible evidence at the package level
  - EOS damage
    - Large areas of damage
    - Burned silicon and metallization
    - Sometime visibly evident package damage
Trying to distinguish between EOS & ESD

- **EOS: Thermal overstress to a component’s circuitry**
  - Short Pulse Width Failure – Junction Spiking
  - Long Pulse Width Failures – Melted metallization and open bond wires
  - Junction spiking occurs when the amount of Al migration into the silicon substrate has reached the point wherein the Al has penetrated deep enough so as to short a p-n junction in its path. By that time an Al spike is said to have shorted the junction, damaging the device permanently.
Sometimes ICs are protected on the input, but not necessarily on the load side. Here we see how a walking wounded device fails after a load is applied.

If this was subjected to a electrical overstress event, then the vertical structure diode would have failed across its entire surface area.
ESD Failures: Latent Failures

Latent Failures

- ESD events not only impact assembly yields, but also can produce device damage that escapes testing and causes latent failures in the field.
- Devices with latent ESD defects have been referred to as “walking wounded” because they are degraded but still function.
- Latent damage can occur when an ESD event is not sufficiently strong to destroy a device:
  - Device continues to function and is still within data-sheet limits
  - Device can be subjected to numerous weak ESD events, with each new event further degrading a device until total failure
  - No known practical way to screen for walking wounded devices
  - Damage to insulators: weakening of the insulator structures, leading to accelerated breakdown and/or increased leakage
  - Damage to junctions: lowering the lifetime of minority carriers with consequent bipolar transistor gain loss; increasing resistance in forward biased state; increasing leakage in reverse biased state
  - Damage to metallization: weakening of the conductor, leading to increased resistance or increased rate of electromigration
Discussion – Physics Behind ESD

- When silicon is heated, the electrical carriers normally present in the device are supplemented by thermally generated carriers. This causes the resistivity of silicon to decrease sharply with an increase in temperature. This is known as Runyan’s curve.

- This conductor shorting phenomenon allows some conclusions about the thermo-mechanical behavior of silicon to be reached.
  - When energy is suddenly dumped into a silicon device in the form of an impulse, the heating of the silicon is inherently uneven.
  - A small area of the junction will absorb current and heat up, causing its resistivity to drop sharply. This small area is sometimes addressed as a resistive filament.
  - Once heating is taking place, the small area becomes effectively thermally isolated from its surroundings because the thermal conductivity of the silicon decreases.
  - This effect is a positive feedback mechanism known as secondary breakdown resulting in damage to the device known variously as a punch-through or melt-through.
Discussion – Duration of ESD

- The duration of an ESD event ranges from less than one nanosecond to one millisecond and longer.
  - Long events can lead to damaged areas such as blown metal lines, cavities in the silicon, or discoloration of silicon due to local heating with a characteristic radius of 100um or greater.
  - Long events lead to either a reduction in IC performance (e.g., increased leakage current on one or more pins) or total circuit failure.
- Surface breakdown generally occurs when the rise time of the pulse is short enough to break down the junction, usually just beneath the oxide, before secondary breakdown (closed loop thermal fusing) can occur.
  - Surface breakdown can also occur when the voltage is high enough to bridge a gap between two metal lines, on the device surface. This is called gaseous arc breakdown.
- Time duration for typical failure modes:
  - < 10 nanoseconds to 1 microsecond causes melting of thin metallization and polysilicon
  - > 50 microseconds to 100 microseconds causes junction punch through
  - > 100 microseconds causes melted metal and fused wires
Thanks!

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EPI Sensing Polymer Devices for ESD

Presented at DfR Solutions
March 9th 2016
Outline

• Introduction to EPI
• EPI Polymer Devices
• TVS Characterization
• High Speed Requirements
• Zener TVS versus EPI Diode
• EPI Application Examples
• Summary
LINTEC OF AMERICA specializes in proprietary semiconductor manufacturing related products, called Adwill. These include a wide array of product lines featuring high-function adhesive tapes such as Non UV and UV dicing tape, BG surface protective tape, and die attach specialty films. Lintec is also the industry leader in Wafer Mounting Systems and UV Irradiation Systems.

Lintec with it’s 110 man global sales organization will be representing Electronic Polymers as a new addition to their highly qualified product line. EPI will be benefiting from the extensive customer base Lintec has cultivated over a 30 year period.
Competitive Advantages

• Extremely low capacitance – typically 50 fF
• No signal interference up to 100 Ghz
• Linear device with no harmonics for antenna applications
• Z-height < 150 um
• Gold plate electrodes
• Design flexibility – electrodes on top/bottom layers and allows between board and component placement
• Tester provides parameters enabling design cycle reduction from months to days
Implementing for ESD Protection

EPI’s holistic approach to protect the system.
First line of defense: Connector array
second line of defense: strategically placed on-board protectors in DFN1006 and DFN0603 (metric)
third line of defense: Interposer to protect specific devices right at the silicon level.
EPI offers an innovative strategy to protect sensitive silicon chips and relieves silicon designers from the burden of sacrificing extremely expensive silicon real-estate needed for on-chip system level ESD protection. EPI can add an ultra thin (down to 80um) interposer to protect all IO pins on the silicon during assembly and life time system ESD events.
Multi-chip Interposer

Advantages:
Customer advantages:
- use lowest cost options
- optimize chip technology for function not for protection
- Use of ball grid array or plated pads

EPI advantages
- EPI advanced interposer substrates (50-100um thickness)
- EPI added system level performance (15-30kV IEC contact)

Example: Customers IC’s + EPI Interposer

An interposer to allow a very small footprint C-Type USB3.1 connector array. The customer just has to place his existing IC’s on top of the interposer.
Wafer-level TLP Characterization

Hardware designed for wafer level TLP testing

✓ Rack mounted testing system
✓ Integrate-able into standard e-test software (GPIB)
✓ Produces key statistics, and SPICE device parameters
✓ Can use same system on packages and Post package testing

Wafer Level Testing Value

✓ Enables large data sets for I/O Protection
✓ Enables fast characterization of I/O protection designs to generate true design rules and hardened designs
✓ Enables an entire library of I/O ESD protection to meet specific market needs - No need to over design.
✓ Utilized in Ongoing reliability monitoring and production monitoring with scribe line structures
EPI Protection Test Equipment

Test Equipment:
Aid to select the right Protection Concept

Ultra Fast TLP: HMM specification
Extreme high power: 90A

Unique Intelligent Software:
- easy extraction of key parameters
- for protection devices
- for components and whole system

EPI offers test equipment to customers who want to characterize their systems.
With the extraction of key parameters it enables the board designer to pick exactly the right protection devices and to predict ESD performance.
Electrostatic Discharge (ESD)

**Component Level ESD**

- Human Body Model (HBM): *ANSI ESDA/JEDEC JS-001*
- Charged device model (CDM):
  - **JESD 22-C101C**

**System Level ESD**

- **IEC 61000-4-2**
- **ISO 10605** (automotive)
- Cable discharge events (**CDE**) (company specific test specs)

Industry Council 2015
ESD Testing Models – System Level ESD
International Electro-technical Commission (IEC)

CDM-like

HBM-like

Equivalent Circuit

$V_{\text{IEC}}$

8 kV

330 Ω

150 pF

DUT

Time (ns)

IIEC (A)
Waveforms of Component HBM and System Level

- System level ESD gun test has to be performed under powered conditions
- For powered systems there are two failure mechanisms
  - Destructive fail
  - Functional/Operational fail
- Improving the component ESD levels will not solve this issue
- There is no clear correlation of system level performance to the HBM robustness

4 kV HBM is not the same as 4 kV System Level IEC!

Note the extreme initial I(peak) due to the direct capacitive coupling with the gun tip

Industry Council 2013
Excursion: ESD Device Characterization

Device characterization by **Transmission Line Pulser (TLP)**

- HV source
- MOhms transmission line (e.g. 5m)
- switch
- DUT
- Voltage probe
- Current probe

**Graphical representation:**
- Voltage [V] vs. time [ns]
- Current [A] vs. voltage [V]
- I-V data point
- Vhold
- Vt1
- Vt2
- It1
- It2

H. Gossner
High Current TLP

Trigger at 4 Volts and Holding at 3 Volts

On-resistance = 10 V / 8 A = 1.25 Ohms

Passed TLP > 7 Amps or equivalent to IEC at 4 kV

Duvvury 2013
Comparison of Different Stress Events

- 2kV HBM
- 8kV IEC
- 500V CDM

System Level ESD
Cable Discharge
Electrical Overstress (EOS)

Time: 0 ns to 1 ms
Current: 0 A to 30 A
Voltage: 500 V to 8 kV
ESD Protection Review

Human Body Model (HBM) Charged Device Model CDM

Chip Level Protection: typically 2KV HBM and 500 VCDM

- Constantly evaluated and tested on each new technology or modification to
- Requires constant evaluation and characterization
- Consumes large amount of area for each I/O on chip

IEC System Level Testing

- Completed system: Typical 8KV/15KV requirement
- Very Critical for Mobile and battery based systems
- Chip and system level dependent
- Requires External Protection on Devices
- On-chip devices can be done but not a good strategy
ESD Characterization with TLP

Current and Time domain testing methodology for evaluation of Electrostatic discharge robustness.

Simple idea - Charges a cable then releases pulse onto the device under test.

Difficult to Implement - Require precise control to predict ESD protection

Industry standard for ESD characterization and evaluations

System is typically dedicated hardware

Requires either standard packaged devices or expensive sockets for unique packaged

Only delivers limited capacity, since lab based
What is a System?

A system consists of embedded ICs and other electronic components to form a consumer/automotive/military/medical product that can be exposed to various random uncontrolled severe ESD events with unspecified waveforms.
What is a System Event?

An ESD event enters a system: it can be coupled directly into a port on any signal, power or ground line, induced into circuit paths from currents flowing on a chassis surface, or radiated into a product.

ESD currents flowing on printed circuit track, through ground or power plane will cause E and H fields to be developed and unwanted voltages to be generated.
Differentiation of Internal Vs. External Pins

Other types of pins, including **Inter-chip**, and the effects of **Cross-Talk** have to be considered.

Industry Council 2015
Impact from On-Chip System ESD Design

On-Chip Solution

ESD and EMI spread into the system creating secondary issues

Off-Chip Strategy

ESD and EMI are guided out of the system keeping noise isolated
System Efficient ESD Design

The design of overall system protection requires understanding of the “Residual Pulse” going into the IC pin with external interface.
What are the problems for an On-Chip System Protection Strategy?

• Misconception
  • Is necessarily a cheaper solution than off-chip design
  • A single IC can cover protection for the whole system
• Added IC level costs
  • ~30% increase in area
  • Need for a larger package
  • Increased design cycle time
• Uncertainty
  • No information on other components on the board
  • How the test would be done
  • To design for surviving the worst-case IEC stress
  • additional system protection measures may be needed
What is an ideal approach?

• **External Protection Choices**
  • Transient Voltage Suppressor (TVS) like a Zener Diode
  • Polymer Integration

• **Zener**
  • Readily available as a component
  • Placed on the Printed Circuit Board (PCB)
  • Effective but voltage buildup at higher current levels
  • Adds extra capacitance

• **Polymer**
  • Can be integrated into the IC package
  • No additional area on the PCB
  • Fast trigger and offers lower capacitance
  • Currently very useful for GaAs, DLP, and other products with 100-300V applications
IEC Protection

Zener Diode is a voltage limiting protection device

R. Ashton
Voltage Limiting

How fast does it turn on?
Has to be faster than the IEC pulse rise time
Faster the better

Where does it hold?
The lower the better
Lower on-resistance makes it more efficient

Voltage

Current

Snapback

Voltage Clamping
MOV and Polymer TVS
And some Silicon Based Devices

Wireless and Power Line Communication

Silicon TVS
And Zener

Bidirectional

Unidirectional
Characterizing TVS Device

Single shot measurement only

R. Ashton
Modeling Methodology
Modeling the IEC Stress

IEC Model Circuit

R, L, C values are tweaked to match the IEC spec

Simulation of 8kV IEC

\[ I_{\text{peak}} = 32 \text{A} \]

\[ I_1 = 16.3 \text{A} @ 30\text{ns} \]

\[ I_2 = 9.4 \text{A} @ 60\text{ns} \]
USB2 Protection With Zener (limited)

CDM Info : $I_p$

TLP Info : $I_{t2}$

TLP Info

$100\text{-ns Pulse IV}$

Power IC

$C_F B$

VCC pin

OMAP IC

$C_{M F}$

$C_{1}$

Receptacle

VBUS

$C_{3}$

$100\text{-ns Pulse IV}$

$TLP\text{ Info}$

$T V S$

Residual Pulse from Board Design

$TV S\text{ Response to IEC Pulse}$

IEC Stress
TVS Device Characteristics

- Maximum working voltage VM
- The TVS manufacturer recommends VM for long term use of the product.
- Maximum leakage currents are usually specified at this voltage
- Sufficient margin beyond nominal voltage values by considering the voltage ringing during fast transients
- This margin above the nominal voltage prevents the protection device from turning on during each signal transient.
TVS Device Characteristics

- Must not degrade signal integrity (SI)
- Capacitance is the most important factor for SI
- For USB and HDMI <1 pF (with 1MHz cap measurement)
- Eye Diagram is used to understand a protection device’s high speed properties.
TVS for high speed applications

- Random data patterns are applied at fixed frequency in persistent mode on a scope.
- A loss in signal integrity is seen with closing of the eye with repeating data patterns.
- The less signal distortion ➔ the less system performance degradation and give the system designers more margin for other elements in the signal path.
Random data pattern at a fixed frequency is observed in persistent mode on an oscilloscope which is time synced to the data source
Closing of the eye from the repeating data patterns represents loss of signal integrity
S-Parameters

- Another method to evaluate a TVS signal integrity is through S-parameters.
- S21 is the key parameter for insertion loss for a TVS.
- This measures how much signal is lost when the TVS is placed on a 50-Ohm transmission line and is measured in decibels (DB).
- The bandwidth limit for a system is when S21 reaches -3dB.
Signal Integrity

$S_{21}$ (insertion loss for a TVS device) gives how much signal is lost when a TVS device is placed on a 50 ohm transmission line and is expressed in dB.

Device A is better than device B
Silicon Based TVS Devices

Zener Diode

Higher breakdown devices have lower leakage

R. Ashton
Transient Behavior of PCB Protection Elements

Significant overshoot during turn-on of varistors and Polymer diodes

8 kV ESD event (contact discharge as per IEC 61000-4-2)

Voltage (V)

Time (ns)

Industry Council WP3P1/

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Oct09
Cap vs Voltage Zener TVS

Can be used for many medium and low signal lines
USB and HDMI Applications

R. Ashton
A Simple Device Based upon Overlapping Electrodes with continuous Polymer Film between the Electrodes
Polymer Physics is such the EPI device looks like a bidirectional Silicon Diode, but that is just the Start Point of Advantages.

A polymer ESD protection device is a thin film of polymer doped with conducting particles. It is bidirectional with ‘trigger’ and ‘clamp’ voltages and ‘snapback’ current characteristics.
High Speed Data Transfer

Eye diagrams show the HF system designer if the signal is impacted by the additional components on the signal line. EPI-Flo devices are essentially invisible during operation thanks to their extreme low capacitance. They, (EPI-Flo devices), only engage if dangerous ESD spikes hit the system.

Silicon based Diodes are considered “Ultra Low Capacitance” if they reach 500fF, Polymer Diodes have those values as worst case maximum and EPI-Flo devices can be at a typical capacitance of about 50fF (10x lower). This allows for freedom of enormous bandwidth if EPI-Flo devices are used for protection.
The “Box”
Antenna Vendors need the full bandwidth to unleash the full 5G Performance

Perfect match to the “Box”!
Covers 0-89 GHz

EPI’s newest technology will protect antennas in GSM phones built for the upcoming 5G standard. The EPI-Flo protector will allow full bandwidth coverage.

<table>
<thead>
<tr>
<th>Name</th>
<th>2G</th>
<th>3G</th>
<th>4G</th>
<th>5G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Date Line</td>
<td>since 1991</td>
<td>since 2001</td>
<td>since 2010</td>
<td>2020 Samsung &amp; Huawei evaluating right now</td>
</tr>
<tr>
<td>Freq.Band</td>
<td>~0.8 GHz</td>
<td>~1.7 GHz</td>
<td>~2.7 GHz</td>
<td>~15 GHz</td>
</tr>
<tr>
<td>Download Speed</td>
<td>&lt;0.024 Gbps</td>
<td>&lt;0.1 Gbps</td>
<td>&lt;1 Gbps</td>
<td>&lt;10 Gbps up to 89 GHz (theoretical)</td>
</tr>
<tr>
<td>Movie Streaming</td>
<td>Impossible</td>
<td>Download</td>
<td>Standard Resolution</td>
<td>Realtime HD</td>
</tr>
<tr>
<td>Standard</td>
<td>GSM</td>
<td>UMTS</td>
<td>LTE</td>
<td>No standard yet</td>
</tr>
<tr>
<td></td>
<td>GPRS</td>
<td>HSPA</td>
<td>LTE Adv.</td>
<td></td>
</tr>
</tbody>
</table>
EPI core laminate material consisting of patented nano-particle polymer which is sandwiched between two electrodes.
Polymers: ESD Protection Options

- Polymer is a nano-particle material device between two electrodes
- With breakdown it behaves like a bi-directional SCR

![Diagram showing polymer structure and ESD protection options]

- **Test 844 TLP I/V Curve**
  - Breakdown Voltage = 84.13 V
  - Snapback Voltage = 21.85 V
  - Dyn.On Resistance = 0.45 Ohm

Courtesy: Electronics Polymer
How it works

The ESD is shunt down at the area indicated. The polymer changes from non conductive state to conductive state in a few pico seconds after the ESD stress is applied. This is far faster than silicon based Diodes can react and ensure the excellent ESD protection capabilities of the EPI-Flo device. “EPI-Flo” concept, regardless if it is a connector array, a discrete protection or an interposer. Because of the relatively small active area, “EPI Flo" devices can be built into very small form factors.
Polymer Devices

- Polymer voltage suppressors (PVS): At high fields breakdown in the small spaces between the conducting particles creates a low resistance path in the polymer.
- The polymer films are laminated between electrodes and processed into devices using processes similar to printed circuit boards.
- PVS devices are always bidirectional snapback devices.
- PVS devices can be made into a number of form factors from 2 terminal surface mount devices including 0603, 0402 and 0201 form factors and multi line devices intended for interfaces such as HDMI.
- The polymer films can also be incorporated into connectors to provide built in protection.
- These devices offer very low capacitance, making them very attractive for high speed signal lines where any extra capacitance will degrade signal integrity.
RF Antenna Protection with Polymer

The polymer can be engineered to match the application, especially ultra high speed signals benefit from the exceptional low line capacitance (<0.05 pF)

Can have larger band width than TVS diodes

Can be implemented as an interposer to protect sensitive silicon area and replace a TVS device

Courtesy: Electronics Polymer
IC Pin Without Protection

IC Pin fails at 10A and does not meet the IEC test requirements
Parallel protection with polymer device takes majority of the current and reduces the stress current magnitude through the IC pin.
Polymer trigger under fast transients

The system passes 8kV IEC protecting the interface IC pin
Dynamic Resistance Comparison of Silicon ESD Protector Vs a Polymer Protector

![Graph showing measured current vs measured voltage for polymer and silicon devices.]

- **Polymer**
- **Silicon**
- **Polymer Dynamic Region**
- **Silicon Dynamic Region**

Devices tested are a PVS SMT=0201-20 and a SOT-23 Silicon for IEC 61000-4-2

- Silicon $R_{dyn} = 0.64 \, \Omega$
- Polymer $R_{dyn} = 0.42 \, \Omega$

Silicon diode fails at 22 A
MEMS Antenna Protection

RF Antenna Pins need <0.4 pF capacitance solution

They have breakdown capacitors around ~400 V

Their operation frequencies in the range of 5 GHz

TLP Captures the trigger at 160 Volts

This means the Polymer can protect the RF pin
Other Applications

A Customer Specification Example

- Trigger Voltage: 100V min, 150V max
- Clamp Voltage: 20V min, 40V max
- Capacitance: 100 fF max

Devices with > 40 V applications can use the EPI solution
# Comparison

<table>
<thead>
<tr>
<th>Device</th>
<th>Vtrig</th>
<th>Vhold</th>
<th>On-res</th>
<th>V@15 A</th>
<th>Speed</th>
<th>Cap</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zener</td>
<td>7.5 V</td>
<td>7.5 V</td>
<td>1-2 Ohms</td>
<td>35-40 V</td>
<td>1-2 ns</td>
<td>1 -2 pF</td>
<td>1-2 GB</td>
</tr>
<tr>
<td>PVS</td>
<td>70-80 V</td>
<td>20 V</td>
<td>&lt; 0.5 pF</td>
<td>&lt; 30 V</td>
<td>&lt;&lt; 1 ns</td>
<td>&lt; 50 fF</td>
<td>&gt; 5 GB</td>
</tr>
</tbody>
</table>

**Diagram:**
- **Left Panel:** Current vs. Voltage graph for a device showing a sharp increase in current at a certain voltage level.
- **Right Panel:** Voltage vs. Amplitude graph for a TLP test, indicating breakdown voltage, snapback voltage, and dynamic on resistance.
EPI Solutions

Antenna ESD Protection for cell phone

50 fF capacitance

No interference with signal up to 100GHz, enables 5G today

Does not create harmonics

Surge Applications for multiple long cords

Protection up to 80 Amps

Can be used in conjunction with lower trigger TVS devices
# IEC Protection Requirements

<table>
<thead>
<tr>
<th>Automotive Applications</th>
<th>Wireless Applications</th>
<th>Wireline Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN BUS</td>
<td>ANTENNA PORT</td>
<td>A/B LINE DRIVER</td>
</tr>
<tr>
<td>LIN BUS</td>
<td>USB</td>
<td>ETHERNET</td>
</tr>
<tr>
<td>CAMERA INTERFACE</td>
<td>CAMERA INTERFACE</td>
<td>HDMI</td>
</tr>
<tr>
<td>DISPLAY INTERFACE</td>
<td>DISPLAY INTERFACE</td>
<td>DISPLAY PORT</td>
</tr>
<tr>
<td>USB INTERFACE</td>
<td>HEADSET</td>
<td>eSATA*</td>
</tr>
<tr>
<td>SIM CARD INTERFACE</td>
<td>SIM CARD INTERFACE</td>
<td>*External Serial ATA</td>
</tr>
</tbody>
</table>

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# System Ports Connected to External Pins

<table>
<thead>
<tr>
<th></th>
<th>Relevant Stress Models</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8 kV IEC (contact)</td>
</tr>
<tr>
<td>USB</td>
<td>X</td>
</tr>
<tr>
<td>HDMI</td>
<td>X</td>
</tr>
<tr>
<td>Ethernet</td>
<td>X</td>
</tr>
<tr>
<td>Antenna port</td>
<td>X</td>
</tr>
<tr>
<td>Head set</td>
<td>X</td>
</tr>
<tr>
<td>CAN/LIN</td>
<td>X</td>
</tr>
<tr>
<td>A/B line driver</td>
<td>X</td>
</tr>
<tr>
<td>RF-ID</td>
<td></td>
</tr>
</tbody>
</table>
USB Roadmap

- **USB1**
  - 1995
  - 12MB
  - 130nm
- **USB1.1**
  - 2001
  - 48MB
  - 90nm
- **USB2**
  - 2004
  - 480MB
  - 65 to 28nm
- **USB3**
  - 2011
  - 5GB
  - 28nm

Includes compatible port for USB2

- Voltages: 5V, 3.3V, 1.8V

Industry Council
HDMI Projections

- Composite
- S-Video

- 65nm
- 32nm
- 28nm

- 2005
- 2008
- 2011
- 2012
- 2015

- Display Ports
- 5.4GB
Summary

Prevent ESD events to enter the System by using EPI Connector array protection. Arrays can be retrofitted and can be custom build to fit any interface connector on the board.

Place strategically EPI protectors on the PCB board to complete protection concept for very sensitive devices or protect antenna ports against unwanted ESD stress coupled into the system by the Antenna.

If on chip protection is insufficient or too expensive to place, use EPI Interposer to protect the silicon at handling and on board against system level ESD.
Backup
EPI Fabrication

Fabrication Design for an EPI-Core inserted in a FOUR Layer RF Module Providing Multiple Line ESD Protection for a GaAs Chip Package
PEI Protection Connector Array

EPI can retrofit to add extra ESD protection

Simply press over Male connector pins

Physical stability guaranteed by special self securing layout of the connector array IO’s

Used by Automotive and Military customers to fix and enhance field ruggedness of existing systems

Connector arrays can also be retrofitted by dropping the array into the male connector. This has been done enhance weak systems in the field for automotive and military customers.
EPI Flow Device

(1x0.6mm) or 0201 (0.6x0.3mm)

Other footprints available on

From standard DFN1006 (metric) and DFN0603 (Metric) or customer specific package sizes (see Picture of “Penny Custom device)

The performance of the device is also scalable. Trigger voltage, Clamping voltage and even the Capacitance can be adjusted to accommodate customer and application specific needs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>VDC</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Trigger Voltage</td>
<td>V_T</td>
<td>200</td>
<td>150</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>Clamping Voltage</td>
<td>V_C</td>
<td>&lt;50</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Response Time</td>
<td>T_R</td>
<td>200</td>
<td></td>
<td></td>
<td>pS</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C_IN</td>
<td>50</td>
<td>200</td>
<td>500</td>
<td>fF</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>I_L</td>
<td></td>
<td></td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>ESD Withstand</td>
<td># pulses</td>
<td>20</td>
<td>1,000-10,000</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>T_A</td>
<td>-55</td>
<td>+25</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>
EPI Protection

ESD and Surge protection on all Interface connectors

Defeat ESD stress before it enters the system

Easily fits the pin footprint of the connector
Solderable without adding any Board real estate

Connector arrays can be placed right under the IO connectors as they can be custom made to fit the connector pinout. No extra board space needed, solderable and self aligned.