Temperature Cycling in Electronics

Webinar Series: Tom O’Connor and Gil Sharon

June 20, 2013
Agenda

- **Introduction**

- **Part 1: Temperature cycling basics**
  - CTE mismatch in electronics assemblies
  - Temperature cycles in the field
  - Accelerating the life tests
  - Solders and their grain structures
  - Failure modes: Solder fatigue, PTH fatigue
  - How to perform temperature cycling studies

- **Part 2: Predicting performance with CAE**
  - Overview of Sherlock
  - Setting up a temp. cycle in Sherlock
  - Running an analysis
  - The results viewer
  - Interpreting the results
  - Validation documents for the various packages

- **Part 3 Q&A**
Speaker Bio

- **Research focus:**
  - Mechanical reliability of electronic systems and components
  - Multidisciplinary reliability of complex electro mechanical systems
  - Characterization and modeling of material behavior
  - Physics of failure of electromechanical and MEMS system
  - Mechanical performance of flip chip packages

- **Doctoral research**
  - Solder reliability
  - MEMS structures characterization
  - Embedded components failure analysis
  - Particle beam accelerator mechanical fatigue.

- **Experience at Amkor technology**
  - Advanced product development group as senior engineer
  - Analysis of chip-package interactions

- **Ph.D, Mechanical Engineering (University of Maryland)**
Introductions

- DfR Solutions is a laboratory services, engineering consulting & CAE software firm.
  - Specializing in the Physics of Failure (PoF) approach to investigating & learning from all types of failures in Electrical/Electronic (E/E) technologies with a focus on failure prevention.
  - DfR provides forensic engineering knowledge and science based solutions that maximize product integrity and accelerates product development activities, (a.k.a. the Reliability Physics approach to Total Product Integrity)
  - (i.e. E/E Quality, Reliability and Durability (QRD))
- Speakers: Gil Sharon and Tom O’Connor
Thermal Cycling Fatigue

- The majority of electronic failures are thermo-mechanically related*
  - By thermally induced stresses and strains
  - Root cause: excessive differences in coefficient of thermal expansion


CTE Mismatch in Electronics Assemblies

- **1st level interconnects**
  - Connect die to substrate
  - Can be underfilled
  - Global and local CTE mismatch
  - Not considered at “Board level”

- **2nd level interconnects**
  - Connect substrate to PCB
  - Several mitigation techniques exist
  - Conformal coating
  - Considered at board level
Temperature Cycles in the Field

- Field conditions are based on usage and application
- The same electronics assembly can have several field conditions depending on the industry

<table>
<thead>
<tr>
<th></th>
<th>Temp range</th>
<th>Cycles/year</th>
<th>Service time</th>
<th>Failure rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consumer</td>
<td>0 to 60 °C</td>
<td>365</td>
<td>1 year</td>
<td>1 %</td>
</tr>
<tr>
<td>Computer</td>
<td>15 to 60 °C</td>
<td>1460</td>
<td>5 years</td>
<td>0.1 %</td>
</tr>
<tr>
<td>Telecom</td>
<td>-40 to 85 °C</td>
<td>365</td>
<td>7 to 20 years</td>
<td>0.01 %</td>
</tr>
<tr>
<td>Aircraft</td>
<td>-55 to 95 °C</td>
<td>365</td>
<td>20 years</td>
<td>0.001 %</td>
</tr>
<tr>
<td>Automotive</td>
<td>-55 to 95 °C</td>
<td>100</td>
<td>10 years</td>
<td>0.1 %</td>
</tr>
</tbody>
</table>

- Examples: LCD touchpanels, voltage regulators, networking modules and many more.
- Special field conditions may exist
  - Long period of storage followed by short period of usage (Munitions, launch platforms, AED, airbags)
Accelerating the Life Tests

- Testing an electronics assembly for 20 years at 1 cycle/day is not desired
- In general: use stresses that are beyond normal life while maintaining the same dominant failure mode
  - Higher temperature
  - Higher load
- Accelerating the test can result in different failure modes to appear
- There are limits on how much a test can be accelerated
- Example: 15 minute ramps and 15 minute dwells = 24/cycles per day = 6 weeks for 1000 cycles
Example: Norris Landzberg Acceleration Factor

\[
AF = \left[ \frac{\Delta T_L}{\Delta T_f} \right]^{1.9} \left( \frac{f_f}{f_L} \right)^{1/3} \exp \left( 1414 \left( \frac{1}{T_{max_f}} - \frac{1}{T_{max_L}} \right) \right)
\]

L = Lab condition
f = Field condition
f = Frequency [Cycles/day]

<table>
<thead>
<tr>
<th>Use Condition</th>
<th>Use Condition Requirement</th>
<th>Equivalent Condition B -55 °C to +125 °C 700 cycles</th>
<th>Equivalent Condition G -40 °C to +125 °C 850 cycles</th>
<th>Equivalent Condition J 0 °C to +100 °C 2300 cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desktop 5 yr Life</td>
<td>ΔT 40 °C 2000 cy</td>
<td>14,175 cy (12,475 cy)* (11,057 cy)**</td>
<td>14,463 cy (12,761 cy)* (11,332 cy)**</td>
<td>14,375 cy (12,675 cy)* (11,250 cy)**</td>
</tr>
<tr>
<td>Mobile 4 yr Life</td>
<td>ΔT 15 °C 1500 cy</td>
<td>100,800 cy</td>
<td>102,850 cy</td>
<td>102,221 cy</td>
</tr>
<tr>
<td>Server 11 yr Life</td>
<td>ΔT 40 °C 44 cy</td>
<td>14,175 cy</td>
<td>14,463 cy</td>
<td>14,375 cy</td>
</tr>
<tr>
<td>Telecom (uncontrolled) / Avionics Controlled 15 yr Life</td>
<td>ΔT 25 °C 5500 cy</td>
<td>36,288 cy</td>
<td>37,026 cy</td>
<td>36,800 cy</td>
</tr>
<tr>
<td>Telecom (controlled) 15 yr Life</td>
<td>ΔT 6 °C 5500 cy</td>
<td>630,000 cy</td>
<td>642,812 cy</td>
<td>638,889 cy</td>
</tr>
<tr>
<td>Networking 10 year Life</td>
<td>ΔT 30 °C 3000 cy</td>
<td>25,200 cy</td>
<td>25,712 cy</td>
<td>25,557 cy</td>
</tr>
</tbody>
</table>
Controlling the Coefficient of Thermal Expansion

- It is unlikely that the designer or end user will be able to influence the component properties
  - Component packaging is typically driven by the die and assembly
  - Passing of JEDEC level package tests
  - Lead frame material has a limited number of options
- Controlling printed wiring board properties
  - Glass style
  - Laminate type
  - Copper Thickness
  - Board thickness
Influence of Board Properties

- Electronic packages used to have CTE values close to that of copper, 17.6 [ppm/°C]
  - Leadless packages = stiffer leads
  - Larger packages = more CTE mismatch effect
- Larger die and smaller packages reduced the overall CTE
  - Leadless ceramic chip resistors – 5.6 [ppm/°C]
  - QFN (quad flat no-leads) – 8 to 12 [ppm/°C]
- The CTE of laminates is decreasing, but:
  - The PCB laminate manufacturers do not make it easy to determine the CTE of their laminate
  - Low CTE laminates have their own set of problems
  - Trade off between low CTE and cost
Effect of PCB Glass Style

- Realistic target for board CTE is between 15 and 17 ppm/°C
- Most laminate suppliers provide CTExy values

<table>
<thead>
<tr>
<th>Property</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass Transition Temperature (Tg) by DSC, spec minimum</td>
<td>180</td>
</tr>
<tr>
<td>CTE, Z Axis Pre-Tg</td>
<td>45</td>
</tr>
<tr>
<td>CTE, Z Axis Post-Tg</td>
<td>230</td>
</tr>
<tr>
<td>CTE, X, Y Axes Pre-Tg</td>
<td>13-14</td>
</tr>
<tr>
<td>CTE, X, Y Axes Post-Tg</td>
<td>14-17</td>
</tr>
</tbody>
</table>

- These values are typically for a low resin content laminate (46%-50% resin content by weight, 7628 glass style)
- However the most popular laminates have much higher resin contents
  - Higher resin content = higher CTE
  - Lower modulus
Example: Calculating Modulus

- Back calculate what the resin only modulus is and compute modulus accounting for glass content
- Fr-4 board has fibers oriented in both X and Y direction
  - Assume that half the fibers are oriented in the X direction and half in the Y direction
  - Calculate $E_x$ or $E_y$

\[
E_{x,y} = \frac{V_f E_f}{2} + V_m E_m + \left( \frac{V_f}{2E_f} + \frac{V_m}{E_m} \right)^{-1}
\]

- Solve for $E_m$

\[
E_m = \frac{-\left(V_f^2 E_f + 4V_m^2 E_f + 4E_f - 2V_f E_{x,y}\right) \pm \sqrt{\left(V_f^2 E_f + 4V_m^2 E_f + 4E_f - 2V_f E_{x,y}\right)^2 - 4(2V_m V_f)(2 V_m V_f E_f^2 - 4V_m E_f E_{x,y})}}{2(2V_m V_f)}
\]

- Consider Positive value of $E_m$ as solution
Effect of Glass Style

- Modulus decreases as resin content increases
- CTE increases as resin content increases
- Copper content plays a significant role in PCB properties
- These values can be used in solder joint fatigue predictions

<table>
<thead>
<tr>
<th>Glass Style</th>
<th>Resin Content [Weight %]</th>
<th>Resin Content [Vol %]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1027</td>
<td>75%</td>
<td>86%</td>
</tr>
<tr>
<td>1037</td>
<td>75%</td>
<td>86%</td>
</tr>
<tr>
<td>106</td>
<td>72%</td>
<td>84%</td>
</tr>
<tr>
<td>1067</td>
<td>71%</td>
<td>84%</td>
</tr>
<tr>
<td>1035</td>
<td>70%</td>
<td>83%</td>
</tr>
<tr>
<td>1078</td>
<td>68%</td>
<td>82%</td>
</tr>
<tr>
<td>1080</td>
<td>64%</td>
<td>79%</td>
</tr>
<tr>
<td>1086</td>
<td>63%</td>
<td>78%</td>
</tr>
<tr>
<td>2313</td>
<td>57%</td>
<td>74%</td>
</tr>
<tr>
<td>2113</td>
<td>55%</td>
<td>72%</td>
</tr>
<tr>
<td>2116</td>
<td>54%</td>
<td>71%</td>
</tr>
<tr>
<td>3313</td>
<td>54%</td>
<td>71%</td>
</tr>
<tr>
<td>3070</td>
<td>50%</td>
<td>68%</td>
</tr>
<tr>
<td>1647</td>
<td>48%</td>
<td>66%</td>
</tr>
<tr>
<td>1651</td>
<td>48%</td>
<td>66%</td>
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<tr>
<td>2165</td>
<td>48%</td>
<td>66%</td>
</tr>
<tr>
<td>2157</td>
<td>48%</td>
<td>66%</td>
</tr>
<tr>
<td>7628</td>
<td>48%</td>
<td>64%</td>
</tr>
</tbody>
</table>
Solder Alloys and Grain Structures

- **Solder joints construction:**
  - Base metal at PWB
  - IMC solid solutions between the solder and the PWB base metal
  - Layer of solder that has been depleted due to IMC formation
  - Bulk solder grain structure
  - Layer of solder that has been depleted due to IMC formation
  - IMC solid solutions between the solder and the component base metal
  - Base metal at component termination

- **Grain growth over solder joint life**
  - Residual stresses will relax due to creep
  - Stresses from CTE mismatch in the solder will contribute to grain growth
  - Faster grain growth at higher temperatures
  - Grain growth forms micro-voids that grow into micro-cracks that grow into macro-cracks
Solder Alloys and Lead Types

- Components with leads
  - Super compliant leads
  - Compliant
  - Non-compliant

- Components without leads
  - With fillet
    - Chip resistors
    - Chip Capacitors
    - Metal Electrode Face (MELF)
    - Leadless chip carriers
  - Without fillet
    - Flip-Chip C4 (Controlled Collapse Chip Connection) “Bump”
    - BGAs C5 (Controlled Collapse Chip Carrier Connection) “Ball”
    - CGA (Column Grid Array) “Column”
Solder Shape: Different Failure Modes

- The different surface mount solder attachment types can have significantly different failure modes.
- Uniform load distributions: BGA
  - Advancing macro-crack
  - Localized grain growth micro-cracks

Non-uniform load distributions: Chip components, leaded components
  - Advancing macro-crack
  - Localized grain growth micro-cracks
Solder Fatigue Model (Modified Engelmaier)

- Modified Engelmaier
  - Semi-empirical analytical approach
  - Energy based fatigue
- Determine the strain range ($\Delta \gamma$)

\[
\Delta \gamma = C \frac{L_D}{h_s} \Delta \alpha \Delta T
\]

- $C$ is a correction factor, $\alpha$ is CTE, $h$ is solder joint height
  - $C$ is function of activation energy, temperature and dwell time
  - $L_D =$ diagonal distance
  - $\Delta \alpha = \alpha_2 - \alpha_1$
  - $\Delta T =$ temperature cycle
  - $h_s$ defaults to 0.1016 mm (5 mils)
Solder Fatigue Model (cont.)

- Determine the shear force applied to the solder joint

\[(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L_D = F \cdot \left( \frac{L_D}{E_1 A_1} + \frac{L_D}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left( \frac{2 - \nu}{9 \cdot G_b a} \right) \right)\]

- F is shear force, L_D is length, E is elastic modulus, A is the area, h is solder thickness, G is shear modulus, and a is edge length of bond pad

- Subscripts: 1 is component, 2 is board, s is solder joint, c is bond pad, and b is board

- Takes into consideration foundation stiffness and both shear and axial loads

- Leaded models include lead stiffness
Solder Fatigue Model (cont.)

- Determine the strain energy dissipated by the solder joint
  \[ \Delta W = 0.5 \cdot \Delta \gamma \cdot \frac{F}{A_s} \]

- Calculate cycles-to-failure \( (N_{50}) \), using energy based fatigue models for SAC developed by A. Syed – Amkor
  \[ N_f = (0.0019 \cdot \Delta W)^{-1} \]

- Energy Based model for SnPb
  \[ N_f = (0.0006061 \cdot \Delta W)^{-1} \]
Example Fatigue Calculations for a 2512 Resistor

- Low CTE part (Alumina 5.6 ppm/°C)
- Board thickness
  - This highlights why some component manufactures may test on thin laminates
**Effect of Lead Material**

- Fatigue predictions using Sherlock for TSOP type devices with Copper and Alloy 42 lead frames
Solder Alloys SnPb and SAC

- Tin Lead solder typically performs better under high stress thermal cycling conditions
  - Large ceramic devices (stiff parts)
  - Large changes in temperature
- Due to RoHS regulations most high performance parts are manufactured with Pb-free alloys
- SAC alloys tend to do better for moderate thermal cycles
SnPb vs. SAC

- Where does SnPb out perform Pb-free?
  - Leadless, ceramic components
    - Leadless ceramic chip carriers (crystals, oscillators, resistor networks, etc.)
    - SMT resistors
    - Ceramic BGAs
  - Severe temperature cycles
    - -40 to 125°C
    - -55 to 125°C

(-55) to 125°C, 70 minute cycle
SnPb vs. SAC: Resistors

Time to 1% failure for 2512 resistors attached with SAC or SnPb solder and subjected to long dwells (~8 hours)
SnPb vs. SAC: TSOP

Time to 1% failure for TSOPs attached with SAC or SnPb solder and subjected to long dwells (~8 hours)
Plated Through Hole Fatigue

- **PCB in thermal cycling**
  - expansion/contraction in the z-direction is much higher than that in the x-y plane.
  - The glass fibers constrain the board in the x-y plane but not through the thickness.

- **As a result**
  - Stress can be built up in the copper via barrels
  - Eventual cracking near the center of the barrel
Industry-Accepted Failure Model IPC-TR-579

- Determine stress applied ($\sigma$)
  - Assumes perfectly elastic deformation when below yield strength ($S_y$)
  - Linear stress-strain relationship above $S_y$

\[
\sigma = \frac{(\alpha - \alpha_{Cu}) \Delta T A_E E_E E_{Cu}}{A_E E_E + A_{Cu} E_{Cu}}, \text{ for } \sigma \leq S_y
\]

\[
\sigma = \frac{[(\alpha - \alpha_{Cu}) \Delta T + S_y \frac{E_{Cu} - E'_{Cu}}{E_{Cu} E'_{Cu}}] A_E E_E E_{Cu}'}{A_E E_E + A_{Cu} E_{Cu}'} \text{, for } \sigma > S_y
\]

- Determine strain range ($\Delta \varepsilon$)

\[
\Delta \varepsilon = \frac{\sigma}{E_{Cu}}, \text{ for } \sigma < S_y
\]

\[
\Delta \varepsilon = \frac{S_y}{E_{Cu}} + \frac{\sigma - S_y}{E'_{Cu}}, \text{ for } \sigma > S_y
\]
o Apply calibration constants
  o Strain distribution factor, \(K_d(2.5 - 5.0)\)
    o 2.5 recommended
  o Quality index, \(K_Q(0 - 10)\)
o Iteratively calculate cycles-to-failure \((N_f)\)

\[
\Delta \varepsilon_{\text{eff}} = \Delta \varepsilon \left( K_d \frac{10}{K_Q} \right)
\]

\[
N_f^{-0.6}D_f^{0.75} + 0.9 \frac{S_u}{E} \left[ \frac{\exp(D_f)}{0.36} \right]^{0.1785\log\frac{10^5}{N_f}} = 0
\]
Assessment of IPC-TR-579

- Based on round-robin testing of 200,000 PTHs
  - Performed between 1986 to 1988
  - Hole diameters (250 µm to 500 µm)
  - Board thicknesses (0.75 mm to 2.25 mm)
  - Wall thickness (20 µm and 32 µm)

- Advantages
  - Analytical (calculation straightforward)
  - Validated through testing

- Disadvantages
  - Validation data is ~20 years old
  - Unable to assess complex geometries (PTH spacing, PTH pads)
    - Complex geometries tend to change lifetime
  - Difficult to assess effect of multiple temperature cycles
  - Can be performed using Miner’s Rule
Factors

- The closer the CTEz value is to copper the better

- Laminate
  - Glass style
  - Resin

- Tradeoff
  - High glass content = Harder to drill
  - Copper ductility
The use of underfills, potting compounds and thick conformal coatings can greatly influence the failure behavior under thermal cycling.

- Any time a material goes through its glass transition temperature problems tend to occur.
- Conformal coating should not bridge between the PCB and the component.
- Underfills designed for enhancing shock robustness do not tend to enhance thermal cycling robustness.
Part 2: Sherlock and Temp. Cycling
Part 2: Sherlock CAE Tool

- Sherlock Automated Design Analysis™ is a software tool developed by DfR Solutions
  - Certifying the expected reliability of products
  - Circuit card assembly level analysis
- The software is designed for use by design and reliability engineers and managers in the electronics industry
Using Sherlock to Predict Thermal fatigue

- **Design Capture**
  - Automatically provides the detailed inputs to the modeling software and calculation tools

- **Life-Cycle Characterization**
  - Define the reliability/durability objectives
  - Set the expected environmental & usage conditions (Field or Test) under which the device is required to operate

![Thermal Profile](image-url)
Using Sherlock to Predict Thermal Fatigue

- **Load Transformation**
  - Determines the operational loads across a circuit board
  - Determines the load on individual parts and features.

- **Durability and Reliability Analysis**
  - Performs a design and application specific durability simulation
  - Calculates life expectations and reliability distributions
  - Risk Assessment for each component
  - Prioritizes risks by applying PoF algorithms to the virtual PCBA model
Open a Design File Directly From “File.tgz”
Files Imported/Exported Via Standard Menus

- **Import PCBA Layout,**
  - Gerber, ODB++, Eagle & Valor CAD formats.
- **Import BOM Parts List**
  - Correlated supplier component part # and industry/JEDEC package styles to auto link component to Sherlock’s libraries of component geometry and material property to the individual parts locations mounted on the PCB to create the computer models for the life assessment.
- **Define PCB Laminate & Layers to Calculate Substrate Performance**
Design Capture - Graphic Verification

- Files Viewable As PCB Layers
- Provides Feedback To The User

- Users can modify, delete and add parts
- Users can modify mount points
- Boards can be stacked up and assembled together
Verify Component Placement
Stack up Material Properties

- From the material properties of each layer, Sherlock calculates:
  - Thickness
  - Density
  - CTE x-y
  - CTE z
  - Modulus x-y
  - Modulus z

- Using the built-in laminate data library
Laminate Library: the “Laminates.csv” file

- Defines 48 Material Properties
- Over 400 built-in circuit board laminates
- Over 20 global producers
- New entries can be added by users
- Material properties can be modified and customized by user
Interpreting the BOM List

- Logic algorithms recognize:
  - Supplier Part Numbers
  - Industry package names
  - JEDEC package names
  - Internal part numbers

- The source of information is color coded

- Missing Data, Data Errors or Correlation Concerns are Flagged.
Interpreting the BOM List

Original parts list

Updated parts list: Unconfirmed

Updated parts list: Confirmed

Original parts list gets updated from the user’s parts database

User confirms the parts in the list
Add the Thermal Cycle

- Enter numbers by hand
- Load from a saved profile
- Copy/paste profiles
- Example: -55 to 125°C in one hour cycles
Add the Thermal Map (Click Click Click)
Align the Thermal Image to the Board

- Click and drag the blue board outline to the board image
- Click and drag the red legend outline to the legend image
- Verify that the thermal image is lined up to the components
- If there is a $\Delta T$ of $17^\circ C$ on the board (for example)
  - The “Hot” areas will cycle from $-55^\circ C$ to $125^\circ C$
  - The “Cold” areas will cycle from $-55^\circ C$ to $108^\circ C$
Solder Fatigue Results

- Sherlock performs a solder fatigue calculation
  - Part by part
  - Each part has a temperature applied according to thermal map
- The board gets a score card for solder fatigue probability of failure
- The analysis uses PoF approach
Combined Life Prediction for the Board

**PTH Fatigue**

- **Module Score:** 1.1
- **Analysis Type:** Deterministic
- 7 or more: 0 (0.0%)
- 3 to 7: 433 (100%)
- less than 3: 0 (0.0%)
- **Timestamp:** 13/06/19 14:38:34

**Solder Fatigue**

- **Module Score:** 0.0
- **Analysis Type:** Deterministic
- 7 or more: 215 (97.3%)
- 3 to 7: 4 (1.8%)
- less than 3: 2 (0.9%)
- **Timestamp:** 13/06/19 14:37:04

**ODB++ Tutorial - Life Prediction**

- Service Life = 0.0 yrs
- Prob. of Failure Goal = 20%

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**Combined Life Prediction for the Board**

- **Combined**: 
- **PTH Fatigue**: 
- **Solder Fatigue**:

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**DfR Solutions**

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### Part List With Individual Scores Shown on the Board

<table>
<thead>
<tr>
<th>RefDes</th>
<th>Package</th>
<th>Part Type</th>
<th>Model</th>
<th>Side</th>
<th>Solder</th>
<th>Max $dT$ (C)</th>
<th>Max TTF</th>
<th>Damage</th>
<th>TTF (hrs)</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>U2</td>
<td>LCCC-20</td>
<td>IC</td>
<td>LCCC</td>
<td>TOP</td>
<td>63SN37PB</td>
<td>173.1</td>
<td>1.00</td>
<td>1.3E0</td>
<td>&gt;0</td>
<td>0.0</td>
</tr>
<tr>
<td>U1</td>
<td>LCCC-20</td>
<td>IC</td>
<td>LCCC</td>
<td>TOP</td>
<td>63SN37PB</td>
<td>171.2</td>
<td>1.00</td>
<td>1.3E0</td>
<td>&gt;0</td>
<td>0.0</td>
</tr>
<tr>
<td>U18</td>
<td>TSOP-32</td>
<td>(</td>
<td>IC</td>
<td>Leaded</td>
<td>TOP</td>
<td>63SN37PB</td>
<td>175.2</td>
<td>1.00</td>
<td>3.6E-1</td>
<td>&gt;0</td>
</tr>
<tr>
<td>U14</td>
<td>TSOP-32</td>
<td>(</td>
<td>IC</td>
<td>Leaded</td>
<td>TOP</td>
<td>63SN37PB</td>
<td>177.3</td>
<td>1.00</td>
<td>4.0E-1</td>
<td>&gt;0</td>
</tr>
<tr>
<td>U15</td>
<td>TSOP-32</td>
<td>(</td>
<td>IC</td>
<td>Leaded</td>
<td>TOP</td>
<td>63SN37PB</td>
<td>175.2</td>
<td>1.00</td>
<td>3.6E-1</td>
<td>&gt;0</td>
</tr>
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Summary

- **Temperature cycling basics**
  - CTE mismatch is the main driver for solder joint and PTH fatigue in electronics assemblies
  - Analytical tools can be used to predict solder joint and PTH fatigue
  - Board properties can be critical to performance

- **Sherlock is a powerful tool**
  - Speeds up the process
  - PoF based approach
  - Models actual life conditions
  - Quick visualization of results
Q & A

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Gil Sharon  gsharon@dfrsolutions.com