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Design for ESD Prevention & ESD Failure Analysis Techniques

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Instructor Biography

- Cheryl Tulkoff has over 20 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She holds leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years and is also an ASQ Certified Reliability Engineer.

- She has a strong passion for pre-college STEM (Science, Technology, Engineering, and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.

Design for ESD Prevention: What Do You Need to Do?

- ESD Protection is necessary at the IC, component package and system level
  - Different approaches are needed to achieve reliable protection
- Designing for ESD impacts both the product design and the manufacturing process controls
- What technologies are available to assure a reliable ESD protected product?
  - At the IC level
  - At the component package level
  - At the system level

Good General Design Practices for ESD Prevention

- Know the ESD rating for each part, and select parts (where possible) for the best ESD rating
  - Identify all ESD Sensitive Parts on drawings
  - Mark Locations of ESD Sensitive parts on the Board with the ESD symbol
- Consider the entire System (Design) as ESD Sensitive
- Use ESD Protection on all susceptible parts (not just System I/Os)
  - Box or System I/O
    - ESD Rating < Class 2 IEC 1000-4-2 (4000V) MANDATORY
  - Internal Components (not exposed to outside connectors)
    - ANSI/ESDA/JEDEC JS-001-2011, Human Body Model (HBM) - Component Level
      - ESD Rating <= Class 1 MANDATORY
      - ESD Rating < Class 2 WHEREVER POSSIBLE

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ESD Design Practices (cont.)

- High Speed, RF and GaAs parts will be particularly sensitive to ESD
  - GaAs Parts are typically rated as Class 0 (<250V) or Class 1A (<500V) – ONLY THE BEST PROTECTION DESIGN AND HANDLING PROCEDURES WILL PREVENT DAMAGE TO THESE PARTS!
    - Reference: ANSI/ESDA/JEDEC JS-001-2011-:Human Body Model (HBM) - Component Level
- Place ESD sensitive components and traces to avoid locations where the board may be handled
- Consider ESD as well as RF shielding
- Where possible install protective devices before ESD sensitive parts
- Avoid Coupled ESD events – Do not route traces to ESD sensitive parts near lines connected to the outside world

ESD Design Practices (cont.)

- Perform Circuit analysis to insure effectiveness of ESD protection (Class 2 ANSI/ESDA/JEDEC JS-001-2011 for internal, IEC 1000-4-2 level 2 for I/O)
- Test Boards and Systems for Internal and I/O ESD tolerance
- ESD Protection devices must be connected to a good ground to accommodate up to 30A ESD spikes.
  - If upset of operating circuits is to be avoided, a separate Earth ground should be used

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ESD Sensitive Parts (Pin Sensitivity)

- Any pin of a discrete ESD sensitive part (FET, Transistor, etc) may need protection (if not connected to a supply)
- Input pins
  - Can be sensitive since they have little or no built-in ESD protection
  - Especially on high speed devices like GaAs ICs or discretes,
- Pins other than inputs (on an ESD sensitive part)
  - Can also be sensitive because an ESD pulse can affect internal voltage levels
  - Any improperly terminated or unprotected pin can be a conduit for ESD
- Supply pins
  - Provide reference bias connections
  - Should not need additional protection (as long as they are connected to the power supply)
- Outputs of logical or functional parts designed with active (usually buffered) output stages
  - May have clamping diode protection to the supplies and may not need additional protection – check the part ESD rating

Evaluate Potential ESD

- If ESD sensitive parts are used in design, the circuitry connected to device pins should be evaluated
  - Insure that it provides "attenuation" to prevent voltage in excess of the parts ESD rating from developing in case the pin or connected traces are contacted during board handling or system assembly.
- Often the recommended circuit components for operation of the part will provide adequate ESD protection.
  - This should be verified by analysis or simulation and extra protection added as required to limit the voltage seen at the part.
  - Assumptions for analysis/simulation
    - 2000V,1.5K, 100pf for Internal circuits
    - 4000V, 330 Ohms, 150pf for I/Os

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Design for ESD Prevention: ESD IC Device Specifications

- What should you be concerned about?
  - Completely different specification methods for ESD protection of components are commonly used
  - Designers may need to gather comparable data points from differing graphs and tables.
  - Some differentiators to look for and investigate further are outlined below

- IEC Rating: Verify that the ESD protection device is guaranteed to meet or exceed specifications in IEC 61000-4-2.

- Contact versus Air Discharge: Verify that identical specifications are being compared. Some devices are documented with high air discharge ratings, which can be incorrectly compared with the normally lower contact discharge ratings. Contact ratings are fairly repeatable, whereas air ratings vary.

IEC 1000-4-2 COMPLIANCE LEVEL	MAX TEST VOLTAGE, CONTACT DISCHARGE (kV)	MAX TEST VOLTAGE, AIR DISCHARGE (kV)
1	2	2
2	4	4
3	6	8
4	8	15

- Clamp Voltage: Choose a device with a maximum clamp voltage at a given peak current well below the level that the protected devices can tolerate. The lower, the better.

- Pulse Current: Beware of misleading approximations of peak power capacity. It can usually be improved by specifying a shorter peak duration.

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ESD IC Device Specifications

- Response Time: Faster-acting devices reduce the width of the pulse transferred, and these devices can help attenuate the peak clamp voltage.
- Parasitic Capacitance: Added capacitance degrades I/O signal rise and fall times. On lower-speed signals, this stray capacitance can be lumped into or can displace the need for EMI capacitors.
- Parasitic Inductance: Higher impedance in the clamp path (to VDD or ground) can increase the effective system clamp voltage.
- Multistrike Capability: Verify that the protection designed-in can survive the expected life of the system. Resultant field failures are difficult to diagnose and can manifest themselves in unexpected functional errors, or even data loss.
- Integration and Matching: High-speed differential signals, such as in IEEE 1394, benefit from matched loading on the positive and negative lines of each pair. ESD protection products with multiple devices per package (such as thin-film silicon) can have intrachip device-to-device parasitic impedance matching of less than 0.1%. Unitary packages, however, may vary as much as 30% interchip matching. Printed-circuit-board (PCB) signal routing restrictions may also indicate a need for tight multidevice integration.

Design for ESD Prevention & IC Design Rule Checking

- Many ESD design rules
- Two common types of design rule verification/compliance
  - Design Rule Checking (DRC): standard DRC tools with ESD marking layers
    - Example: Mentor Graphics Calibre PERC
      - Rule 1: Primary Protection for I/O Pad
        - For each net in design, IF net is connected to IO Pad THEN check for up HBM diode and down HBM diode IF diode(s) missing THEN ESD Error
      - Rule 2: Secondary Protection for I/O Pad
        - For each net in design, IF net is connected to input buffer and IO Pad THEN check for CDM up diode and CDM down diode check if CDM resistor exists and is correct value IF diode(s) missing or resistor incorrect THEN ESD Error
  - Net-oriented: in-house tools for circuit analysis.

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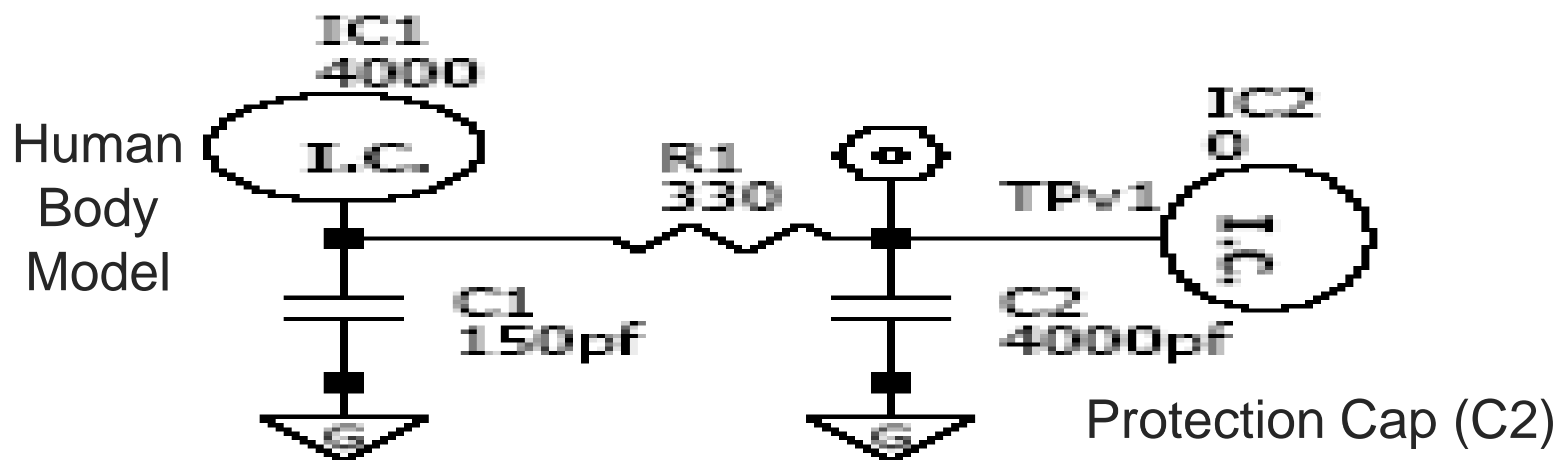
ESD Protective Device Options

- Passive Networks
  - Capacitors – Simple, Low cost
  - Band-pass filters – Somewhat more complex, good ESD protection
- For lower speed devices
  - Schottky Diodes – Simple, but capacitance loads HF circuits
  - Diode Clamping Arrays – Good for LF circuits and outputs
- For higher speed devices (requiring low capacitance)
  - Low capacity protection diodes (<1 pf) – Robust, Good HF compromise
  - Polymer ESD (PESD) Protection devices (<0.25 pf)
    - Excellent HF characteristics, small size 0402, 0603
    - PESDs have limited Pulse life, good parts withstand 100 to 1000 strikes
    - Operating voltage typically 5V, available to 12V, Trigger Voltage 100, 150V

Simple Capacitive Protection

- Use to provide ESD protection on bypassed pins for ESD sensitive devices, or at Supply input connections
  - Make sure capacitance (C2) is significantly larger than the Human Body Model (>> 150pf) to minimize developed voltage (approx 28 times or 4000pf for protection of a Device with an ESD sensitivity of 150V)
  - May add a Resistor to bleed off charge (from C2)
  - Use 200V rated Cap (for C2)



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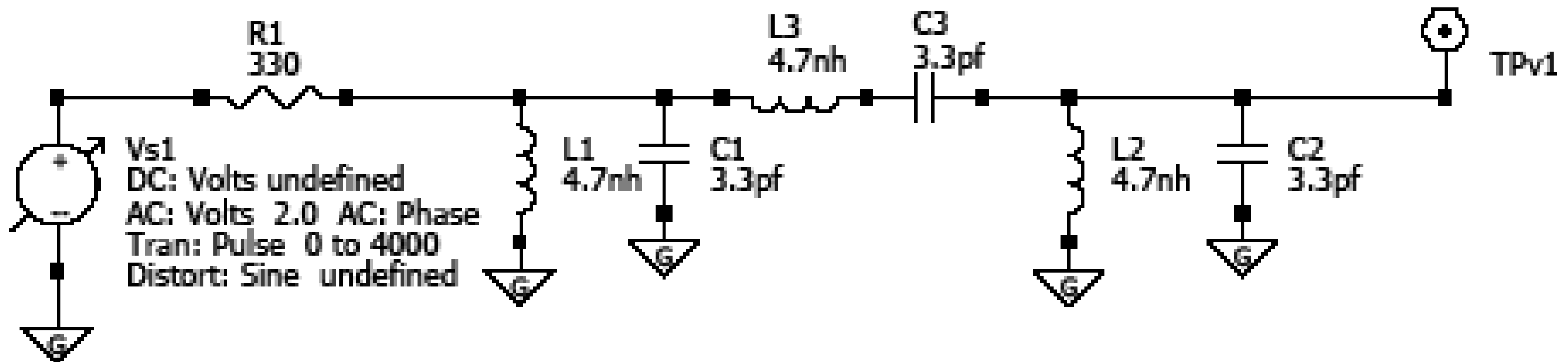
Filters

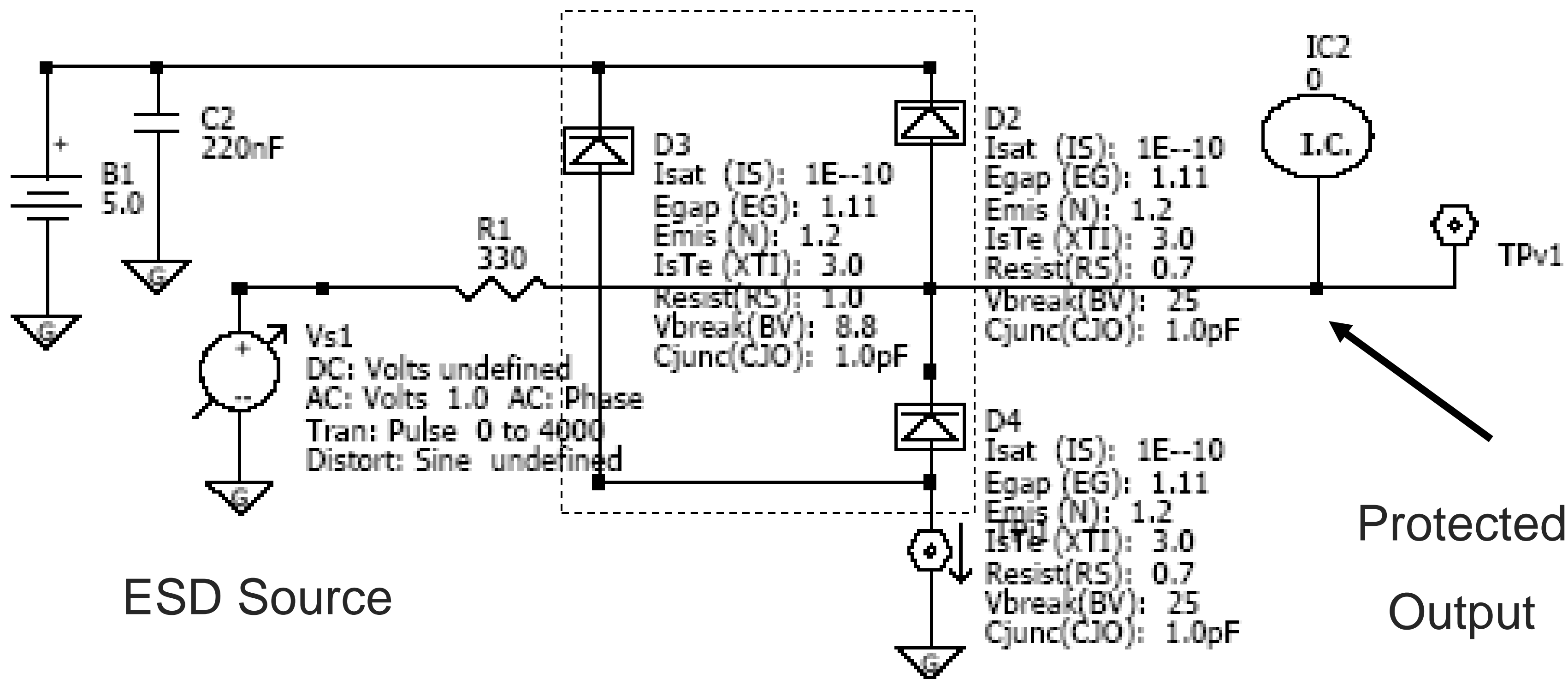
- Band-pass filters can be used for higher frequency applications and can be effective for RF system inputs
- Very Robust circuit with good protection



Band-pass Filter 850-2GHz, 50 Ohm Impedance
C1,C2,C3 rated at 100V

Protection with Clamping Diodes

Protection Diode Array (CM1213-01)



ESD at output is clamped at approximately 14V with 4000V ESD hit through 330 Ohm resistance

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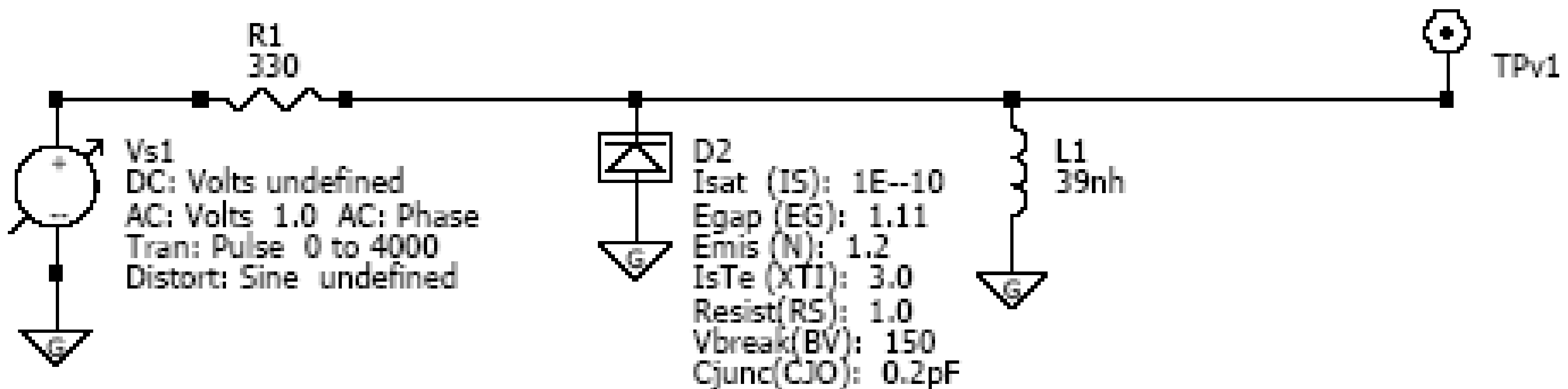
PESD (Polymer ESD) plus Inductor

IEC HBM

PESD, Trigger Voltage =150V



- The Inductor shunts lower frequency energy to ground, removing stress from the PESD.
- Provides better protection than the PESD alone and extends life of the PESD
- The PESD can be used alone for wider bandwidth operation

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Summary of ESD Design Guidelines

- Design ESD Protection for External (System) I/Os to IEC HBM Class 2 (4000V, 150pf, 330 Ohm) Including:
  - RF or signal inputs
  - Control and System I/Os that DO NOT have built in protection to the required limit
- Design ESD Protection for Internal ESD sensitive parts to meet ANSI/ESD S20.20
- Know the ESD rating of every part used
- Select parts (where possible) to meet ANSI/ESDA/JEDEC JS-001-2011-:Human Body Model (HBM) - Component Level 2
  - Parts rated less than Class 2 should have additional protection circuitry added to protect the board during handling

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ESD Design Guidelines (cont.)

- For External (System) Inputs use Robust protection:
  - Band pass filter
  - PESD plus Inductor (for Severe condition use PESD + Filter)
- For Internal ESD Sensitive pins use:
  - Single bypass Cap (where possible)
  - Filter if needed
  - PESD or PESD plus Inductor
- Any Pin of an ESD sensitive part may be at Risk If It is NOT:
  - Connected to a supply plane
  - Adequately decoupled to GND (~4000pf @200V)
  - Protected by a "filter" network (simulate for an ESD hit)
- External (System) Output or I/O
  - Use low capacitance Clamping diodes (1pf)
  - PESD if required for speed (.25pf)

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ESD Failure Mechanisms, Analysis and Tools

General Words of Wisdom on FA

- Before spending time and money on Failure Analysis, consider the following:
  - Consider FA "order" carefully. Some actions you take will limit or eliminate the ability to perform follow on tests.
  - Understand the limitations and output of the tests you select.
  - Use partner labs who can help you select and interpret tests for capabilities you don't have. Be careful of requesting a specific test. Describe the problem and define the data and output you need first.
  - Pursue multiple courses of action. There is rarely one test or one root cause that will solve your problem.
  - Don't put other activities on hold while waiting for FA results. Understand how long it will take to get results
  - Consider how you will use the data. How will it help you?
    - Information?
    - Change course, process, supplier?
    - Don't pursue FA data if it won't help you or you have no control over the path it might take you down. Some FA is just not worth doing

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Failure Analysis Techniques

- Returned parts failure analysis always starts with Non-Destructive Evaluation (NDE)
- Designed to obtain maximum information with minimal risk of damaging or destroying physical evidence
- *Emphasize the use of simple tools first*
- (Generally) non-destructive techniques:
  - Visual Inspection
  - Electrical Characterization
  - Time Domain Reflectometry
  - Acoustic Microscopy
  - X-ray Microscopy
  - Thermal Imaging (Infra-red camera)
  - SQUID Microscopy

Failure Analysis Techniques

- Destructive evaluation techniques
  - Decapsulation
  - Plasma etching
  - Cross-sectioning
  - Thermal imaging (liquid crystal; SQUID and IR also good after decap)
  - SEM/EDX – Scanning Electron Microscope / Energy dispersive X-ray Spectroscopy
  - Surface/depth profiling techniques: SIMS-Secondary Ion Mass Spectroscopy, Auger
  - OBIC/EBIC
  - FIB - Focused Ion Beam

Electrical Characterization: Components

- Most critical step in the failure analysis process
  - Can the reported failure mode be replicated?
  - Persistent or intermittent?
  - Intermittent failures often incorrectly diagnosed as no trouble found (NTF)
  - Least utilized to its fullest extent
  - Equipment often shared with production and R&D
- Parametric characterization
  - Comparison of performance to datasheet specifications
- Curve tracer
  - Applies alternating voltage; provides plot of voltage vs. current response
  - Valuable in characterizing diode, transistor, and resistance behavior
- Time domain reflectometry (TDR)
  - Release and return of electrical signal along a given path
  - Measurement of phase shift of return signal indicates potential location of electrical open
- Other characterization equipment
  - Inductance/capacitance/resistance (LCR) meter
  - High resistance meter (leakage current < nA)
  - Low resistance meter (four wire; < milliohms)

Examples of Lab Testing

- Electrostatic discharge test – Human body model
- Test method was MIL-STD-883, method 3015.8

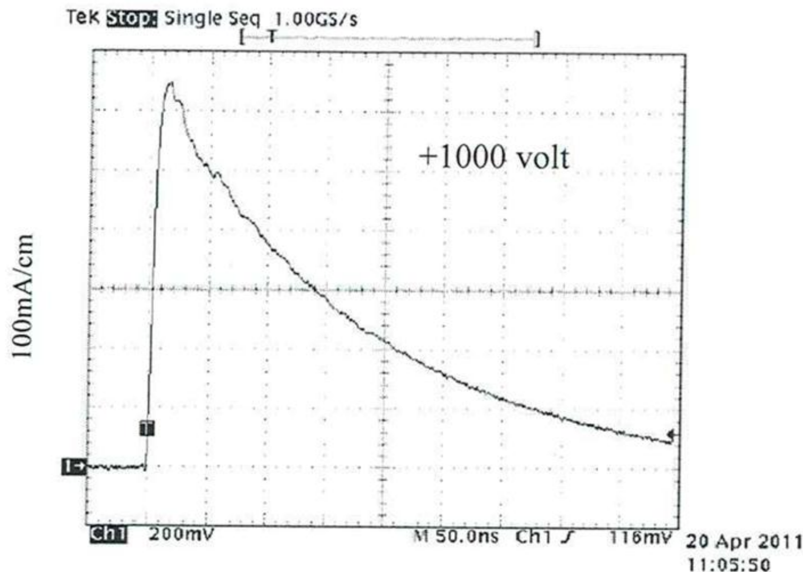


Figure 1. Prestress test positive pulse waveform.

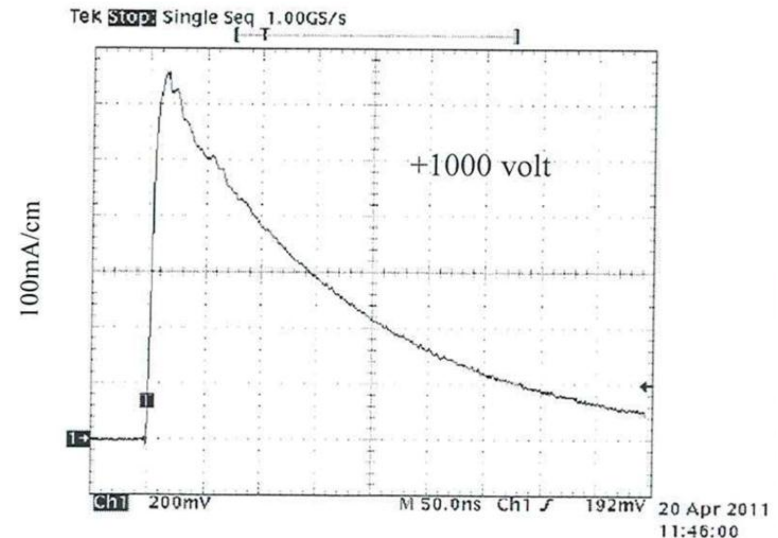


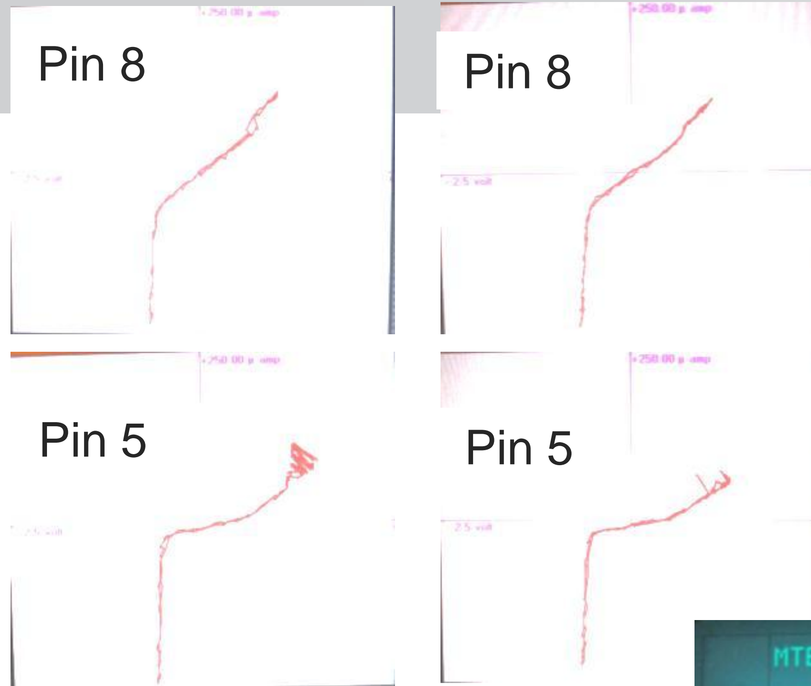
Figure 2. Post stress test positive pulse waveform.

Results
Electrical

Curve tracing example.

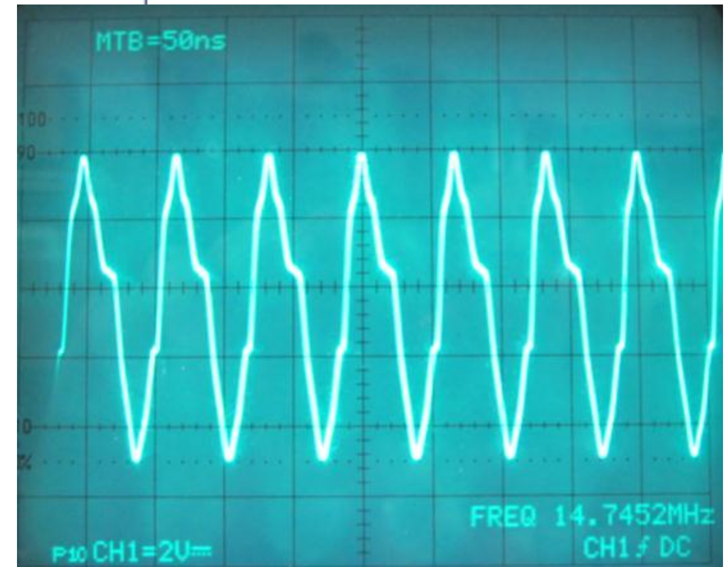
ESD damage was suspected in Part B

Part A   Part B



Curve tracing was done between power (pin 8), output (pin 5) and ground (pin 4). There is a slight difference in traces for the output signal between Part A and Part B.

Part B was powered at 3.3V and output monitored with a 10K ohm load. It operated at the specified frequency (14.745M Hz) but the wave form was not a square wave as expected.



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Trying to distinguish between EOS & ESD

- Often difficult to distinguish between EOS/EOL (electrical overstress and electrical overload) and ESD. Some rules of thumb:
- ESD damage
  - Small failure sites
  - Not always visible without deprocessing
  - No visible evidence at the package level
- EOS damage
  - Large areas of damage
  - Burned silicon and metallization
  - Sometime visibly evident package damage

Trying to distinguish between EOS & ESD

- EOS: Thermal overstress to a component's circuitry
  - Short Pulse Width Failure – Junction Spiking
  - Long Pulse Width Failures – Melted metallization and open bond wires
  - Junction spiking occurs when the amount of Al migration into the silicon substrate has reached the point wherein the Al has penetrated deep enough so as to short a p-n junction in its path. By that time an Al spike is said to have shorted the junction, damaging the device permanently.

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Images of ESD Damage

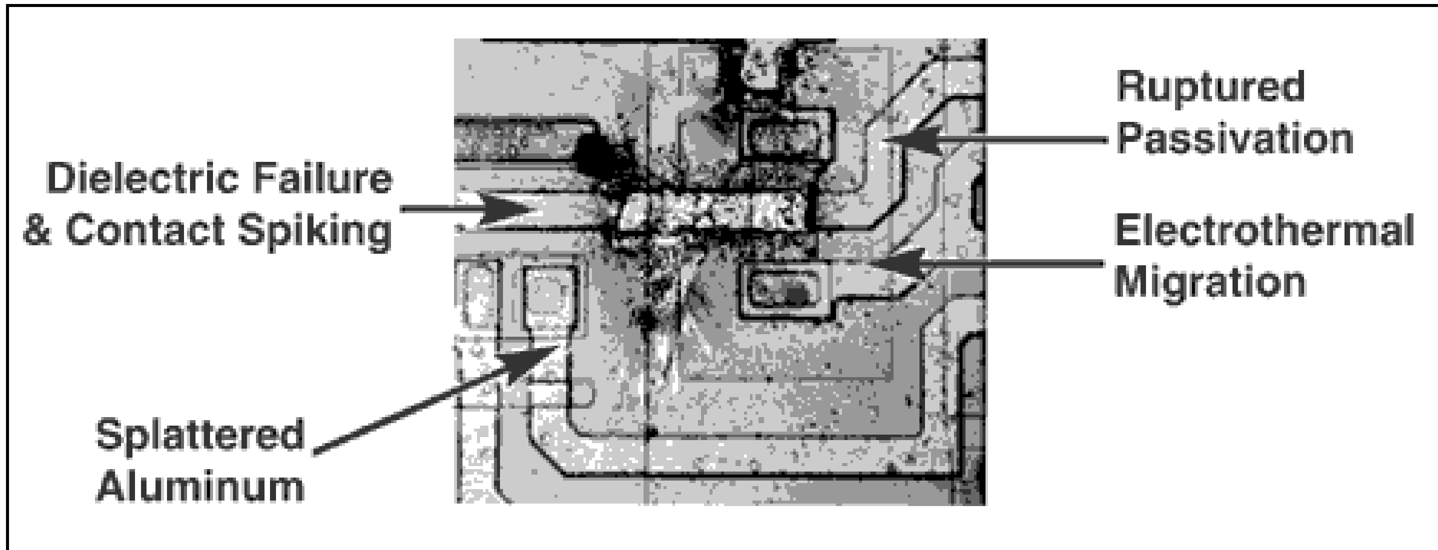

Figure 1. ICs with inadequate ESD protection are subject to catastrophic failure—including ruptured passivation, electrothermal migration, splattered aluminum, contact spiking, and dielectric failure. (Image courtesy of Maxim IC)

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ESD Failures: Latent Failures

Latent Failures

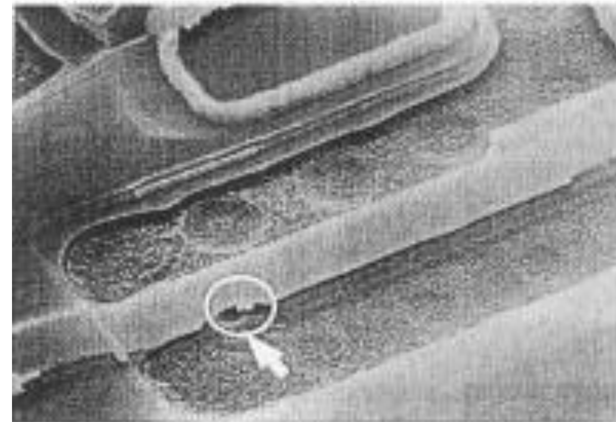
- ESD events not only impact assembly yields, but also can produce device damage that escapes testing and causes latent failures in the field.
- Devices with latent ESD defects have been referred to as "walking wounded" because they are degraded but still function
- Latent damage can occur when an ESD event is not sufficiently strong to destroy a device
  - Device continues to function and is still within data-sheet limits
  - Device can be subjected to numerous weak ESD events, with each new event further degrading a device until total failure
  - No known practical way to screen for walking wounded devices
  - Damage to insulators: weakening of the insulator structures, leading to accelerated breakdown and/or increased leakage
  - Damage to junctions: lowering the lifetime of minority carriers with consequent bipolar transistor gain loss; increasing resistance in forward biased state; increasing leakage in reverse biased state
  - Damage to metallization: weakening of the conductor, leading to increased resistance or increased rate of electromigration

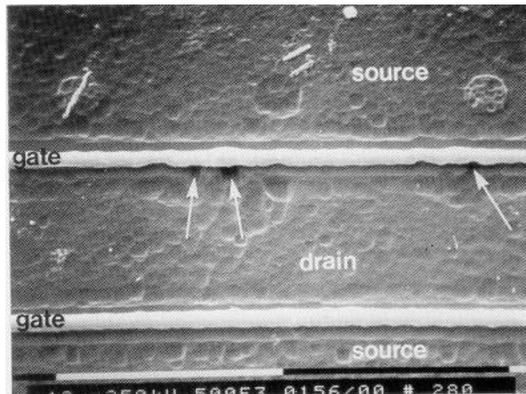
ESD Failure Modes

ESD Failure Modes

- Different ESD models tend to produce different types of failure and require different types of control and protection.
- Basic failure mechanisms include
  - Oxide punchthrough
  - Junction burnout
  - Metallization burnout

Gate-oxide damage to an input buffer after CDM stress. Note the rupture in gate oxide. Image courtesy of TI





Drain-junction damage in an NMOS after HBM stress. Note the thermal damage to silicon. Image courtesy of TI.

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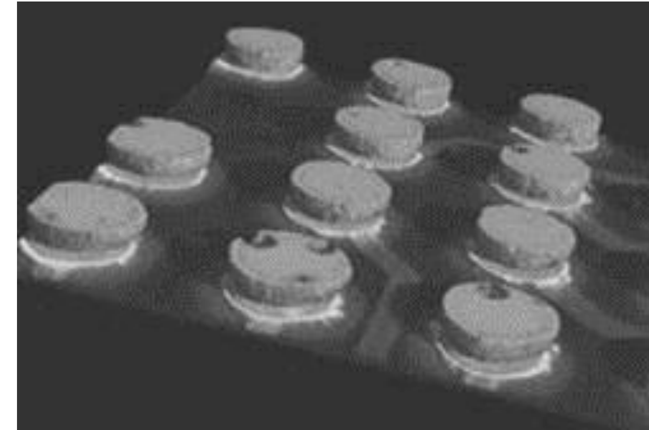
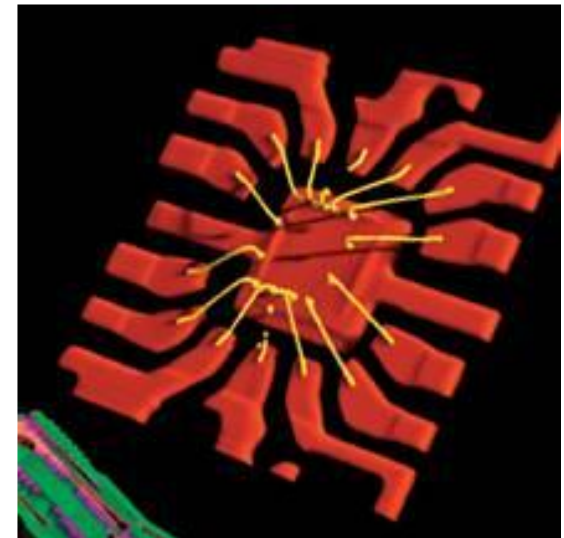
Commonly used Failure Analysis Equipment

X-Ray Microscopy

- Digital detector
  - Provides greater contrast through wider range of grayscale (elemental differentiation)
  - Prerequisite for 3-D imaging
- Laminography
  - Provides X-ray sectional images and slice in any direction as well as three-dimensional visualizations of the specimen
- Types of laminography
  - Agilent 5DX
    - Best setup for inline inspection; moderate FA capabilities
  - Everyone else (computed tomography)
    - Allows for 'virtual cross sectioning' and 3-D reconstruction
    - Requires rotation of the sample (limited sizing) and extensive exposure time
- Resolution
  - Sub-micron
- Oblique viewing
  - Increases capability of 2-D viewing
  - 60 to 80 degree capability





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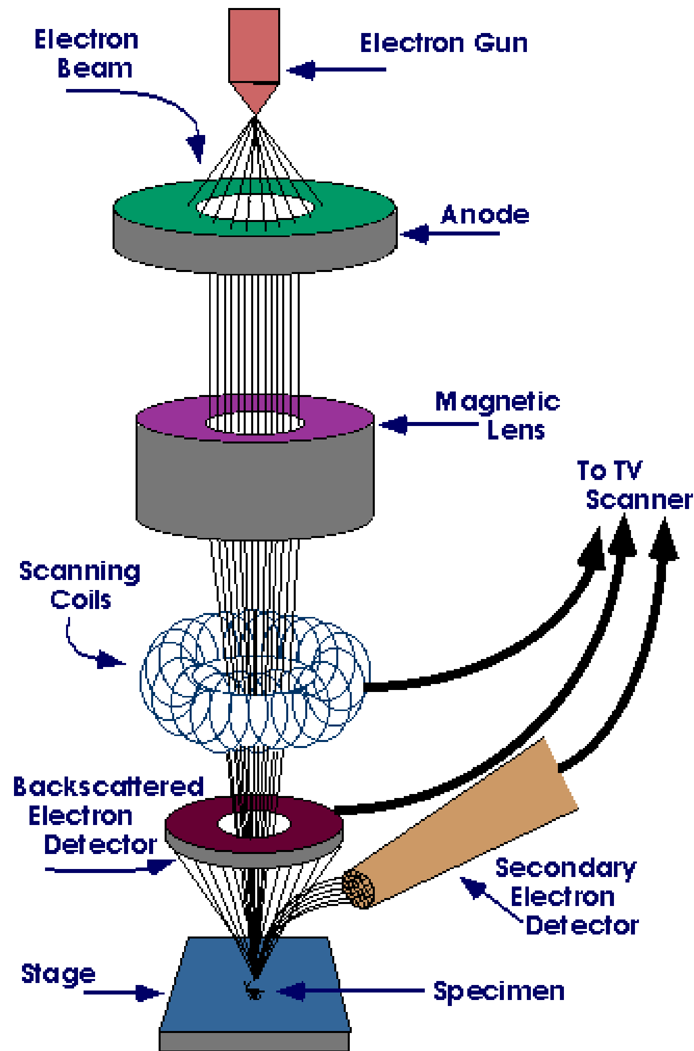
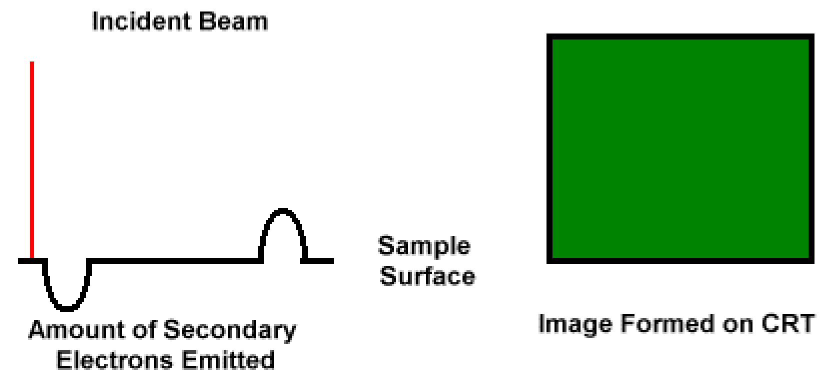
Scanning Electron Microscopy



- Sample rastered with an electron beam
- Emitted electrons sorted by delay and quantity



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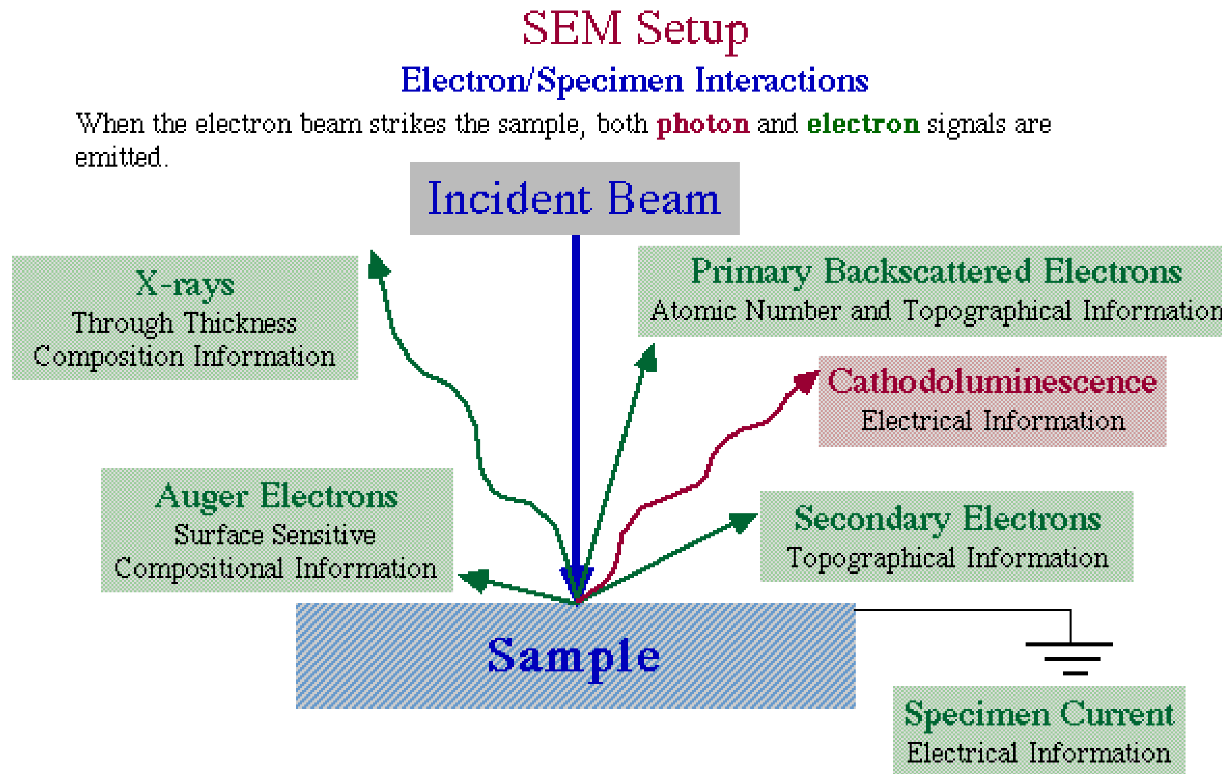
Scanning Electron Microscopy



- Secondary electron detection yields topographic information
- Backscattered electron detection also used for topography and elemental analysis

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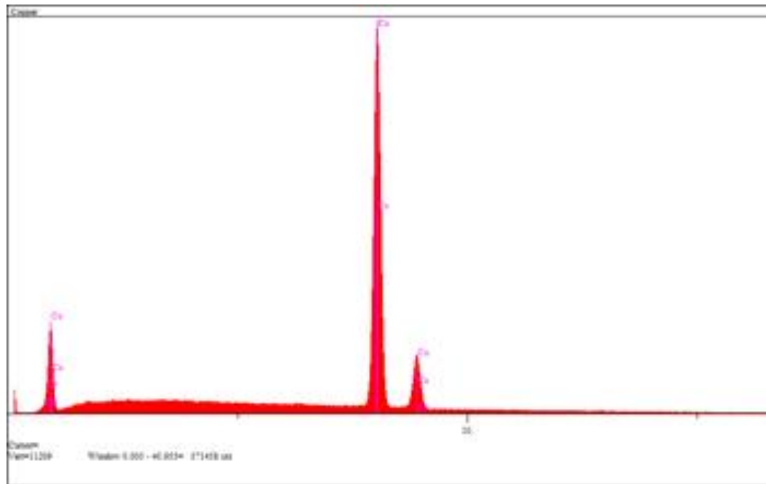
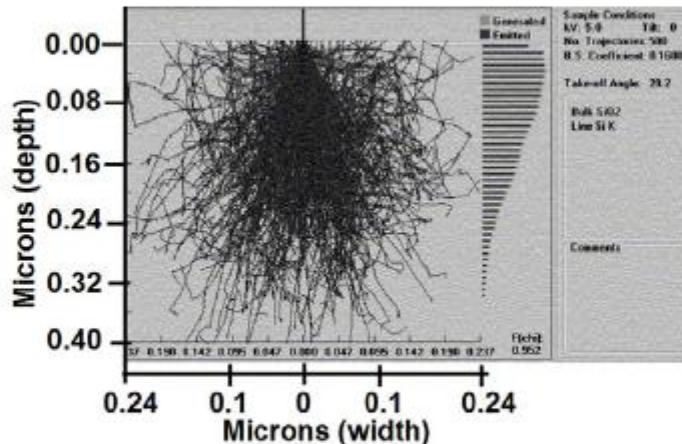
Energy Dispersive X-Ray Spectroscopy (EDS)

EDS scan of elemental copper



Monte Carlo simulation of Si K-α X-rays in an SiO2 matrix at 5 keV (Vanderlinde, 2004)



- Used with SEM
- X-ray emission signature from electron source
- Elemental analysis of solid samples
- Identification based on multiple emission lines (K, L, M)
- Can't detect light elements: H, He, Li, Be
- Emission from subsurface "tear drop"

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Decapsulation

- Note: point of no return! Voids any warrantees
- Mechanical preparation and removal
  - Non-critical material adjacent to die removed with diamond wheel
  - Gross package removal with razor blades, carbide/diamond drill bits, and polishing wheels
  - Stop once the tips of the wirebonds are contacted: electrical testing possible
- Chemical removal
  - **Warning:** significant safety precautions and training required
  - Methods: heated sample + dropper application or immersion
  - Fuming nitric acid: apply, rinse in IPA, ultrasonic rinse with methanol
  - Fuming sulfuric acid: apply, ultrasonic rinse in DI water and then methanol

Material	Nitric	Sulfuric	Dynasolve 160	Uresolve +
Anhydride epoxy		X		
Novolac epoxy	X			
2 part epoxy, Nylon			X	
Silicone package, gel				X
Silicone die coating		X		

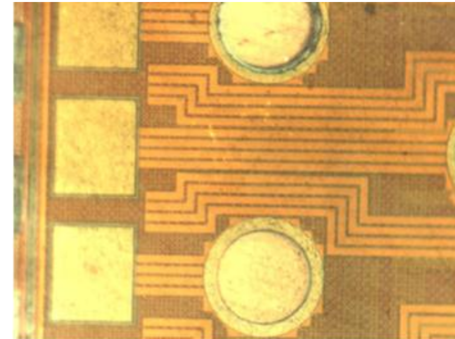
Source: Wills et al., Microelectronics Failure Analysis

Cross-Sectioning

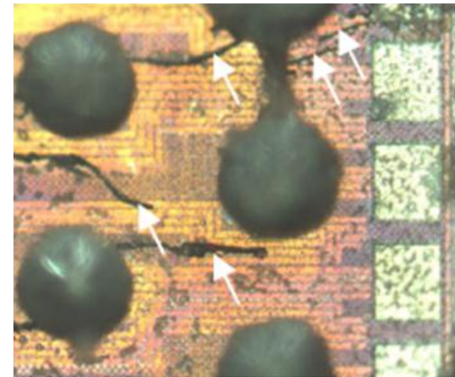
- Standard method for destructive subsurface evaluation
- Method:
  - Cleaving/sawing to approximate area of interest
  - Potting in epoxy resins to aid polishing
  - Polishing medium dependent upon materials: typically diamond, SiC, or alumina suspensions & embedded polishing cloths
  - Coarse to fine (600 grit to 0.05 um) grinding sequence to eliminate damage from previous step
  - Final etch often used for microstructural relief
  - Optical/electron microscopy techniques used for inspection thereafter

Cross-Sectioning: Chip Front & Backside Polishing

- Used to isolate single IC layers for defect inspection
- Top surface optical/SEM images can be correlated with top or bottom surface thermal/electrical/optical images (see subsequent techniques)
- Special fixtures and CMP methods used for maintaining parallelism



Parallel lapped low k ILD



Lap & plasma ash of underfill

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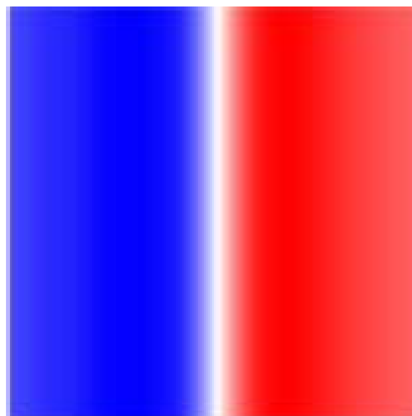
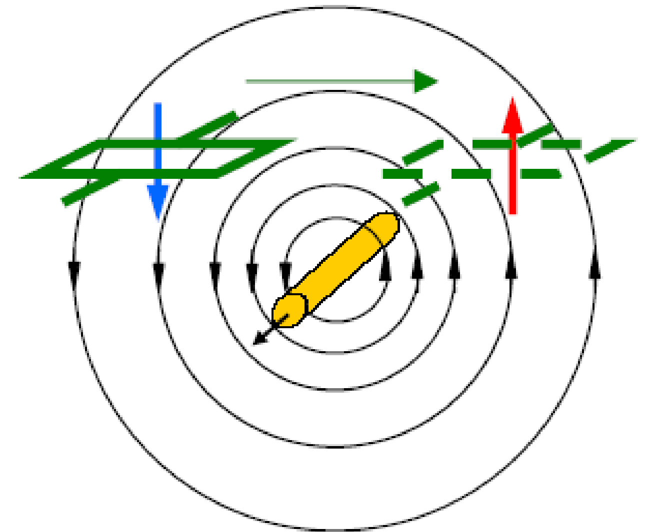
SQUID Microscopy

- Superconducting Quantum Interference Device (SQUID)
- Current flow in devices produce a magnetic field
  - SQUID uses a highly sensitive magnetic detector (superconductor) to resolve these fields
  - Magnetic field image is converted to a current density image, allowing for fault location
- Resolution
  - 500 nA, 300 nm
  - Dependent on working distance (requires a flat sample)





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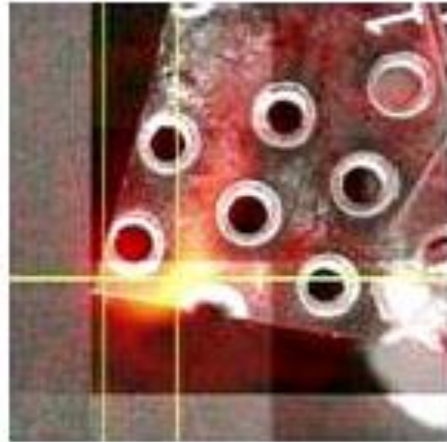
SQUID Microscopy

- Critical technology for detecting package level electrical shorts
  - Much more rapid failure site resolution
  - Absolute confirmation of shorting path
  - Thermal imaging induces damage



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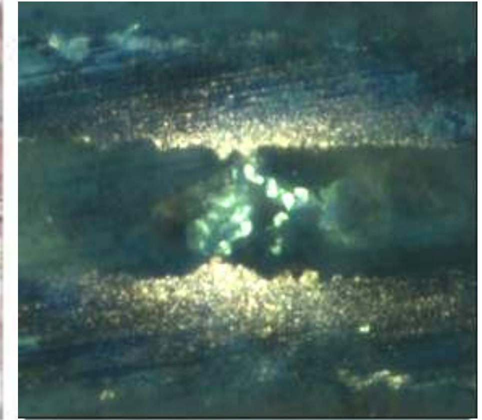

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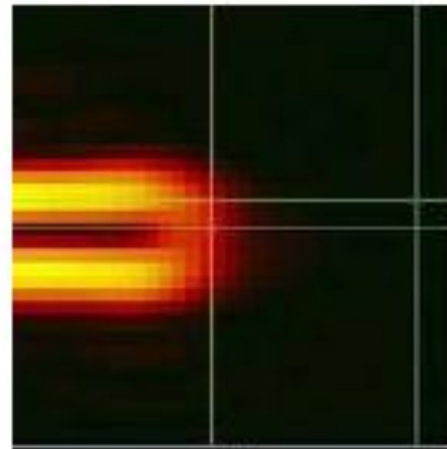

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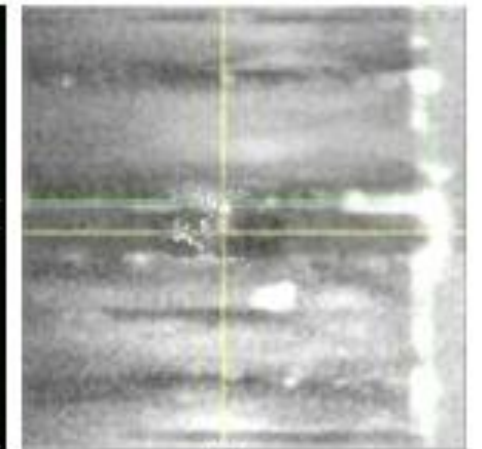

(d)

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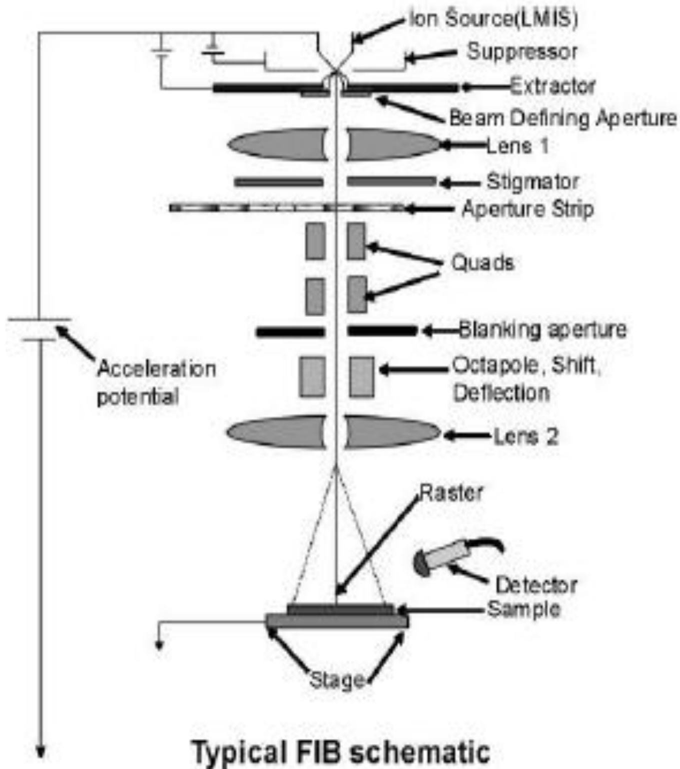
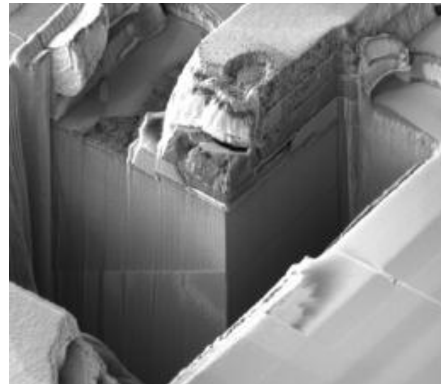
Focused Ion Beam (FIB) Microscopy



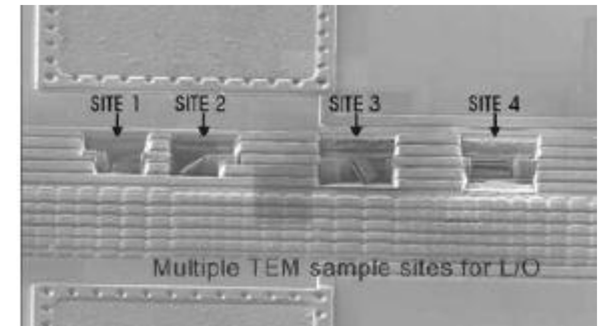
Typical FIB schematic

Source: Hooghan, Microelectronics Failure Analysis, 2004

- Similar to SEM, except that Ga ions are used instead of electrons
- Selective material removal with Ga ion beam
- Excellent for micro- cross sections, electrical circuit isolation, and TEM sample preparation

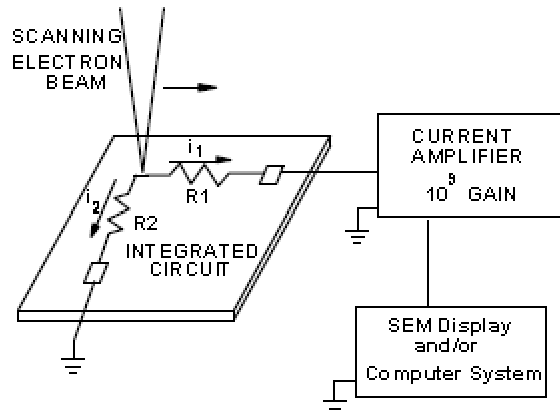


FIB cross-section of line

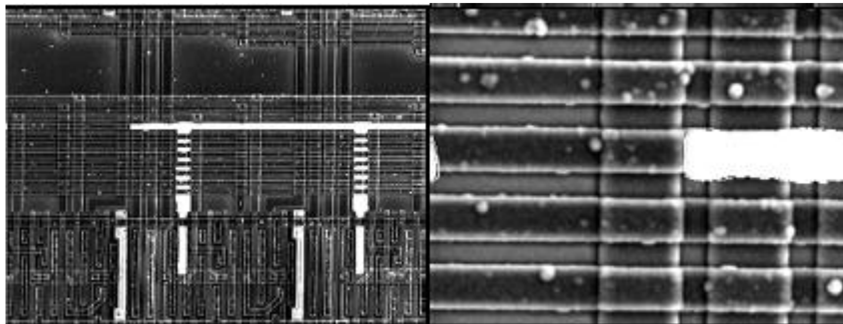


Sample removal for high resolution TEM

Electron Beam Techniques



Schematic of RCI



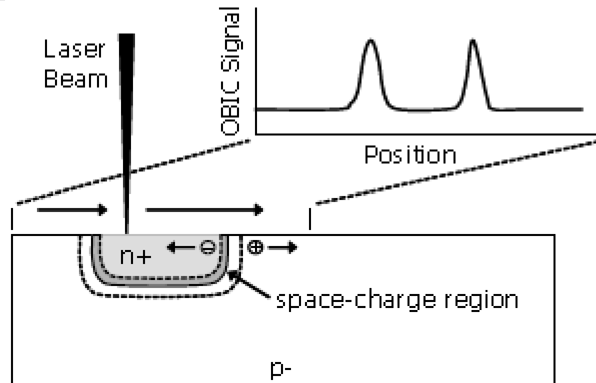
CIVA image showing location of open conductor

Source: Cole, Sandia National Labs, 2004

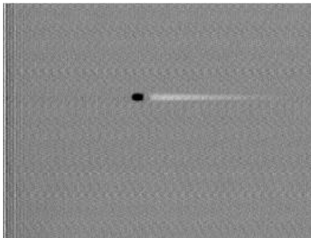
- Techniques utilize SEM with electrical vacuum feed-through
- Electron beam-induced current (EBIC)
  - Fermi transitions
  - Si defects
- Resistive contrast imaging (RCI)
  - Buried and open conductors
  - Passivated ICs
- Charge-induced voltage alteration (CIVA)
  - Open conductors
  - Passivated and depassivated ICs

Optical Beam Techniques

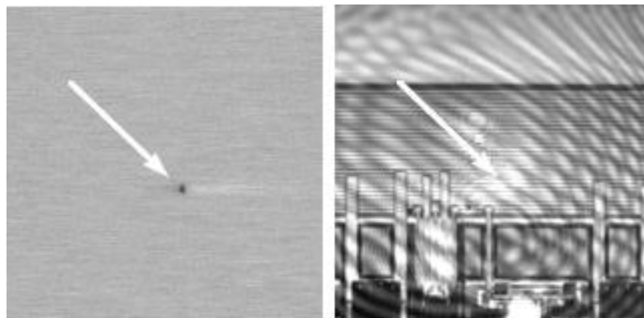
Schematic of OBIC



LIVA and reflected image of microcontroller



TIVA and reflected image of SRAM



Source: Cole, Sandia National Labs, 2004

- Techniques utilize SOM (scanning optical microscope) and lasers
- Optical beam-induced current (OBIC)
  - Fermi level mapping
- Light-induced voltage alteration (LIVA)
  - Visible laser on front, IR on back
  - IC defects, logic states, ESD
- Optical beam-induced resistance change (OBIRCH) and thermally-induced voltage alteration (TIVA)
  - IR > 1.1 um (> band gap of Si)
  - Electrical shorts
- Seebeck effect imaging (SEI)
  - Opens

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Questions

Contact information:

Cheryl Tulkoff

512 913 8624

ctulkoff@dfrsolutions.com

www.dfrsolutions.com

DfR Solutions

Your Partner Throughout the Product Life Cycle

DfR lends a guiding hand on quality, reliability and durability (QRD) issues through our expertise in the emerging science of Reliability Physics, providing crucial insights and solutions early in product design, development and test throughout manufacturing, and even into the field.

Your Needs…

- …faster time to market
- …find, incorporate new technologies
- …extend warranty period
- …reduce warranty costs
- …technically manage suppliers
- …improve employee skills
- …out perform your competition

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...Our Capabilities

- DfR uses Physics-of-Failure (PoF) and Best Practices expertise to provide knowledge-based strategic quality and reliability solutions to the electronics industry
  - Technology Insertion
  - Design
  - Manufacturing and Supplier Selection
  - Product Validation and Accelerated Testing
  - Root-Cause Failure Analysis & Forensics Engineering
- Unique combination of expert consultants and state-of-the-art laboratory facilities
  - Capabilities at package, board, product, and system-level

How Do Companies Use DfR?

- Work overflow
  - Maximize the efficiency of your current staff
- Independent party on critical design reviews
- Supplier benchmarking (commodity / custom)
- Test plan development and execution
- Reliability predictions
- Root-Cause Analysis
- Continuing education

Military / Avionics / Space
- Lockheed Martin
- Northrop Grumman
- Boeing
- General Dynamics
- BAE Systems
- Honeywell
- Hamilton Sundstrand
- Rockwell Collins

Government
- NAVAIR
- NASA
- Air Force

Contract Manufacturers
- Flextronics
- Benchmark Electronics
- Jabil
- Gold Circuit Electronics
- Viasystems

Enterprise / Telecom / ATE
- Cisco Systems
- Huawei
- Sun Microsystems
- Motorola
- Alcatel-Lucent
- Juniper Networks
- KLA-Tencor

Auto / Transportation
- General Motors
- Caterpillar
- Panasonic Automotive
- TRW
- Magna
- Takata

Materials
- Graftech
- Nihon Superior

Consumer / Appliance
- Dell Computers
- Hewlett Packard
- Apple
- Fujitsu
- Samsung
- LG Electronics
- Microsoft
- Xerox

Portables
- LG Electronics
- Kyocera

Components
- Samsung
- Fairchild Semiconductor
- International Rectifier
- Nvidia
- Amphenol
- NIC

Industrial / Power
- General Electric
- Siemens
- Emerson Electric
- Schlumberger
- Ingersoll Rand
- Danaher Motion
- Olympus
- Tyco Electronics

Medical
- Philips Medical
- Medtronic
- Boston Scientific
- Cardinal Health
- Beckman Coulter
- Biotronik
- Cameron Health
- Cardiac Science
- Zoll Medical

DfR Solutions – Senior Experts

- **Dr. Craig Hillman, CEO and Managing Partner**
- Expertise: Design for Reliability (DfR), Pb-free Transition, Supplier Benchmarking, Passive Components, Printed Circuit Board
- PhD, Material Science (UCSB)

- **Dr. Nathan Blattau, Vice President**
- Expertise: Power Devices, DfR, Nonlinear Finite Element Analysis (FEA), Solder Joint Reliability, Fracture, Fatigue Mechanics.
- PhD, Mechanical Eng. (University of Maryland)

- **Cheryl Tulkoff, CRE**
- Expertise: Pb-Free Transition, PCB and PCBA Fabrication, IC Fabrication, RCA (8D and Red X)
- B.S., Mechanical Engineering (Georgia Tech)

- **Dr. Ron Wunderlich**
- Expertise: Design for EMI/EMC, Power Supply Design, Analog Circuit Design, Spice Model Development, Monte Carlo Circuit Simulation
- PhD, Electrical Engineering (SUNY – Binghamton)

- **Greg Caswell**
- Expertise: Nanotechnology CMOS, CMOS/SOS, Input Protection Networks / ESD, SMT, Pb-free
- B.S., Electrical Engineering (Rutgers)

- **Dr. Randy Schueller**
- Expertise: IC Fabrication, IC Packaging, Pb-Free Transition Activities, Supplier Benchmarking, Corrosion Mechanisms
- PhD, Material Science (University of Virginia)

- **Dr. Gregg Kittlesen**
- Expertise: Semiconductor Lasers, Microprocessors, Memory Components, Photonic and RF Technologies, Supply Chain Management
- PhD, Inorganic Chemistry (MIT)

- **James McLeish, CRE**
- Expertise: FMEA, Root-Cause Analysis, Warranty Analysis, Automotive Electronics, Physics of Failure, Battery Technology
- M.S., Electrical Eng. (Wayne State University)

- **Norm Anderson**
- Expertise: Avionics, Product Qualification, Safety Criticality Assessment, FTA, FMEA, Component Uprating, Obsolescence
- B.S., Electrical Engineering (Iowa State University)

- **Anne Marie Neufelder**
- Expertise: Software Reliability Prediction, Best Practices in Software Risk Management
- B.S., Systems Engineering (Georgia Tech)

- **Walt Tomczykowski, Vice President, CRE**
- Expertise: Systems Eng., Life Cycle Management (including obsolescence), Spares Analysis, Counterfeit Mitigation, Failure Analysis
- M.S., Reliability Eng. (University of Maryland)

DfR Locations (North America)

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DfR Resources and Equipment

Electrical

- Oscilloscopes (Digital and Analog)
- Curve Tracers (Digital and Analog)
- Capacitance Meters
- Low/High Resistance Meters
- High Voltage Power Supplies (Hi-Pot)
- Network Analyzer (up to 3 GHz)

Testing

- HALT / HASS
- Temperature Cycling
- Thermal Shock
- Temperature/Humidity
- Vibration
- Mechanical Shock / Drop Tower
- Mixed Flowing Gas
- Salt Spray
- Capacitor Testing (Ripple Current, Step Stress, Partial Discharge)
- Bend Testing (Cyclic and Overstress)
- Mechanical Testing

Material Analysis

- X-ray
- Acoustic Microscopy
- Infrared Camera
- Metallographic Preparation
- Stereoscope
- Optical Microscope
- Scanning Electron Microscope
- Energy Dispersive Spectroscopy
- Ion Chromatography
- FTIR (Solid / Film / Liquid)
- Thermomechanical Analyzer
- Mechanical Testing (Tension, Compression, Shear, etc.)
- SQUID Microscopy

Other

- Circuit Simulation
- Finite Element Analysis (FEA)
- Computational Fluid Dynamics
- Reliability Prediction (Physics of Failure)

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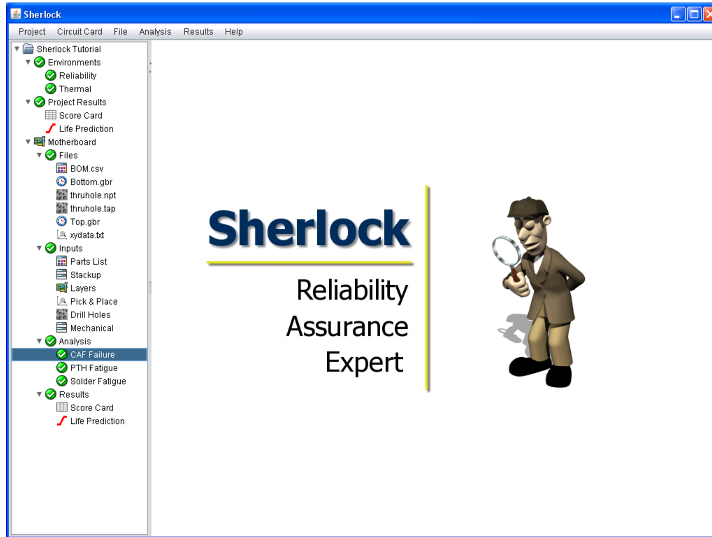
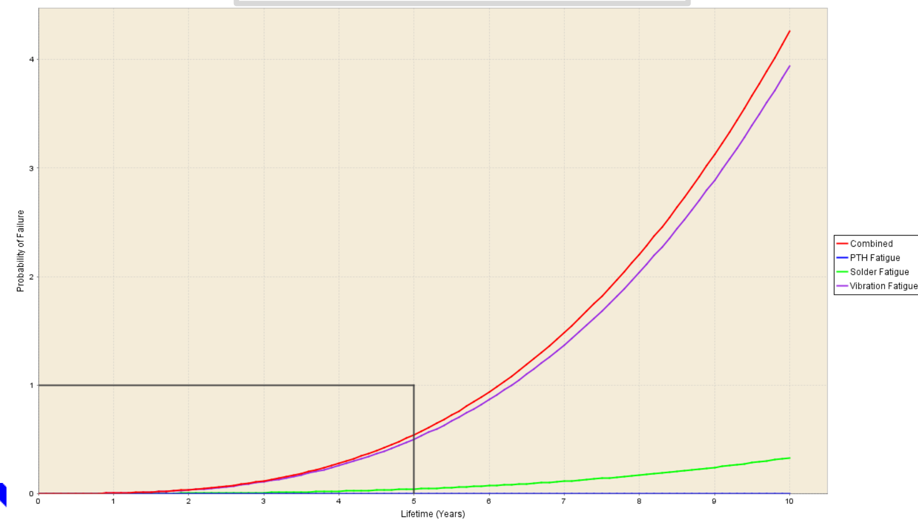
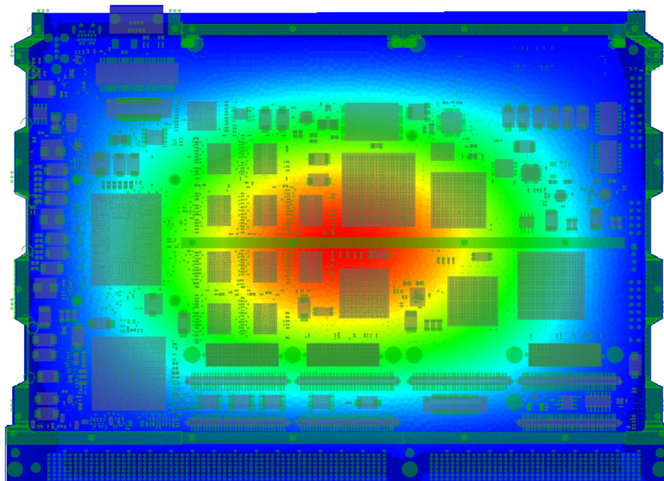
DfR –Software Solutions

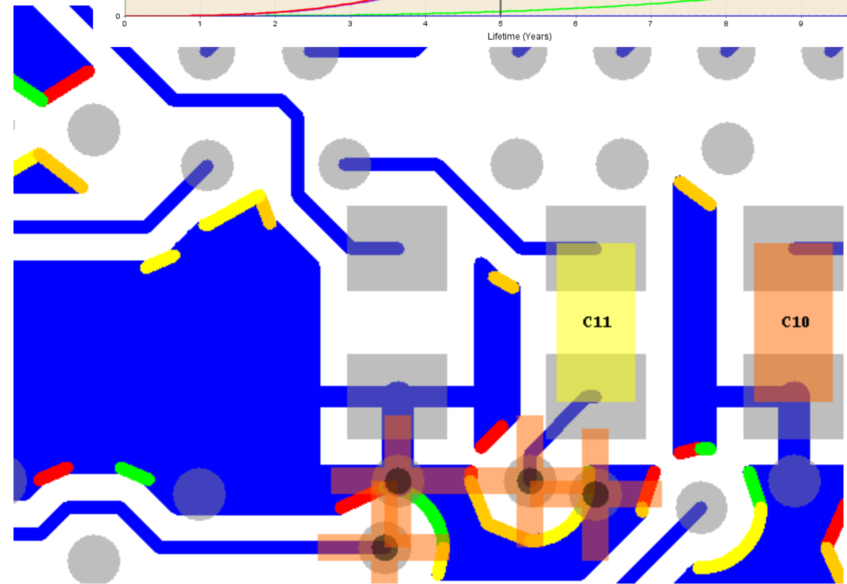
- DfR has developed a revolutionary tool that allows for an early-stage assessment of hardware design
  - Easy-to-use + Comprehensive
  - Identification of high risk design elements
  - Tradeoff analysis
  - Faster time-to-market through guarantee of test success
  - Physics-based reliability prediction
  - Warranty reduction

DfX – A Software Solution







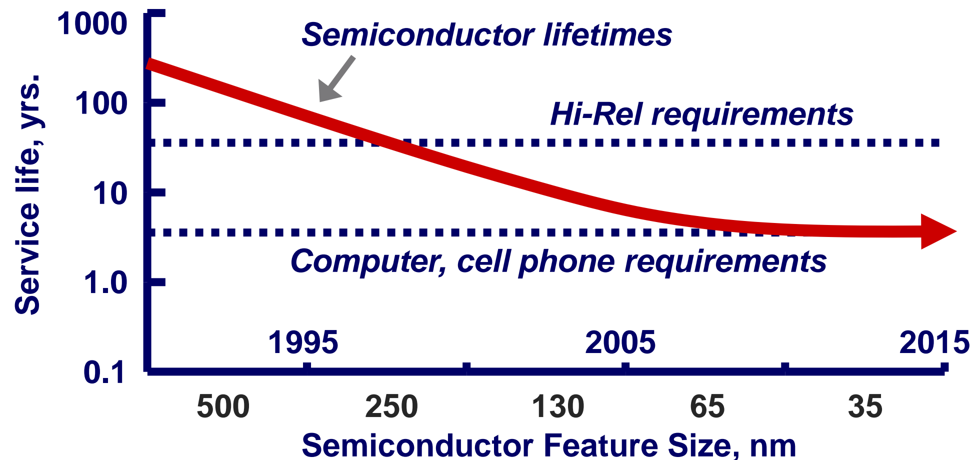


DfR Solutions

Tech Insertion: Integrated Circuit Wearout

"The notion that a transistor ages is a new concept for circuit designers," … aging has traditionally been the bailiwick of engineers who guarantee the transistor will operate for 10 years or so…But as transistors are scaled down further and operated with thinner voltage margins, it's becoming harder to make those guarantees… transistor aging is emerging as a circuit designer's problem.

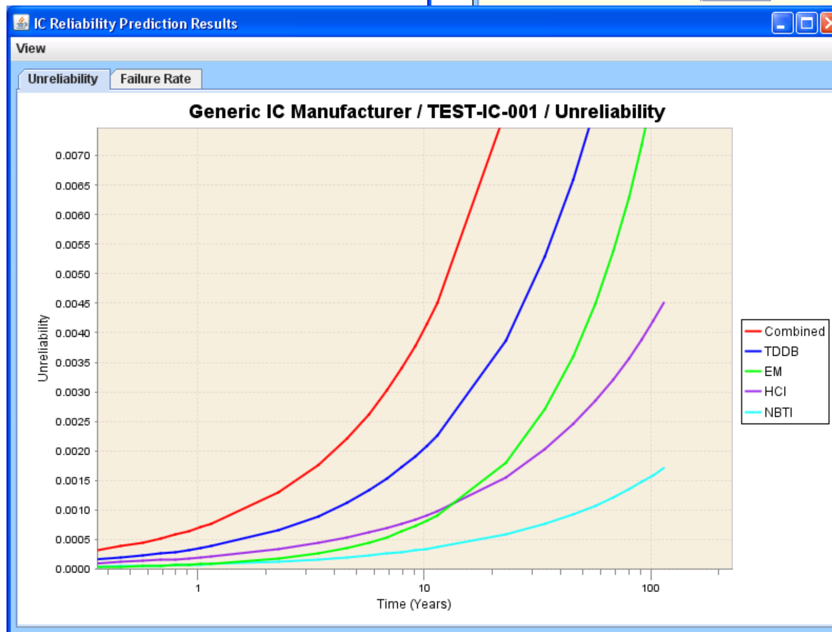
IEEE Spectrum, June 2009



- Working with companies across the electronic supply chain to develop an online solution

IC Wearout – Value Proposition

- Tradeoff studies
- Reliability predictions
- System prognostics and self-healing
- Supplier engagement



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DfR Design Assessment Tool

- Meets current market needs, including
  - Accelerates time-to-market through earlier and more robust analysis
  - Mitigates risk in move to environmentally friendly materials
  - Effectively manages the original design manufacturer (ODM) supply chain
  - Meets new requirements from end-users and regulators for knowledge based assessment

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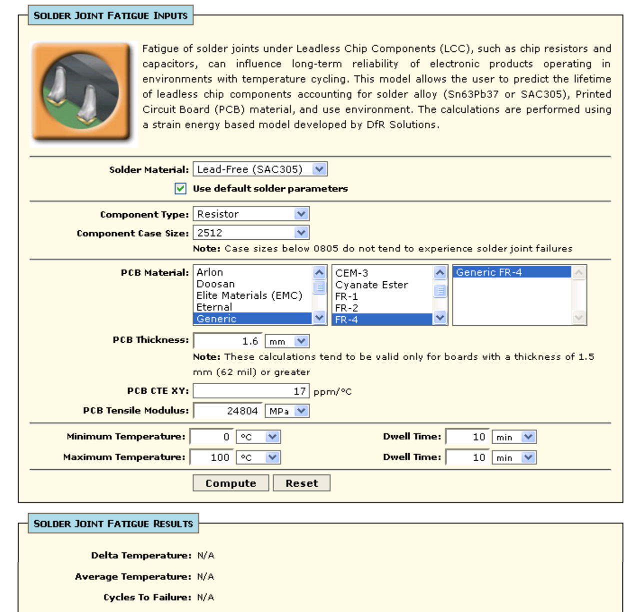
Tech Insertion: 2nd Gen Solder Testing

- Major solder manufacturer needed to demonstrate reliability of 2nd generation Pb-free alloy

Solder Joint Fatigue



- DfR provided a turn-key solution
  - Test plan development
  - Test coupon design
  - Test execution
  - Failure analysis
  - Solder reliability model

- Results
  - Developed new test technology to meet schedule and cost constraints
  - Online calculators now available for customers world-wide

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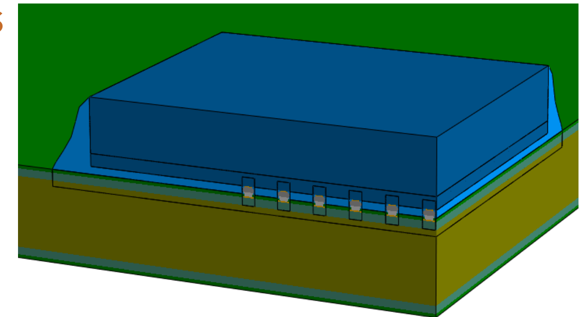
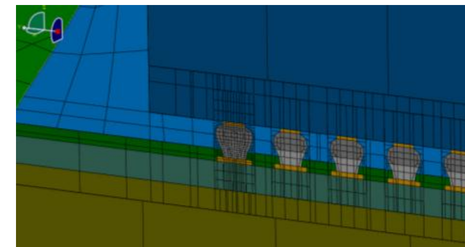
Design: Component Packaging

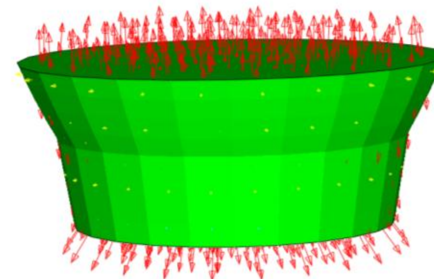
- DfR has assisted numerous component manufacturers and OEMs in ensuring robustness of existing and future packaging solutions



- **Expertise**
  - 1st Level Interconnects (Solder Bumps / Wire Bonds)
  - Underfill Selection and Validation
  - Substrate / RDL
  - Design for Manufacturability (Package Level)
  - Physics of Failure (PoF) Reliability Prediction
  - Finite Element Analysis (FEA)



- **Focus**
  - Flip Chip / Ball Grid Array
  - Bottom Terminated Components
  - Stacked Die / System in Package (SiP)



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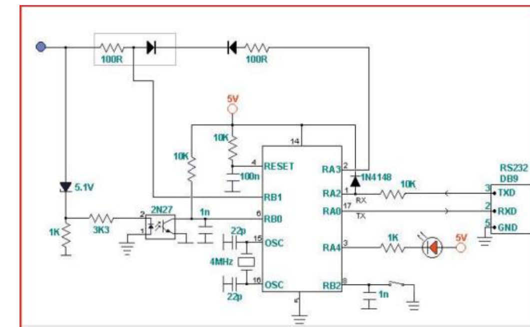
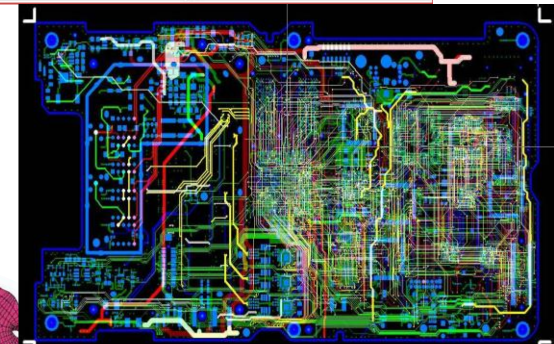
Design: Circuit Board Level

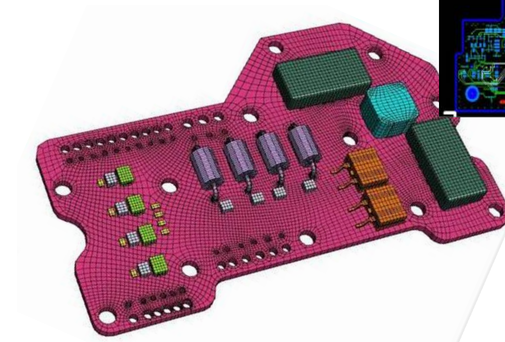
- DfR uses industry-leading design for excellence (DfX) practices to optimize design and ensure success early in new product development (NPD)

  - **Expertise**
    - Circuit Analysis
    - Power Supply Design
    - Design for Reliability
    - Design for Manufacturability
    - Design for Testability
    - Design for Environment
    - Physics of Failure (PoF) Reliability Prediction
    - Finite Element Analysis (FEA)

  - **Focus**
    - Semiconductor Packaging
    - Printed Circuit Board
    - Circuit Card Assemblies
    - Product and System-Level







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Supplier Assessment (Approach)

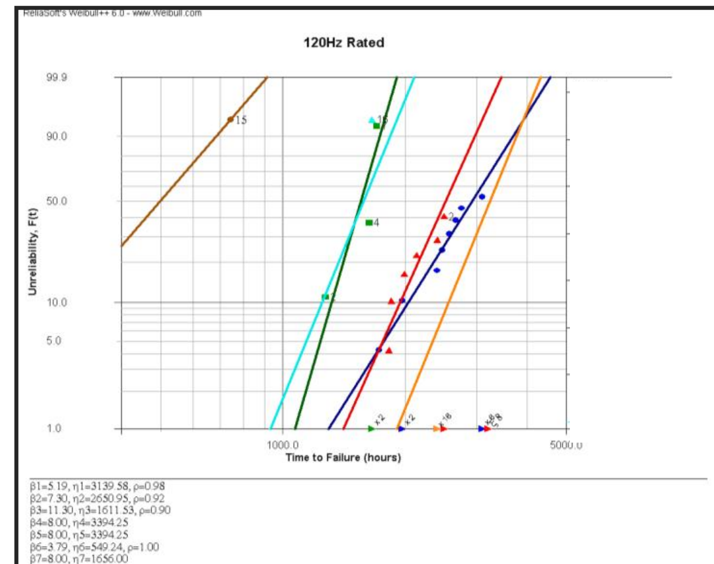
- DfR offers multiple solution paths for ensuring a quality supply chain.
  - Each solution is specifically tailored to each company's production volume, design complexity, and cost requirements

- Approaches include
  - Component-Level Testing
  - Development of Supplier Qualification Documents
  - Supplier Evaluations (Component, Board, Assembly)
  - Construction Analysis
  - Statistical Process Control Evaluations

Supply Chain: Component Qualification

- Working with major electronic OEMs on benchmarking suppliers of critical components

- Actions include
  - Developing test plans
  - Characterizing time to failure behavior
  - Developing qualification criteria based on test results



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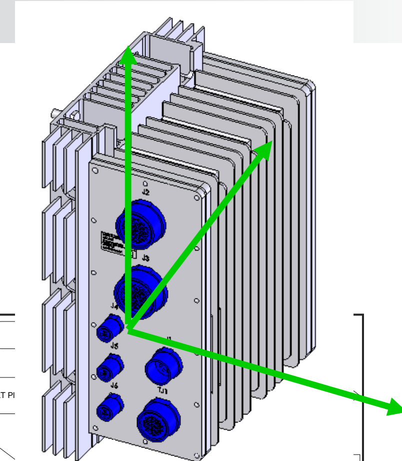
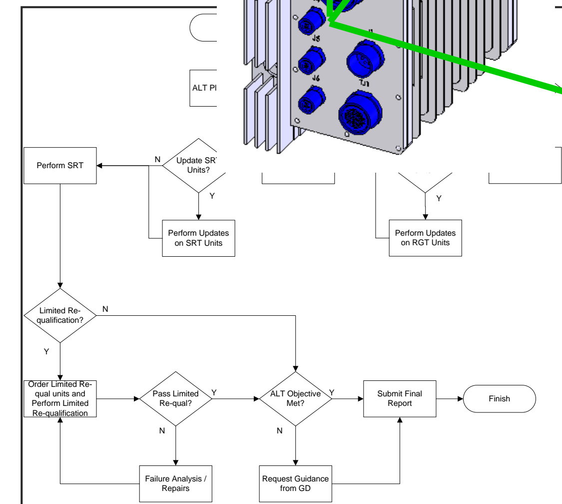
Testing: Test Plan Development

- Product test plans are critical to the success of a new product or technology
  - Stressful enough to identify defects
  - Show correlation to a realistic environment
- DfR Solutions approach
  - Industry Standards + Physics of Failure
- Results in an optimized test plan that is acceptable to management and customers
- Experience in product test plans include
  - Industrial controls
  - Process monitoring
  - Consumer appliances
  - Telecom (Class I, II, and III environments)
  - Personal computers
  - Mobile phones and other mobile products
  - Avionics (engine controls, fuselage)
  - Automotive (under-hood, passenger compartment, chassis, and trunk)
  - Down-hole oil-drilling





Month	Cycles/Year	Ramp	Dwell	Max Temp (ºC)	Min Temp (ºC)	ΔT	Cycles per Day	AF
Jan+Feb+Dec	90	6 hrs	6 hrs	30	5	25	1	12.654
Mar+Nov	60	6 hrs	6 hrs	35	10	25	1	11.799
Apr+Oct	60	6 hrs	6 hrs	40	15	25	1	10.944
May+Sep	60	6 hrs	6 hrs	45	20	25	1	10.26
Jun+Jul+Aug	90	6 hrs	6 hrs	50	25	25	1	9.576
Operational	16.6	5 min	3 hrs	25	-40	65	1	2.223

Root Cause Analysis (RCA) -- Personnel

- The number one requirement in failure analysis
- DfR has all the necessary elements
  - Electrical engineers, mechanical engineers, materials scientists, inorganic chemists, etc.
- Extensive in-house expertise
  - PhD, MS, BS + industry experience
- The right background
  - Over 800 failure analyses combined

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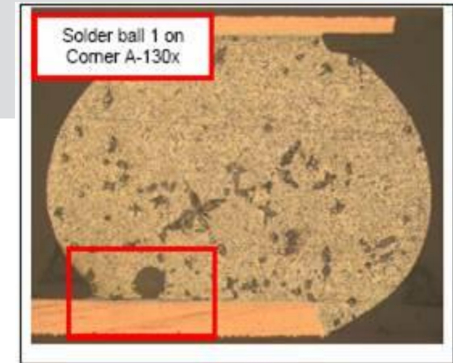
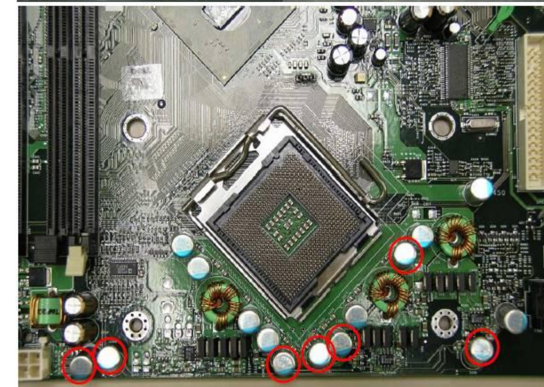
Failure Analysis: Desktop Computer





- Failures during HALT
  - Exposure to vibration
- Electrical testing indicated electrical open
  - Under BGA socket
- Validity of failure mechanism?
  - Shearing of electrolytic capacitor leads
- Dependent upon orientation of capacitors
  - Only those along the board length
- Vibration test may not have applied random loads
  - Potential issues with vibration table or fixturing

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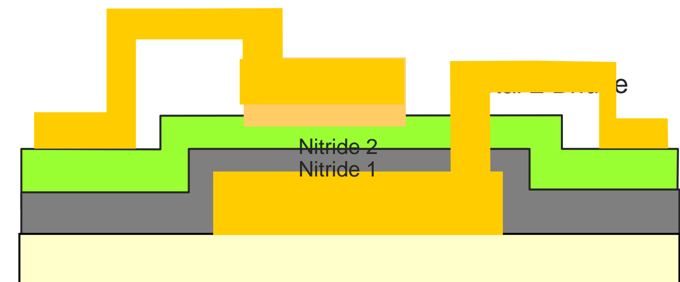
On-Die RCA

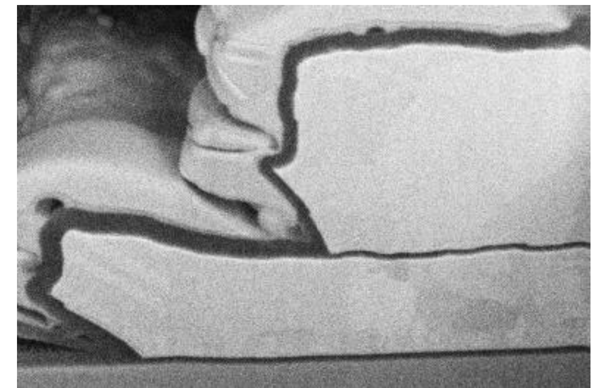
- Wireless and telecom component manufacturer
  - Issues with new silicon nitride technology in MIMCAP structure
  - Halted multi-million dollar product launch

- Identified potential root causes based on
  - Knowledge of semiconductor process technology
  - Fundamental behavior of the material

- Recommended experimental design and analytical techniques to confirm failure mechanism
  - Guided modification in process parameters for fundamentally more robust technology

Standard dual nitride layer MIMCAP





Knowledge and Education (Website)

- Let your staff learn all day / every day

E-LEARNING

- Scholarly articles
- Technical white papers
- Case studies
- Reliability calculators
- Online presentations

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E-LEARNING
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SBIR INFO
US ROHS

Problems Solved. Better Yet — Problems Prevented.

DfR Solutions works with companies and individuals throughout the life cycle of a product, lending a guiding hand that allows you to focus on creativity and ideas. Our expertise in electronics can provide crucial insights and solutions early in product design, throughout manufacturing, and even into the field. **[more...]**

EDUCATION

Featured Articles

- An Experimental Investigation into the Creep Behavior of Pressure Sensitive Adhesive Tapes for Air-cooled Component-Heat Sink Assemblies
- Determining the Lifetime of Silver-filled Isotropic Conductive Adhesive (ICA)/Solder-plated Interconnections
- Has the Electronics Industry Missed the Boat on Pb-free? Failures in Ceramic Capacitors with Pb-free Solder Interconnects
- Improved Methodologies for Identifying Root Cause of Printed Board Failures
- The Kinetics of Formation of Ternary Intermetallic Alloys in Pb-Sn and Cu-Ag-Sn Pb-free Electronic Joints
- **[more...]**

Featured White Papers

- Derating of Schottky Diodes
- Qualifying for Moisture Containing Environments
- Temperature Dependence of Electrical Overstress
- **[more...]**

Featured Case Study

- Identification of BGA Failure
- **[more...]**

UPCOMING EVENTS

- **DfR Solutions on Orange County, CA**
  August 05
  [Click for details...]
- **DfR Solutions in Los Angeles, CA**
  August 11-12
  [Click for details...]
- **DfR Solutions in Southern Wisconsin & Illinois**
  August 25-27
  [Click for details...]
- **DfR Solutions in Huntsville, AL and Atlanta, GA**
  September 15-16
  [Click for details...]
- **Symposium on Defense and Aerospace Electronics**
  Huntsville, AL: September 16

Our Clients

eywell Applied Data Systems

Read our May/June Newsletter!

DfR Solutions, in collaboration with BestTest and IPC, will hold the first ever Design for Excellence (DfX) Course in October 2009. This collaborative effort will provide tools on how to meet time-to-market deadlines and reduce warranty issues. For more information, please click here.

Dr. Craig Hillman's Webinar presentation "Root-Cause Analysis in the HALT Process" part of the series *Ask the Experts* hosted by the Qualmark Corporation, is now available on our website! To access the presentation, please click here.

DfR Solutions welcomes Cheryl Tulkoff, CRE, as New Senior Member of Technical Staff. To read more, please click here.

WHAT WE DO

Field/Customer Returns
Technology Insertion
Design
Testing Product Qualification
Supply Chain

Field/Customer Returns

How can you keep your products from being returned? Any return from the customer, regardless of cause, should be considered a failure. DfR has the resources to perform extensive failure analyses and to make recommendations regarding the products that remain in the field. Our expertise with lifetime prediction and statistical analysis all add to the finished report, providing a complete picture to our clients about their product.
[more...]

Technology Insertion

How disruptive does technology have to be? DfR assists companies with their transition into using new technologies and materials. DfR's expert consulting and testing services allow companies to efficiently shift their structure with minimal risk.
[more...]

Design

Will your product meet expectations? DfR has the resources to answer questions that arise during the

Interested?

- Could your next product benefit from DfR's extensive expertise and PoF knowledge base?
  - Bring us in as an independent party during critical design reviews
- Are your concerned with new technologies?
  - DfR's scientists and engineers can provide comprehensive analysis to ensure risk-minimization during these difficult transitions
- Take advantage of our unique Open-Door policy!
  - See how much we already know about your current issues
  - Chances are we have already solved your problem at least once before
  - We work around the clock and around the world
  - Contact us by phone (301-474-0607) or email (askdfr@dfrsolutions.com)

DfR Solutions