

The Effect of Coating and Potting on the Reliability of QFN Devices

Cheryl Tulkoff and Dr. Nathan Blattau

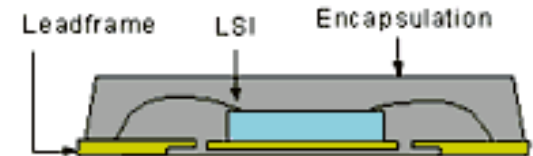
QFN: What is it?

- **Quad Flat Pack No Lead or Quad Flat Non-Leaded**

- ‘The poor man’s ball grid array’

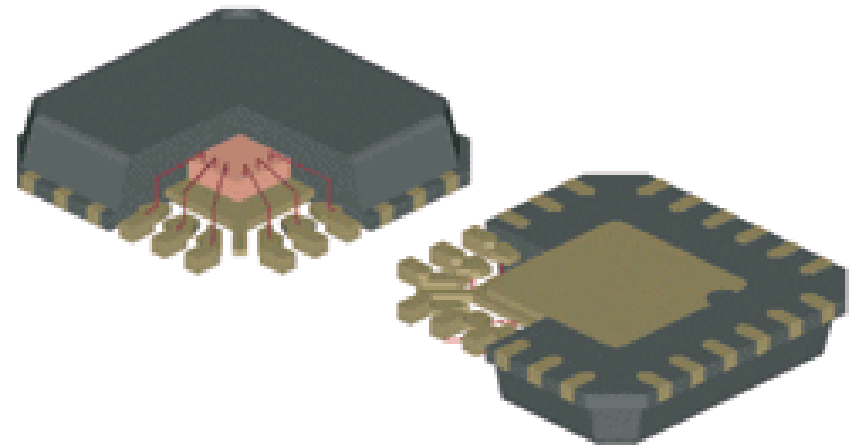
- Also known as

- Leadframe Chip Scale Package (LF-CSP)
- MicroLeadFrame (MLF)
- Others (MLP, LPCC, QLP, HVQFN, etc.)



- **Overmolded leadframe with bond pads exposed on the bottom and arranged along the periphery of the package**

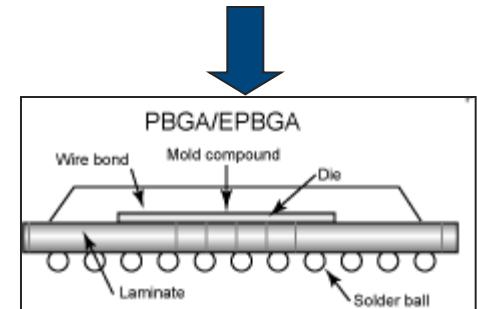
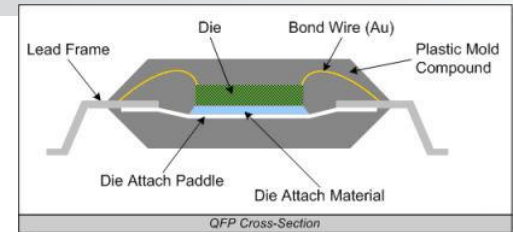
- Developed in the early to mid-1990’s by Motorola, Toshiba, Amkor, etc.
- Standardized by JEDEC/EIAJ in late-1990’s
- Fastest growing package type



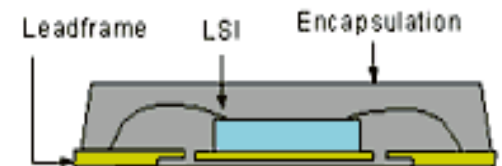
Quad Flat No-Leads (QFN)

- **Elimination of leads**
 - Provides lower resistance
 - Lower inductance
 - Higher performance
 - Higher package densities
- **Tradeoffs**
 - Increased power density
 - Manufacturability
 - More susceptible to thermal mechanical fatigue

QFP: >10,000



BGA: 3,000 to 8,000



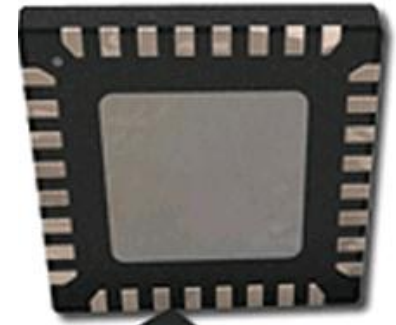
QFN: 1,000 to 3,000

Cycles to failure
-40 to 125C

DfR Solutions

Advantages: Thermal Performance

- More direct thermal path with larger area
 - Die → Die Attach → Thermal Pad → Solder → Board Bond Pad
- θ_{Ja} for the QFN is about half of a leaded counterpart (as per JESD-51)
 - Allows for 2X increase in power dissipation



Package Type	Body Size (mm)	Leads	Height (mm)	Max Die Size	PCB Area	θ_{Ja}
QFN	7 x 7	48	1.00 max	203 x 203 mils	49 mm ²	27
TQFP	7 x 7	48	1.20 max	190 x 190 mils	81 mm ²	55
QFN	5 x 7	38	1.00 max	124 x 202 mils	35 mm ²	34
TSSOP	4.4 x 9.7	38	1.10 max	108 x 207 mils	62 mm ²	73
QFN	5 x 5	16	1.00 max	124 x 124 mils	25 mm ²	37
QSOP	3.9 x 4.9	16	1.75 max	86 x 120 mils	31 mm ²	112

Advantages: Inductance

- At higher operating frequencies, inductance of the gold wire and long lead-frame traces will affect performance
- Inductance of QFN is half its leaded counterpart because it eliminates gullwing leads and shortens wire lengths

**Popular for
RF Designs**

Table 1. Comparison of inductance components for a QFN and SOIC.

Package	Inductance (nH)	
	QFN 7 mm, 48 Lead	TQFP 7 mm, 48 Lead
Die size	4.5 x 4.5 mm	4.25 x 4.25 mm
Center lead	0.067	0.871
Center wire	0.867	0.837
Center total (lead + wire)	0.934	1.708
Corner lead	0.085	1.010
Corner wire	1.081	0.964
Corner total (lead + wire)	1.166	1.974

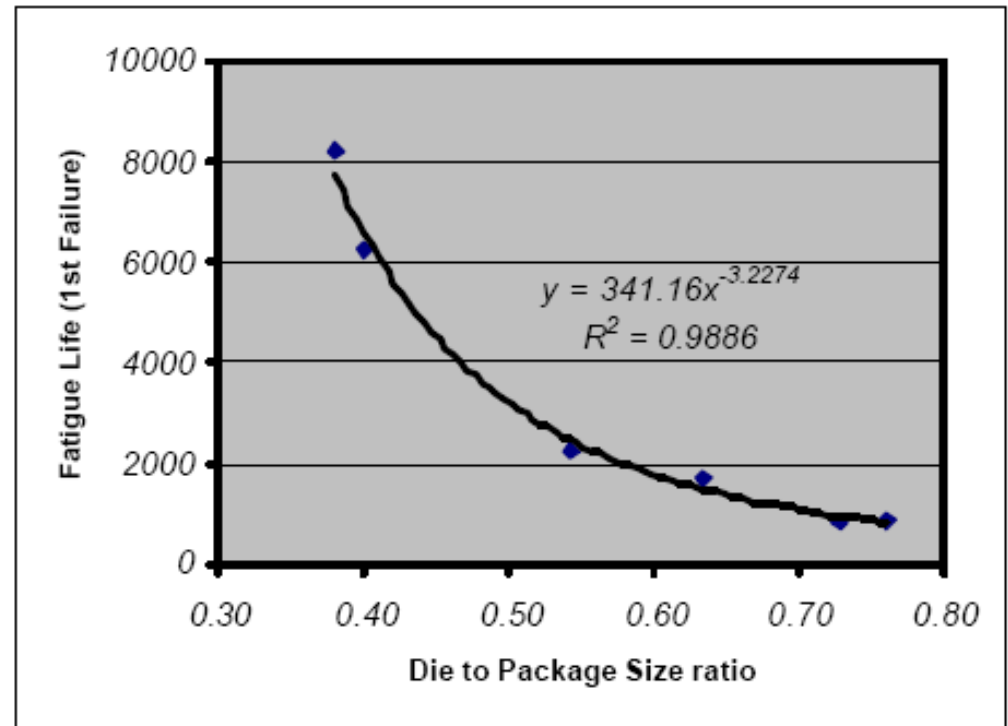
http://ap.pennnet.com/display_article/153955/36/ARTCL/none/none/1/The-back-end-process:-Step-9-QFN-Singulation/

Disadvantage: Thermal Mechanical Fatigue (Solder)

- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)

Does the increased susceptibility of QFN devices make them more sensitive to conformal coating and potting effects

BOARD LEVEL ASSEMBLY AND RELIABILITY
CONSIDERATIONS FOR QFN TYPE PACKAGES,
Ahmer Syed and WonJoon Kang, Amkor Technology.

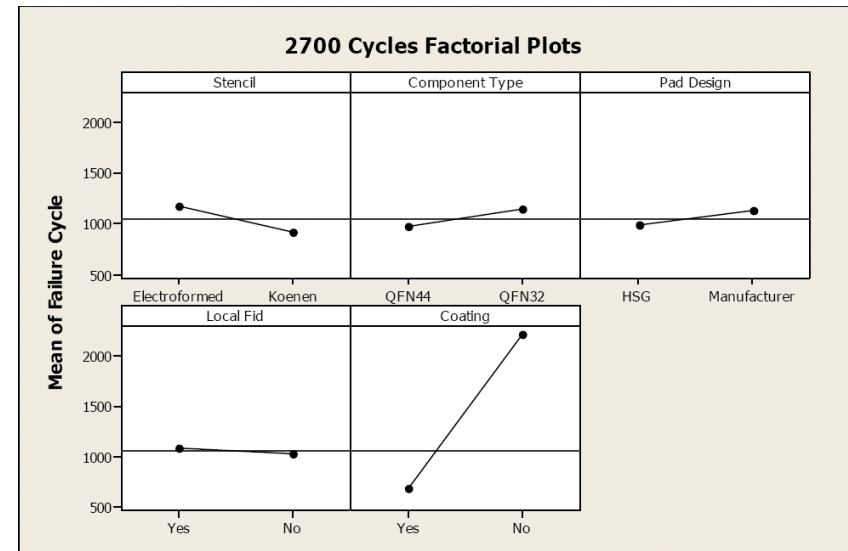


Rules of Thumb

- The use of underfills, potting compounds and thick conformal coatings can greatly influence the failure behavior under thermal cycling
 - Anytime a material goes through its glass transition temperature problems tend to occur
 - Conformal coating should not bridge between the PCB and the component
 - Underfills designed for enhancing shock robustness do not tend to enhance thermal cycling robustness
 - Potting materials can cause PCB warpage and tensile stresses on electronic packages that greatly reduce time to failure

Thermal Cycling: Conformal Coating

- Care must be taken when using conformal coating over QFN
 - Coating can infiltrate under the QFN
 - Small standoff height allows coating to cause lift
- Hamilton Sundstrand found a significant reduction in time to failure (-55 / 125C)
 - Uncoated: 2000 to 2500 cycles
 - Coated: 300 to 700 cycles
- Also driven by solder joint sensitivity to tensile stresses
 - Damage evolution is far higher than for shear stresses



Wrightson, SMTA Pan Pac 2007

Conformal Coating Properties (Glass Transition Temperature)

- Why did conformal coating effect thermal cycling performance?
- Verification and determination of mechanical properties
 - Elastic Modulus as a function of temperature
 - Glass Transition Temperature
 - Coefficient of Thermal Expansion

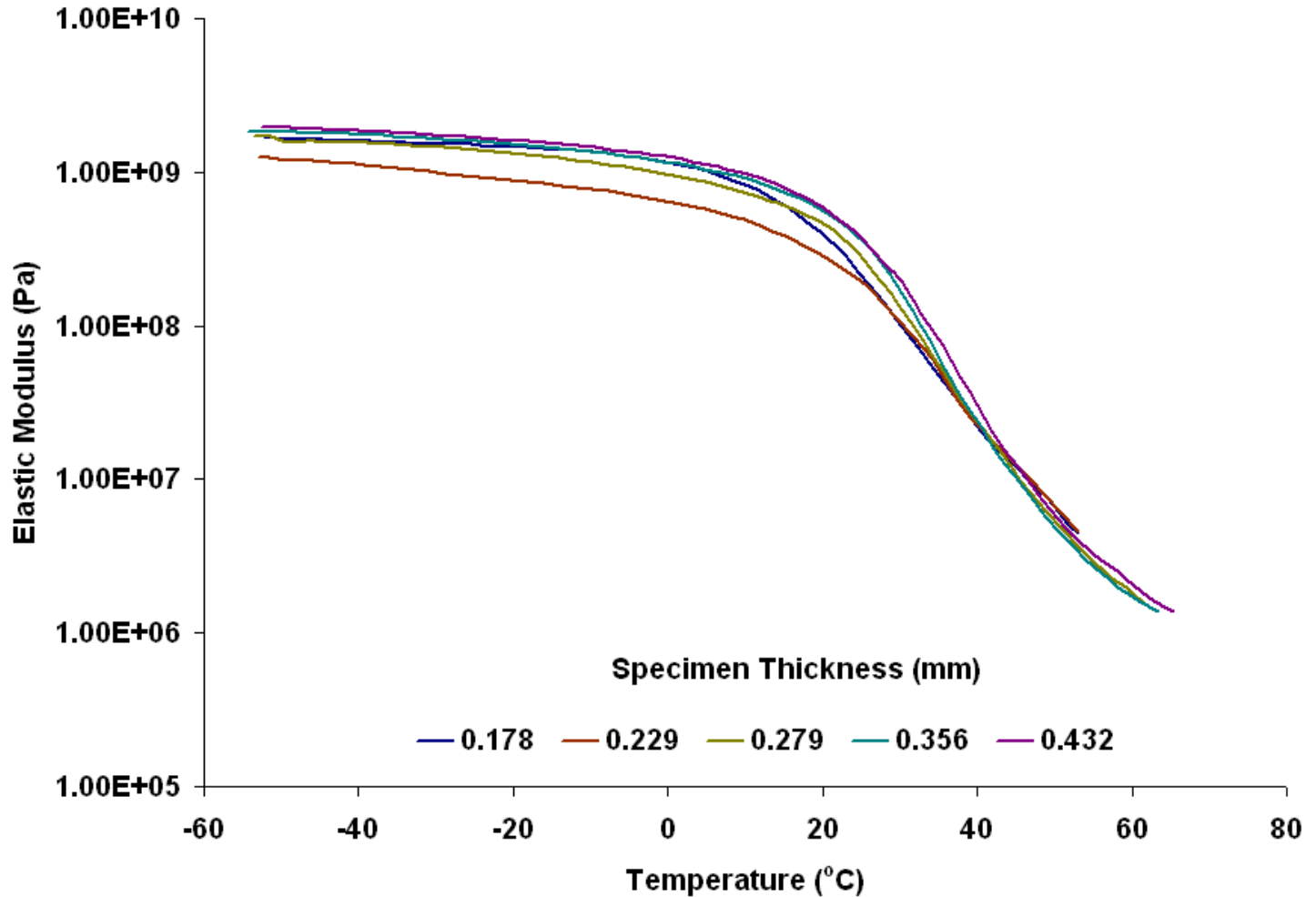
Physical	Continuous Use Temp. Range °C	-65 +125
	Thermal Shock Test ⁷	Passes
	Flammability ⁸ (self extinguishing)	Yes
	TCE in/in/°C ⁹	5.5 x 10 ⁻⁶
	Young's Modulus ¹⁰ psi	1260
	Tg °C ¹¹	15
Electrical	Dielectric Constant ¹²	2.5
	Dissipation Factor ¹³	.01
	Dielectric Withstand ¹⁴ (volts)	>1,500
	Insulation Resistance ¹⁵ (teraohms)	800
	Moisture Resistance ¹⁶ (gigaohms)	60

Young's Modulus
Datasheet 1260 psi (8.7 MPa)

Coefficient of thermal Expansion
Datasheet 55 ppm/°C

Elastic Modulus – DMA - Tensile

Acrylic
conformal
coating

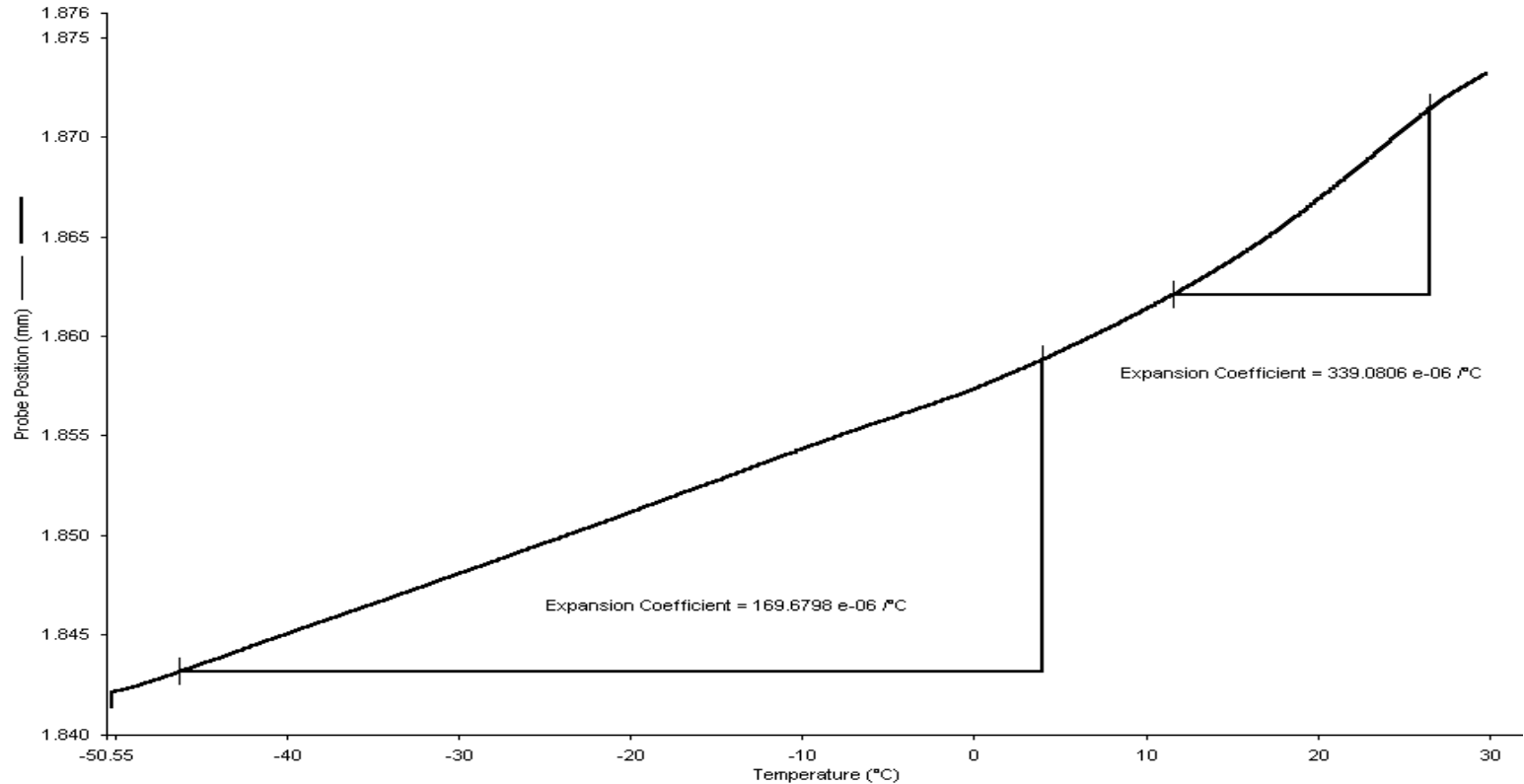


Datasheet - Specification (8.7 MPa, 1260 psi), $T_g = 15^\circ\text{C}$

DfR Solutions

Coefficient of Thermal Expansion - TMA

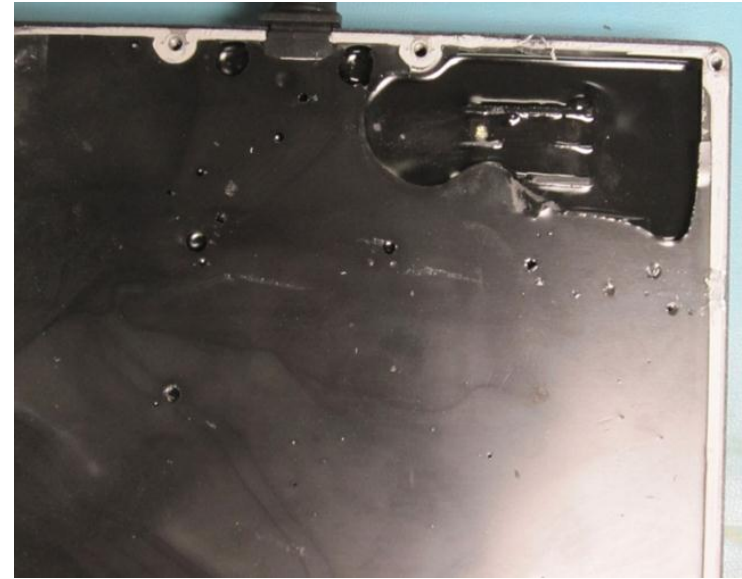
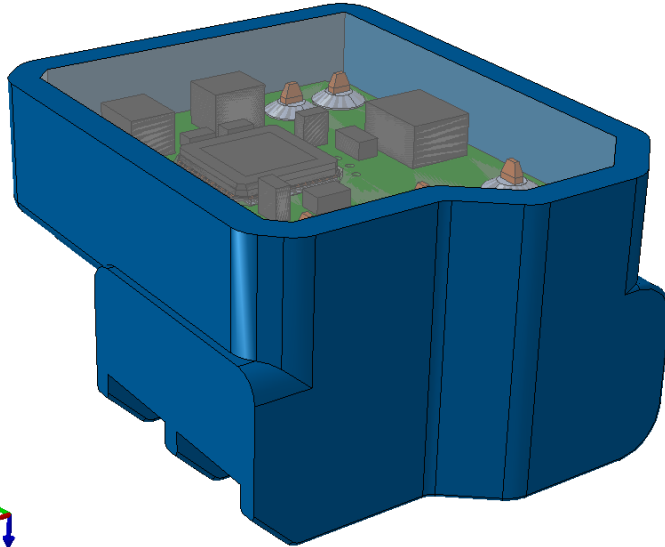
Acrylic conformal coating



Below Tg CTE – 170 ppm/°C
Above Tg : CTE – 340 ppm/°C

Glass Transition Temperature
Tg ≈ 5 to 15°C

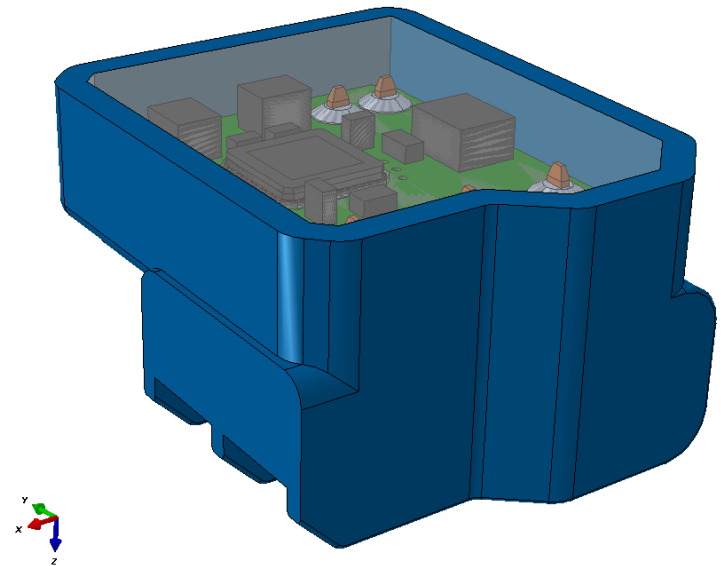
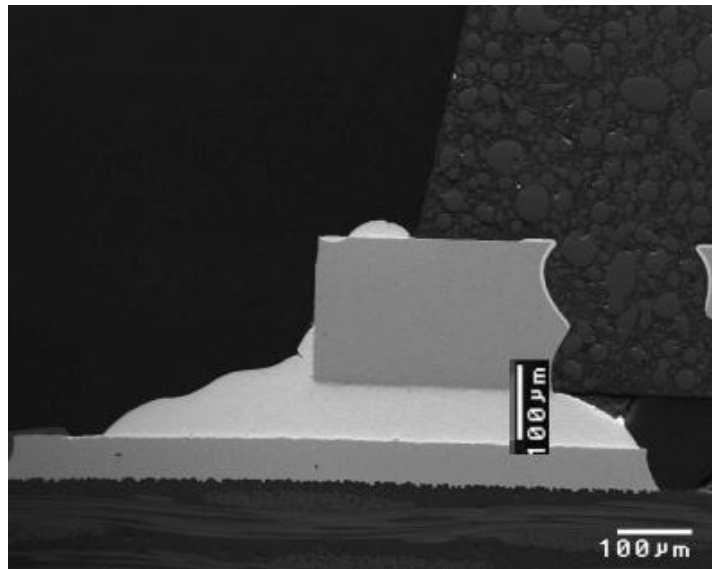
Potting



- Ideally the CTE of the potting should be as close to the CCA as possible
 - Usually in the 20 to 30 ppm/°C
 - The larger the CTE, the more compliant the potting must be to limit the stresses imparted to the CCA
 - Potting should generate hydrostatic pressure (equal on all sides) of the circuit card
 - This prevents warping of the CCA as the potting expands
 - Excessive warping will greatly reduce time to failure
 - May cause overstress failures.
 - This may require modification to the housing
 - Housing may need to be relatively stiff

Rigid Housing with Free Surface

- QFN failures occurring very rapidly during temperature cycling with urethane based potting material
- All units were failed at the 100 cycle inspection (-40 to 105C)
- Good quality joints with sufficient solder thickness



DFR SOLUTIONS

Material Properties

Potting Compound

Isotropic Material

$$CTE_{x,y} = 120 \text{ ppm}$$

Significant increase in modulus or stiffness below with high CTE

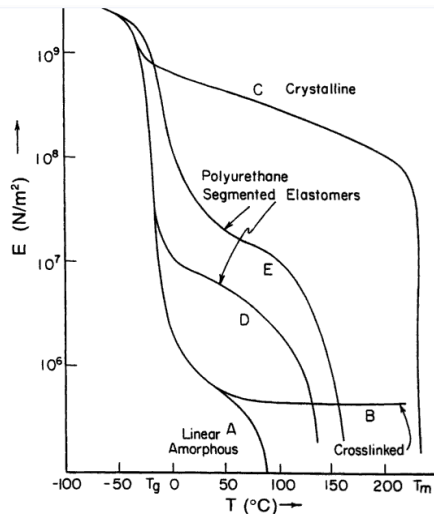
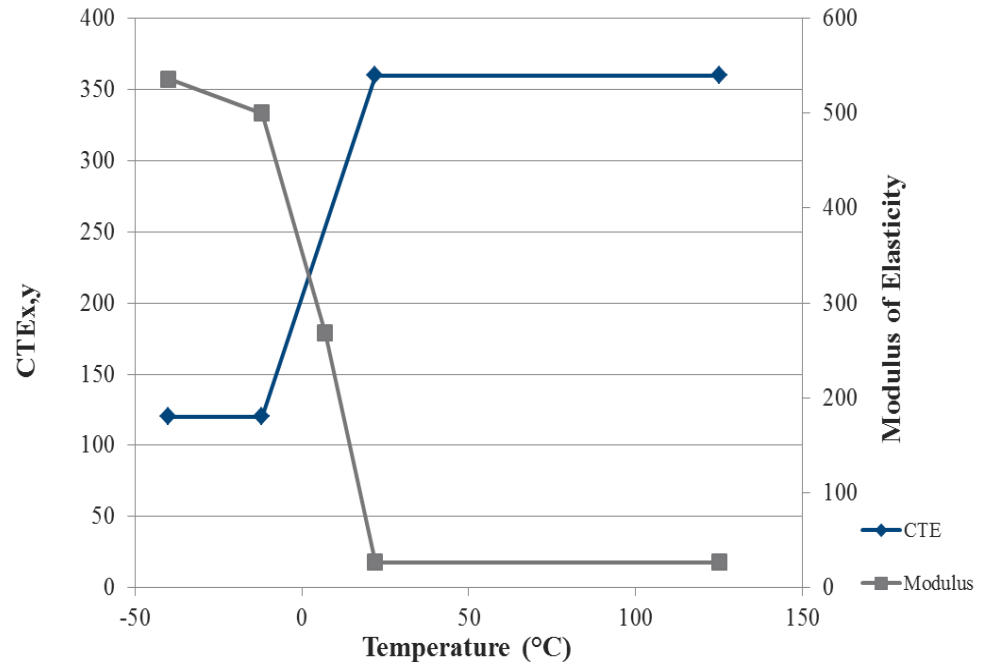
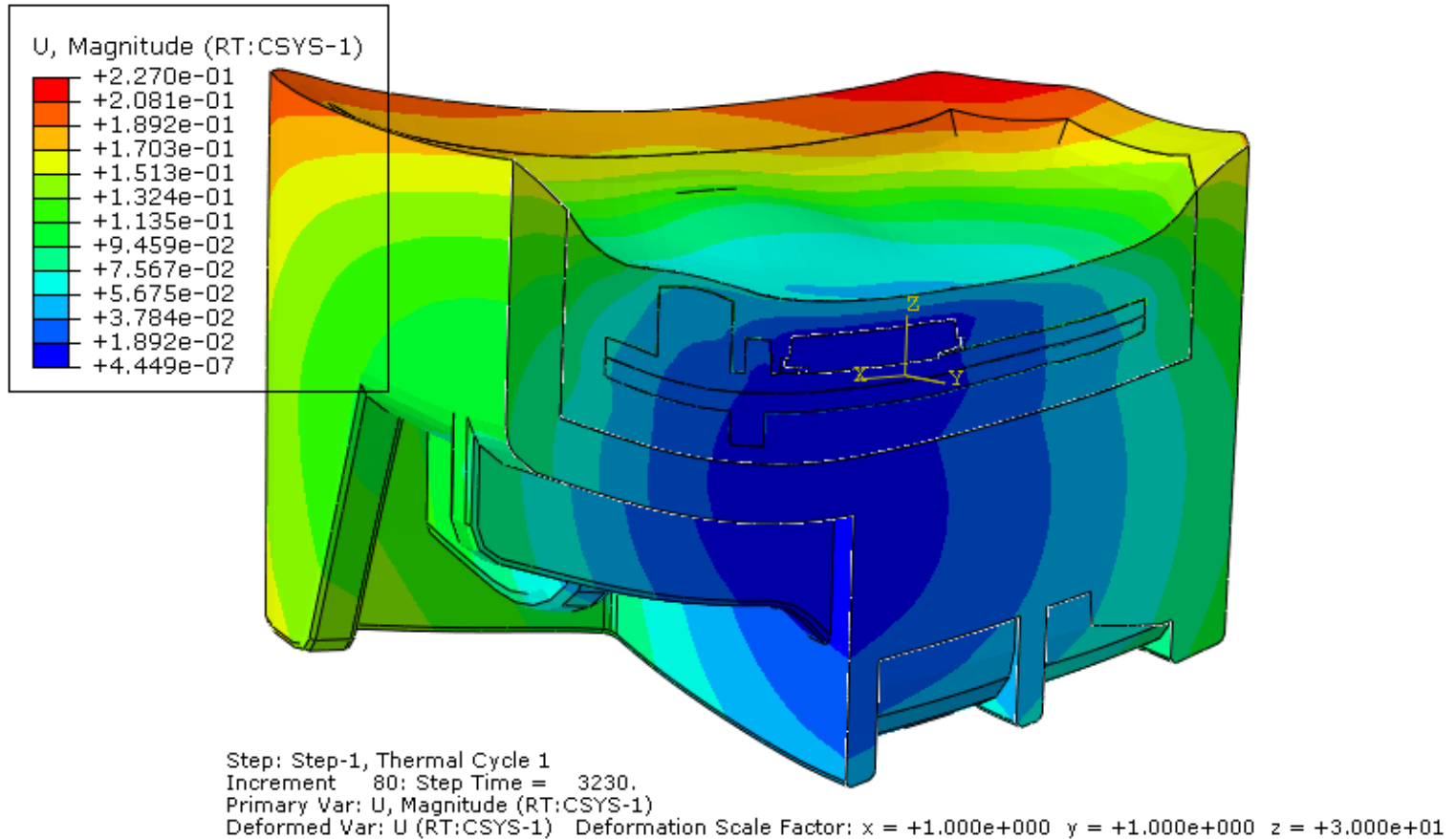


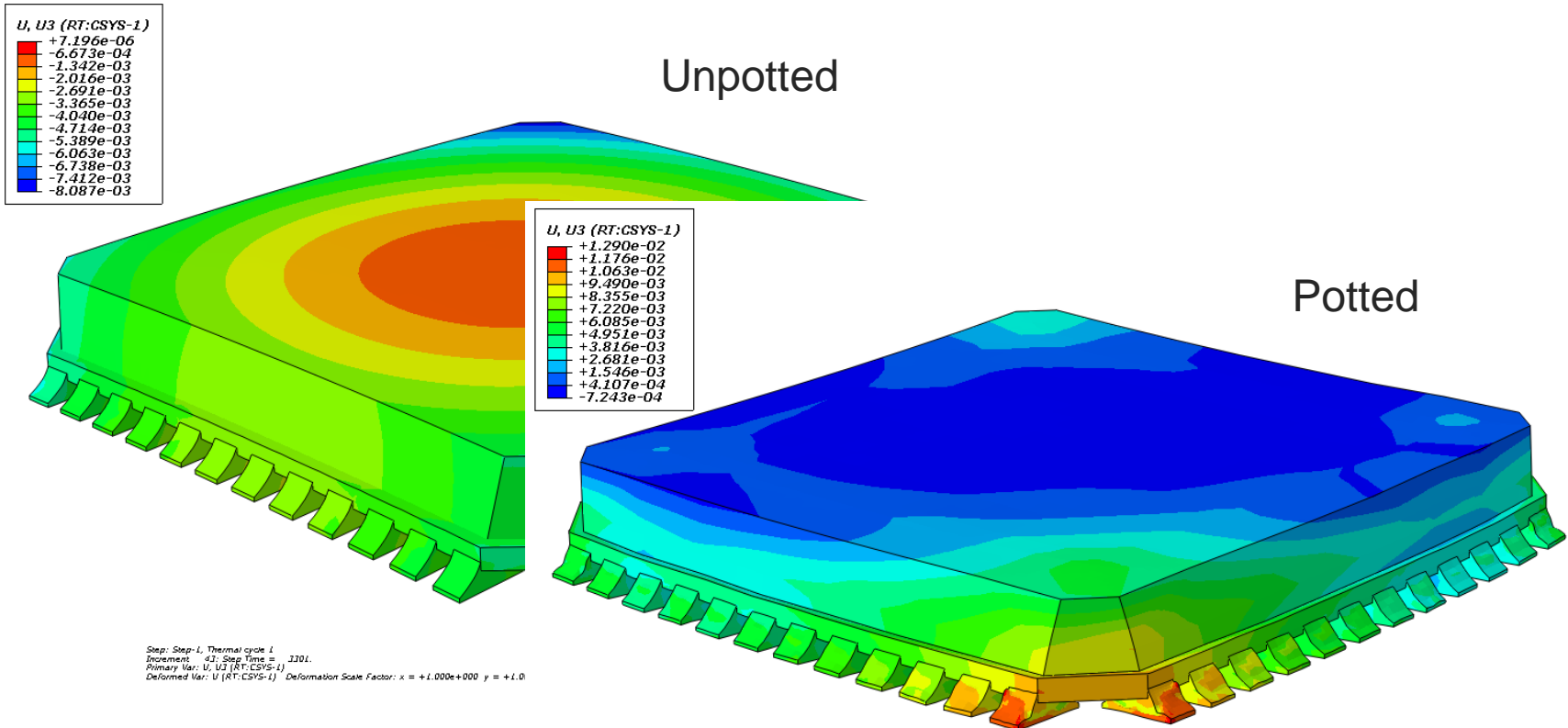
FIGURE 22 Storage modulus v temperature curves for (A) linear amorphous polymer, (B) crosslinked polymer, (C) semicrystalline polymer, (D) MDI/BD/PTMA segmented polyurethane (32% MDI by weight), (E) MDI/BD/PTMA segmented polyurethane (38% MDI by weight). From Cooper S.L. and Tobolsky A.V.J. *Appl. Polym. Sci.*, 10:1837, Copyright 1966. Reprinted with permission by John Wiley & Sons.



PCB Warpage due to Potting Shrinkage



QFN Warpage



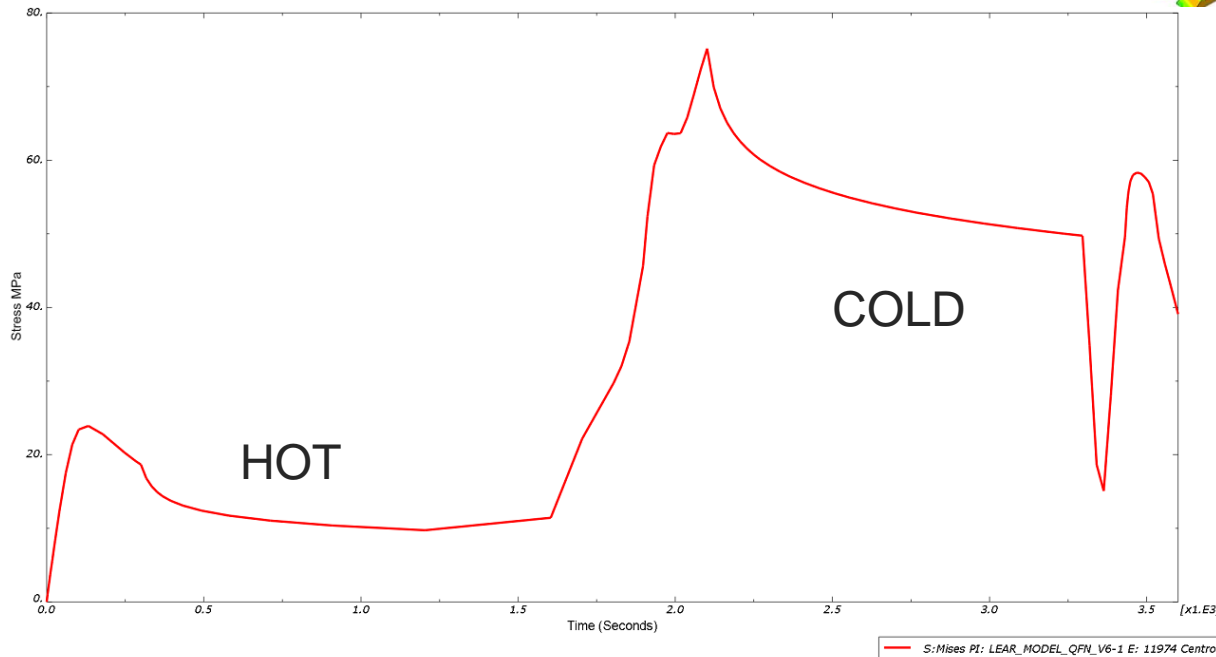
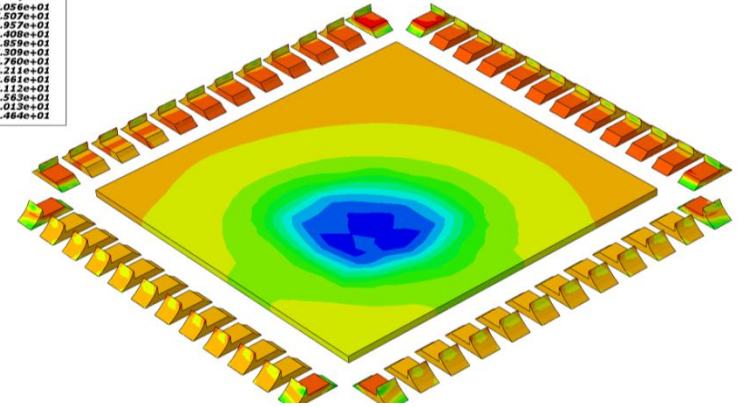
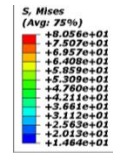
Step: Step-1, Thermal cycle 1
Increment: 43, Step Time = 3301.
Primary Var: U, U3 (RT:CSYS-1)
Deformed Var: U (RT:CSYS-1) Deformation Scale Factor: x = +1.000e+000 y = +1.0

Step: Step-1, Thermal Cycle 1
Increment: 73, Step Time = 3226.
Primary Var: U, U3 (RT:CSYS-1)
Deformed Var: U (RT:CSYS-1) Deformation Scale Factor: x = +1.000e+000 y = +1.000e+000 z = +2.000e+01

Order of magnitude higher deformation and deformation concentrated over corner solder joints

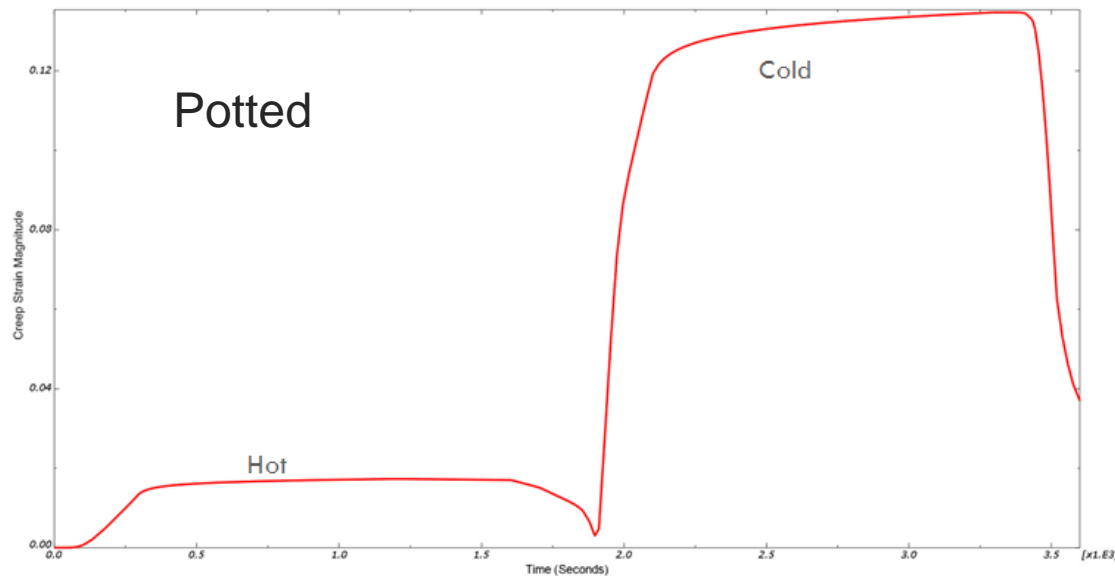
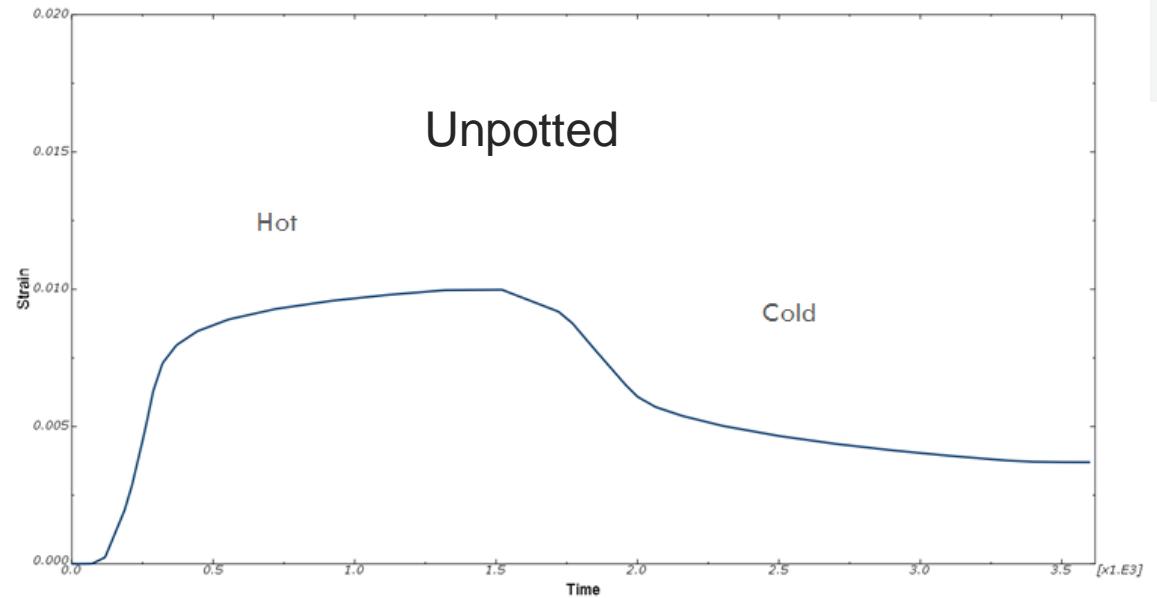
Solder Stresses

- Very high stresses during cold dwell of thermal cycle



Creep Strains

- The higher the creep strains the shorter the time to failure



- Excessive creep occurring at cold temperature
- More energy required to cause cold temperature creep (more damaging)

Conclusions

- The lack of a compliant lead structure makes QFN devices more susceptible to PCB warpage related failures
- Mechanical properties of the potting material
 - Glass transition temperature (T_g)
 - Modulus should be specified above and below the T_g
 - CTE should be specified above and below the T_g
- The design of the housing
 - May provide a surface to which the potting material can pull against when shrinking causing PCB warpage
 - Should be designed to provide as close to a hydrostatic pressure as possible (equal pressure on all sides)