Reliability Challenges of Flat No Lead (FNL) ICs in Automotive Electronics

James McLeish
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Reliability Workshop
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Introduction

- DfR Solutions is an Laboratory Services, Engineering Consulting & CAE software firm.
  - Formed by senior scientists from the University of Maryland’s DoD/NSF Sponsored Consortium for developing the Physics-of-Failure approach to achieving Ultra Reliability & Total Product Integrity for E/E Technology
    - Quality, Reliability and Durability (QRD) and Failure Analysis of electronics:
      - The Sherlock ADA Durability Simulation Reliability Assessment CAE Program
      - Advanced Accelerated Testing
      - E/E Component Robustness & Supply-Chain Selection and Management

- James McLeish - Michigan Office Manager DfR Solutions -Rochester Hills, Michigan (jmcleish@dfrsolutions.com)
  - 35 Years of Vehicular, Military & Industrial Product Engineering Experience
    - E/E Product Design, Development, Systems Enrg & Production (Chrysler & GM)
      - Help Invent 1st Microprocessor Engine Controller (1979-82 Chrysler ESA/EFC System)
      - 3 Patents Automotive Electronic Control Systems
      - E/E Engineering Manager - GM Military Vehicle
      - GM E/E Reliability Manager & QRD Technical Expert
      - Manager GM Reliability Physics (Advance QRD, A/D/V & Test Technology Development)
      - Author/Co-author of 3 GM Reliability/Validation Test Standards (Including GMW-3172)
      - SAE Reliability & ISO-26262 Functional Safety Committees
Automotive Electronics Technology Has Constantly & Rapidly Evolved
Each New Technology Has Experienced QRD Challenges the Auto Industry had to Adapt to
The Evolution to Flat No Lead ICs is Now Well Under Way.

Single Sided Then Thru-hole
DIP Integrated Circuits
1970 ‘s- Today
~4 up to 68 I/O, 1” x 3.5”
Up to 10 Meg Hz Speeds.

1st Generation Quad Surface Mount
J Lead PLCC, 1982 - Today
~6 Up to 160 I/O, 1.5 in sq.,
Up to 100 Meg Hz Speeds
Source of Many Reliability Problems.

2nd Generation Quad Surface Mount
Fine Pitch Gull Wing I.C, 1993 - Today
~54 Up to 450 I/O, 1.75 in sq
Up to 250 Meg Hz Speeds
>10 Time the Life of J Lead in Auto ECMs.

Bump & Ball Grid Arrays
Leadless Attachments
1996 - Today
~24 - 1000 I/O  1.2 in. sq
500+ 1000 Meg Hz Speeds.
Life Varies Greatly w/Size & Conf.

Flat No Lead Chip Scale Packaging (FNL-CSP)
(QFN, DFN, MLF, SON)
2002 - Today
~8 - 480 I/O, .75 in SQ
Gigi Hz Speeds
Can have significantly reduces life
What is it a Flat No Lead (FNL) IC Package?

- Leadless, Near Chip Scale, Surface Mount, Plastic Encapsulated Integrated Circuit Packages.
- One of the fastest growing IC package type, replacing other package, increasing used in automotive EE modules
- Proliferation of more advanced FNL package styles
  - MLF - Micro-Lead Frame
  - BTC - Bottom Termination Components
  - LPCC - Leadless Plastic Chip Carrier
  - SON - Small Outline Non-leaded Package
  - LF-CSP - Lead-Frame Chip Scale Package (LF-CSP)
  - DFN/QFN - (.9-1mm) Dual/Quad Flat No-Lead
  - TDFN/TQFN - (.75mm) Thin Dual/Quad Flat No-Lead
  - XDFN/XQFN - (.35-.45mm) Extremely Thin DFN or QFN
  - DR/MR-QFN – Dual/Multi Row Flat No Lead
Why Flat No Lead (FNL) IC Packages?

- Developed in the 1990’s by Motorola, Amkor Toshiba, standardized by JEDEC/EIAJ to be smaller and have better electrical performance than leaded IC packages & be a low cost alternative to Laminate Plastic Over-molded BGAs

- Wire bonded lead frame mounting of the IC Die is lower cost than designing & fabricating a custom flexible interposer PCB

- Do not require expensive solder ball attachments

- Many Electrical & PCB Layout Advantages
  - Smaller, lighter & thinner than comparable packages
  - Shorter connection path reduces impedance provides superior electrical signal integrity performance & operation at higher speeds
  - Lead frame thermal flag pad provides good thermal performance
Why Flat No Lead (FNL) IC Packages?

- FNL ICs help make ultra thin and light portable consumer electronic products possible.
  - Products with a short service life (2-5 years)
  - In a relative benign environment

- The vastly large size of the consumer electronics market provides significance power to influence IC suppliers to develop IC packages & products that meet their needs and priorities.

- With significantly less market influence the high reliability, harsh environment, long life market segments like the auto industry must increasingly learn to use and adapt to the components produced by the predominate market trends.

Introducing ThinkPad X300

The art of thin

The no-compromise, ultra portable, 13.3" widescreen notebook with an optional integrated DVD drive and 3 USB ports, starting at just 2.9 lb. Everything else is just hot air.
Flat No Lead (FNL) IC Package Construction

- **Two Configurations.**
  - **Wire Bonded Version - Provides Better Thermal Performance**
    - IC die is attached to a copper lead frame that also services as the thermal pad
    - Die is wire bonded to the bottom termination pads along the package’s periphery
    - Package is plastic encapsulated
    - Excess lead frame is either sawed or punched off (Results in an Exposed Copper stub)
  
  - **Flip Chip Version – Lower Cost & Provides Better Electrical Performance**
    - Flip Chip solder bump are directly soldered to the lead frame (Eliminates the cost and added impedance of the wire bonds)
    - Package is plastic encapsulated
    - Excess lead frame is either sawed or punched off (Results in an Exposed Copper stub)
Flat No Lead (FNL) IC Package – PCB Assembly & Quality Issues

- Smaller & easier to handle.
  - Good co-planarality
  - Less susceptible to lead bending or ball handling damage
  - Easier to place correctly on PCB pads than leaded IC.
  - Larger pad geometry simplifies solder paste printing
  - Less prone to bridging short defects
  - Reduced pop corning moisture sensitivity issues

- More difficult to inspect and rework (similar to BGAs).
  - X-Ray inspection is essential

- Flux residues can be trapped under the device, harder to clean
  - More susceptibility to dendritic growth electro-chemical migration short circuits

- Susceptible to board flexure handling damage
  - With SAC lead free solder potential of damage can start at only 500 microstrain
  - Flexure damage may occur during
    - In Circuit Test (ICT), board depanelization, connector insertion, manual assembly
    - While operating - shock, vibration or thermal cycling related PCB warpage.
Without a flexible terminal lead to absorb thermal Expansion/Contract motions, a high amount of thermal expansion stress is applied to the low profile under body solder joints, which accelerate solder fatigue failure.

**Solder Attachment Cycles to Failure**
- Order of magnitude (10X) reduction from QFPs
- 3X reduction from BGAs

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Typical Thermal Cycles to Failure ((-40°C to 125°C))</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFP</td>
<td>&gt;10,000</td>
</tr>
<tr>
<td>BGA</td>
<td>3,000 – 8,000</td>
</tr>
<tr>
<td>QFN</td>
<td>1,000-3,000</td>
</tr>
</tbody>
</table>

*TTCL = Typical Thermal Cycle Life \(-40°C to +125°C\)
Flat No Lead (FNL) IC Package Reliability: Thermal Cycling

Reasons for Shorter Solder Attachment Thermal Cycling Fatigue Life

- **Driven by die to package ratio**
  - 40% die; MCL = 8K cycles (-40 / 125°C)
  - 75% die; MCL = 800 cycles (-40 / 125°C)
- **Due to Component to PCB CTE Difference**
  - CTE FR4 PCB ~ 13-17 ppm/°C
  - CTE Encapsulates ~ 8-15 ppm/°C
  - CTE IC Silicon Die ~ 2.6 ppm/°C
- **Exasperated larger package sizes & #I/O pads**
  - 44 I/O; MTCL = 1500 cycles (-40 / 125°C)
  - 56 I/O; MTCL = 1000 cycles (-40 / 125°C)
Flat No Lead (FNL) IC Package Reliability: Solder Joints

- In addition to thin packages FNL’s IC were also designed to have low profile solder joints (goal is 2-3 mils of post-reflow solder thickness).
  - Originally intended for thin and lightweight portable consumer electronics.

- A low profile solder joint results in high CTE mismatch expansion/contraction shearing stresses which also accelerate fatigue.

Wasted solder force out from under the FNL IC by excessive placement force. Produces an even thinner joint.
Flat No Lead (FNL) IC Package Reliability: Solder Fillets

- FNL’s ICs may not have effective structural side wall fillets to augment the thin under body solder joint (can add 25-50% to fatigue life)
  - Exposed lead frame tip (when present) is bare, unfinished oxidized copper
    - Result of the punched or sawed lead frame removal process
  - Solder does not readily bond to unfinished oxidized copper,
  - Flux in no clean solder paste may be too weak to deoxidize the copper.
- There are efforts to develop FNL ICs with finished termination ends
  - Ask you IC suppliers if this is an option

Solder force out by excessive placement may look like a fillet, but may not bond well to end terminations

Example of a castellated solder joint side wall filet on a Leadless Chip Carrier (LCC) package
Flat No Lead (FNL) IC Package Reliability: Solder Joints

- Why Do FNL Land Patterns Extend PCB Pads 0.2 – 0.3 mm beyond package footprint
  - Helps makes solder observable for visual inspection
  - But solder may or may not be bonded to cut edge
  - If proper amount of paste disposition is achieved may reducing solder joint height to provide a visual inspection indicator that in reality is may be inappropriate for this type of package.

- X-ray Inspection is better for FNL, essential for most accurate results, (Similar to BGAs)
  - Allows for verification of bridging, adequate solder coverage and void percentage
  - Cannot detect fractures or head in pillow defects
Flat No Lead IC Package Reliability: Conformal Coating Issues

- Care must be taken when using conformal coating with LNCSPs
  - Coating can infiltrate under the LNCSPs
  - Small standoff height allows coating to cause lift
- Can produce a significant reduction in time to failure (-55 / 125°C)
  - Uncoated: 2000 to 2500 cycles
  - Coated: 300 to 700 cycles
- Also driven by solder joint sensitivity to tensile stresses
  - Damage accumulation from z axis tensile lifting stress is far higher than for x-y shearing stress

Solder Fatigue DoE Results
Ref: Wrightson, SMTA Pan Pac 2007
Flat No Lead (FNL) IC Package Reliability: Risk Mitigation
- Validation Durability Testing

- Reliability Note from Freescale Semiconductor:
  QFN/ uDFN Application Notes #AN1902- Rev. 4.0, 9/2008
  “For high reliability applications, Freescale recommends evaluating the uDFN/QFN package on a case by case basis. This applies to all lead count & package sizes.”

- IC manufacturers validate FNLs to JEDEC JESD22 series A+B
  - Focuses on die, packaging & internal 1st-level interconnections (wire bond, solder bump, etc.), not 2nd level PCB Interconnects

- Auto OEM EE Module Validation Durability Testing requires at least 12-16 Weeks
  - Risk of late program disruption failure requiring failure analysis & corrective action
  - Extra costs and program delays

1) Design  →  2) Build  →  3) Test

DESIGN - BUILD - TEST - FIX (D-B-T-F)

4) Faults Detected?
   No
   Yes

5) Fix Whatever Breaks.

6) REPEAT 3-5 Until Nothing Else Breaks Or You Run Out Of Time/Money.
Flat No Lead (FNL) IC Package Reliability: Risk Mitigation
- Validation Durability Testing – Other Resources

- IPC-9701A “Performance Test Methods & Qualification Requirements for Surface Mount Solder Attachments”
- Industry / Application Specific Thermal Cycling Profile.

### Table 3-1: Product Categories and Worst-Case Use Environments for Surface Mounted Electronics (For Reference Only)

<table>
<thead>
<tr>
<th>Product Category (Typical Application)</th>
<th>Temperature, °C / °F</th>
<th>Worst-Case Use Environment</th>
<th>Typical service years</th>
<th>Approx. Accept. Failure Risk, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consumer</td>
<td>-40/85 0/55 0/32 60/140 35/63</td>
<td>12 365 1-3 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Computers and Peripherals</td>
<td>-40/85 0/55 0/32 60/140 20/36</td>
<td>2 1460 5 0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Telecomm</td>
<td>-40/85 -40/40 85/185 35/63</td>
<td>12 365 7-20 0.01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Commercial Aircraft</td>
<td>-40/85 -55/-67 95/203 20/36</td>
<td>12 365 20 0.001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial and Automotive - Passenger Compartment</td>
<td>-55/150 -40/85 -55/-67 95/203</td>
<td>20/36 185 10-15 0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military (ground and shipboard)</td>
<td>-40/85 -40/85 -55/-67 95/203 40/72 &amp; 60/108 &amp; 80/144</td>
<td>12 100 10-20 0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Space</td>
<td>-40/85 -40/85 -55/-67 95/203 3/5.4</td>
<td>12 8760 5-30 0.001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military Aircraft</td>
<td>-55/125 -40/85 -55/-67 125/257 40/72</td>
<td>2 100 10-20 0.01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maintenance</td>
<td>-55/150 -40/125 -55/-67 125/257 60/108 &amp; 100/180 &amp; 140/252</td>
<td>2 1000 10-15 0.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* & = in addition
1. All categories may be exposed to a process temperature range of 18°C to 260°C (64°F to 500°F).
2. Tmin and Tmax are the operational (test) minimum and maximum temperatures, respectively, and do not determine the maximum ΔT.
3. ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the temperature range, ΔT, is not the difference between Tmin and Tmax; ΔT is typically significantly less.
4. The dwell time, t(d), is the time available for the creep of the solder joints during each temperature half-cycle.
Flat No Lead (FNL) IC Package Reliability: Risk Mitigation
- Physics of Failure – CAE Durability Simulations

- PoF Models for Stress-Stain Structural Analysis of Electronics are well proved.
- But creating custom FEA models of EE modules is not easy:
  - Time Consuming & Expensive
  - Shortage of PoF CAE modelers.
  - Structural analysis CAE resources are not deployed to EE Enrg. Depts.
Application Specific Customized CAE Solutions.

An emerging trend where auto guided, specific function, CAE Apps or analysis templates are created

- Provides a common, reusable semi-automated interface
  - Perform regularly needed product optimization modeling
  - Solving frequently encountered problems.
  - Allows product teams to perform expert level CAE analysis without a rare, high cost PoF CAE expert

To see full article: [http://www.sae.org/mags/SVE/10767](http://www.sae.org/mags/SVE/10767)
Sherlock is a Semi-Automated CAE App program for Physics of Failure durability simulations & reliability assessment of electronic equipment.

Sherlock is the backbone to one of the most powerful reliability tools to be released for use not just by the reliability group, but by the entire engineering design and management team. Sherlock is the future of Automated Design Analysis (ADA), the integration of design rules, best practices and a return to a physics based understanding of product reliability.

It is not at the Iphone or Droid App store. But yes there is now a Physics of Failure Durability Simulation App.
The 4 Steps of a Sherlock PoF Analysis

1) **Design Capture** - provides the detailed inputs to the modeling software and calculation tools.

2) **Life-Cycle Characterization** - define the reliability/durability objectives and expected environmental & usage conditions (Field or Test) under which the device is required to operate.

3) **Load Transformation** – auto create Finite Element Analysis to calculate and distribute the environmental and operational loads across a circuit board to the individual parts.

4) **PoF Durability Simulation/Reliability Analysis & Risk Assessment** – Performs a design and application specific durability simulation to calculates life expectations, reliability distributions & prioritizes risks by applying PoF algorithms to the virtual PCBA model created in steps 1, 2 & 3.
Create CAE virtual model from standard circuit board CAD/CAM design files (Gerber / ODB Format)
1) Design Capture - Define PCB Laminate & Layers to Calculate

Calculates:
- Thickness
- Density
- CTE x-y
- CTE z
- Modulus x-y
- Modulus z

From the material properties of each layer

Using the Built in Laminate Data Library

Stackup Properties

The following board properties are based on the currently defined board outline and the individual layer properties shown below:

- **Board Size:** 193 x 115 mm [7.6 x 4.5 in]
- **Board Thickness:** 1.8 mm [69.0 mil]
- **Board Density:** 2.6833 g/cc
- **Copper Layers:** 4
- **CTE x:** 13.576 ppm/C
- **CTE y:** 57.310 ppm/C
- **Exy:** 37,972 MPa
- **Ez:** 4,094 MPa

Stackup Layers

Double click any row to edit the properties for that layer or select one or more rows and press the Edit Selected button below to edit properties for a batch of layers. Press the Generate Stackup Layers button to replace all layers using a given PCB thickness and default layer properties.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>Material</th>
<th>Thickness</th>
<th>Density (g/cc)</th>
<th>CTE x (ppm/C)</th>
<th>CTE y (ppm/C)</th>
<th>Exy (MPa)</th>
<th>Ez (MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIGNAL</td>
<td>COPPER (50%)</td>
<td>0.2 oz</td>
<td>2.0</td>
<td>17,600</td>
<td>17,600</td>
<td>113,000</td>
<td>113,000</td>
</tr>
<tr>
<td>2</td>
<td>Laminate</td>
<td>FR408</td>
<td>1.93 mil</td>
<td>1.900</td>
<td>13,000</td>
<td>65,000</td>
<td>23,442</td>
<td>3,450</td>
</tr>
<tr>
<td>3</td>
<td>POWER</td>
<td>COPPER (90%)</td>
<td>0.2 oz</td>
<td>8.1760</td>
<td>17,600</td>
<td>17,600</td>
<td>113,000</td>
<td>113,000</td>
</tr>
<tr>
<td>4</td>
<td>Laminate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>POWER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Laminate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>7</td>
<td>SIGNAL</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Edit Selected Layers

Enter values for each layer property.

- **Laminate Material:** FR4
- **Laminate Thickness:** 19.3 mil

![Edit Selected Layers Dialog](image)
2) Define Environments

- Handles very complex environmental or test stress profiles
3) Load Transformation
Automated FEA Mesh Creation for Calculating Stress Distribution Across the PCBA & to Each Component

- **Automatic Mesh Generation**
  - Days of FEA modeling and calculations, executed in minutes
  - Without a FEA modeling expert.
4) PoF Durability/Reliability Risk Assessment

Thermal Cycling Solder Fatigue

- N50 fatigue life calculated for each of 705 components (68 unique part types), with risk color coding, prioritized risk listing and life distribution plots based on known part type failure distributions (analysis performed in <30 seconds) after model created.
  - Red - Significant portion of failure distribution within service life or test duration.
  - Yellow - Lesser portion of failure distribution within service life or test duration.
  - Green - Failure distribution well beyond service life or test duration.

(Note: N50 life - # of thermal cycles where fatigue of 50% of the parts are expected to fail)

Parts With Low Fatigue Endurance Found In Initial Design
~84% Failure Projection Within Service Life, Starting at ~3.8 years.
Identification of specific reliability/durability limits or deficiencies, of specific parts in, specific applications, enables the design to be revised with more suitable/robust parts that will meet reliability/durability objectives.

Reliability plot of the same project after fatigue susceptible parts replaced with electrically equivalent parts in component package suitable for the application.

Life time failure risks reduced from ~84% to ~1.5%
- Thermal Cycling Solder Attachment Fatigue Life
- Thermal Cycling PCB PTH Via Barrel Cracking Fatigue Life
- Vibration Solder Fatigue Life
- Shock Solder Fracture Life
- Conductive Anodic Filament Risk Assessment
- ISO-26262 Functional Safety FMEA and Metric Generation
5) PoF Durability Simulations/Reliability Risk Life Curves for Each Failure Mechanism Talled to Produce a Combined Life Curve for the Entire Module.

- Detailed Design and Application Specific PoF Life Curves are Far More Useful that a simple single point MTBF (Mean Time Between Failure) estimate.
An AEC Reliability Improvement Proposal.

- Consider an AEC requirement to identify and list in data sheets the x, y, & z axis CTE of EE components, as measured by:
  - Thermal Mechanical Analysis (TMA) or
  - Digital Image Correlation (DIC)

- Would provide value information for product teams/designers to evaluate the degree of CTE mismatch between components and circuit boards.
Thank you!

For Further Questions?

Contact: jmcleish@dfrsolutions.com

or visit www.dfrsolutions.com