

## Reliability Results for a Wire Bondable Tape Ball Grid Array Package

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### ABSTRACT

This paper reviews a new wire bondable tape ball grid array package which exhibits a cost/performance advantage in the industry. This novel package architecture utilizes the fine line capability of flexible circuitry to provide the high performance and reliability required by the increasingly advanced IC's of today and tomorrow. This TBGA is designed to provide excellent heat dissipation through use of a heat spreader to which the die is directly adhered. Heat is therefore efficiently dissipated into surrounding air and into the mother board. With the capability for less than 50 $\mu$ m lines and spaces, the wire bond fingers can be moved in very close to the die thus minimizing the wire bond length and allowing the possibility for die shrink. The resulting decrease in inductance enables packaging of high speed devices. This product can be provided at a competitive price partially due to 3M's efficient process for simultaneous chemical etching of holes in the polyimide substrate to define solder ball pads. This paper includes an overview of this package as well as detailed results of package coplanarity and board level reliability testing. Extrapolations are performed to estimate life in actual use conditions. These results show ample reliability for most applications.

### KEYWORDS

tape ball grid array, reliability, electrical and thermal characteristics, wire bonding

### INTRODUCTION

Ball grid array packages continue to prove themselves to be the package of choice for pin counts above 208 due to their high performance and low defect levels at board assembly compared with high pin count QFPs<sup>1</sup>. Their excellent fit into the existing infrastructure has enabled them to compete on a cost basis as well. With this being the case, the next issue which die manufacturers must address is - what type of BGA will best meet the requirements of a particular device? Although package cost is always a major consideration for most die, better electrical and thermal performance are becoming increasingly important as die grow more sophisticated. Not only must the die manufacturer choose between plastic, tape, and ceramic BGAs, they must also choose amongst the various BGA configurations within each of these groups. A recent Tech Search International publication reported on 13 different tape ball grid array configurations alone<sup>2</sup>. This paper will

address one of these architectures to discuss its electrical and thermal performance and demonstrate its excellent reliability through thermal cycle testing and life predictions.

### Product Configuration and Characteristics

The TBGA carrier being offered is in response to the market need for a lower cost TBGA which allows the wire bonding of a die. Since about 97% of die are currently wire bonded, this vast infrastructure is already in place in the assembly industry. These TBGA carriers are supplied in a strip format similar to a leadframe or PBGA which allows assemblers to easily utilize their existing infrastructure for both die attach and solder ball attach. A representative carrier strip made up of four 35mm 352i/o units is shown in Figure 1. The following Figure is a cross section schematic of a completed TBGA. This structure provides excellent thermal characteristics, since the backside of the die is directly adhered to the metal stiffener/heat spreader. The thin adhesive layer (1-2 mils) between the circuit and stiffener allows a great deal of heat to be dissipated from the stiffener, through the solder balls, and into the circuit board. This is a significant advantage since it enables all the solder balls to act as thermal vias as opposed to only those under the die as with standard PBGAs. As a result, up to 90% of the heat can be dissipated through the board. This is an especially attractive attribute for applications involving confined space such as portable computers. In addition, this spreading of the heat over the whole package may allow more uniform heating of the board beneath the package, thus limiting any warpage that may occur in packages with thermal vias beneath the die only. Uniform heating would also be an advantage during rework by minimizing board damage during the removal and replacement of the package.

The use of microflex circuitry in fabrication of a TBGA offers a number of advantages over other substrate types. One major advantage is the finer pitch capability. 50 $\mu$ m lines and spaces are standard with microflex circuitry (improving to 25 $\mu$ m lines and spaces in the near future) while 75 $\mu$ m lines and spaces are a significant challenge with PCBs and therefore demand a price premium. This fine line capability provides an important advantage in that it allows the wire bond fingers to be brought in very close to the die thereby minimizing the inductance of the wire. A typical 1 mil diameter wire exhibits a self inductance of

1nH for every 1 mm of length<sup>3</sup>. By reducing wire lengths from as much as 5 mm for some PBGAs down to 1.2 mm (demonstrated with this TBGA), 3.8 nH of inductance is eliminated from the signal, a significant amount for high speed devices. The typical limit for wire bond capability is a 90um flat on the bond finger with 50um space. Therefore flex circuitry offers the extendibility necessary as wire bond capabilities continue to improve.

The ability to position the wire bond fingers closer to the die also enables the die manufacturers to continue to shrink the die size while keeping the wire lengths reasonably short. Die are increasingly becoming pad limited as conductor line widths fall to 0.35um and below. Shrinking the die enables more die per wafer which is quite attractive since it reduces the unit cost of each die.

Microflex circuitry can also offer a cost advantage over PCBs in construction of a BGA. Microflex is fabricated in a roll to roll fashion and is therefore economically attractive at moderate to high volumes. This cost advantage is maintained by implementing a simple lamination process which adheres the flex circuitry to a metal stiffener strip. As seen from Figure 2, the flex is adhered with the circuit side toward the stiffener. This orientation enables the polyimide substrate to be used as the solder mask. The standard process in fabricating this flex is to chemically etch holes in the polyimide to define the solder ball pads. With this process, all the vias are created simultaneously in an economic fashion. The uniformity of these etched vias are shown in Figure 3. The sloping sidewalls have been determined to be beneficial since they aid in capturing the solder ball when it is placed prior to reflow attach. In addition the gradual slope eliminates the stress concentration which can be imparted by the 90 degree corner at the soldermask edge<sup>4</sup>.

Some of the other TBGA configurations being offered in the market provide the circuitry on the same side as the solder balls. One must therefore incur an extra cost by performing additional process steps in order to coat on a soldermask followed by reregistration exposing and developing.

Positioning the circuit side of the flex toward the stiffener also provides an electrical advantage. It has been determined that the close proximity of the traces to the metal stiffener (approximately 1 mil space) makes this stiffener an excellent floating ground plane, thus reducing

signal cross talk between parallel traces. In addition, a process is currently being developed to make an electrical connection to the stiffener thus providing a low inductance ground path for high speed devices.

The TBGA package is also known for its light weight and low standoff height. Some physical characteristics, including thickness and weight, for two variations of TBGA packages are shown in Table 1. The package thickness can be reduced further with thinner stiffener materials and backgrinding of the die.

### Stiffeners

Figure 2 depicted a stiffener configuration in which two separate stiffeners (one which has a hole for the die) were adhered together. This stiffener layout provides a well defined inner bond window ledge which enables the bond fingers to be brought in as closely as possible to the die. In addition, it has been determined that the process of laminating the two metal stiffeners together actually improves the coplanarity over that of the individual pieces prior to lamination (as demonstrated in Figure 4)<sup>24</sup>. The final laminated piece typically has a coplanarity of less than 2 mils, while the individual pieces can have coplanarity of as high as 6 mils.

A method of cost reduction being implemented is to replace this two piece stiffener with a single stiffener with a cavity formed for the die, as shown in Figure 5. The stiffener material cost is cut in half and a layer of adhesive is eliminated. However, one drawback to this configuration is the sloped transition area at the edge of the formed cavity can add 10-20 mils to the wire length. There is also some concern that the formed cavity will be more difficult for attachment of a heat sink. Nevertheless, it is felt that the cost savings will make the cavity formed version an attractive alternative for many applications.

Two stiffener materials have been demonstrated to be effective. The first is standard 194 copper with a nickel coverplating. The other is a 304 austenitic stainless steel (nonmagnetic). This material is less costly since a coverplating is not required. The CTE of 17 ppm/°C is near that of copper and thus should be adequate from a board level reliability perspective. The drawback of SS is its low thermal conductivity, therefore this material would be more suitable for die with low to mid power levels.

### Wire Bond Results

**Table 1. Physical characteristics of typical TBGA packages.**

Product Type	Solder Ball Size	Assembled Package Weight	Package Height (on board)	Board Standoff Height
29mm 340i/o w/ 8mm die (20mil thick 1pc Ni/Cu stiffener)	0.76mm (30 mil)	5.8 g	1.7mm (66 mils)	0.56mm (22 mils)
35 mm 352i/o w/ 15mm die (2 pc Ni/Cu stiffener, 10 mils ea)	0.76mm (30 mil)	6.5 g	1.2mm (49 mils)	0.56mm (22 mils)

The challenge in constructing this TBGA was selecting the appropriate adhesive. As described in an earlier paper<sup>5</sup>, the adhesive chosen was a thermoplastic polyimide with a  $T_g$  of 220C. At temperatures lower than 220°C the modulus remains high (1000 MPa) thereby providing an excellent surface for wire bonding. Softer adhesives tend to absorb the ultrasonic energy, thus preventing an adequate bond<sup>3,6</sup>. The viscosity of the material at lamination temperatures also enabled the wire bond fingers to be directly embedded into the adhesive without the material flowing onto the pad surface. A great deal of wire bonding has been successfully performed to this TBGA carrier with various wire bond machines and at a wide range of temperatures. Gold wire bonding has been demonstrated at temperatures ranging from 150-200°C. Room temperature bonding with aluminum wire has also been proven. The following types of wire bond machines have thus far shown to be effective in bonding to this substrate: a K&S bonder, a Shinkawa bonder, an Abacus high frequency bonder, a Hughs bonder, and a Kaijo bonder. An example of standard 1mil gold wire bonds is shown in Figure 6 (note the short 50 mil wire length).

## RELIABILITY

A great deal of excellent board level reliability data has been published for PBGA packages<sup>11</sup>. However, the same has not yet been true for TBGAs which have more recently entered the scene. Since the CTE of a TBGA package is dominated by a metal stiffener with a CTE very similar to that of the circuit board, one would expect excellent thermal cycle reliability. An earlier paper revealed some thermal cycle reliability data which was generated to help guide in selection of the optimum materials for development of a reliable TBGA<sup>12</sup>. The two parameter Weibull distribution results from this -40/125°C cycling are shown in Table 2. Although these results satisfied the primary goal, they were lacking in several areas. For example, the sample sizes were not sufficient for detailed statistical analysis and these samples were daisy chained carriers with no die attached. In addition, the test board was fabricated with standard four layer FR4 with many through hole vias. Standard FR4 material has a  $T_g$  of approximately 120°C, therefore, as this temperature is approached the CTE of the board becomes nonlinear

(increasing to over 60ppm/°C<sup>3</sup>) and creates additional stress on the solder joints and the via barrels. In many cases the via barrels fractured before the solder joints, making it difficult to determine the actual cause of high resistance readings<sup>13,14</sup>. Introducing stresses in accelerated testing which a product would not experience in service is an issue of which reliability engineers must always be aware. Testing at temperatures too close to the  $T_g$  can also make it difficult to compare data with others in the literature since slight differences in the board materials and test temperatures can have a large impact on results.

Board level thermal cycling from 0/100C has also been taking place with these TBGA carriers mounted on four layer FR4. As of this writing over 17,500 cycles have been performed (nearly 16 months of testing) with only 2 failures recently occurring in the sample lots (shown in Table 2). A failure is characterized by a 1 ohm change in resistance of a row of solder joints (typically 30-40 joints). These results are encouraging since they appear to be surpassing QFPs and PBGAs, some of which have shown characteristic lives as high as 10-12000 cycles in this temperature cycling range<sup>9,15</sup>.

## Test Boards

The latest round of testing was performed using TBGA packages with bonded and encapsulated die. The test vehicles were 29mm with 340i/o with an 8 mm die in the cavity. Encapsulation was performed with a dam and fill process. A variety of stiffener configurations and solder ball pad sizes were investigated; ball pads were cover plated with 0.75µm Au over 1.25µm Ni. Sample lot sizes ranged from 21 to 69 samples. Having learned from previous testing, this time samples were attached to cards made from multifunctional FR4 with a  $T_g$  of 140°C. The advertised CTE of the material was 13ppm/°C, however Thermal Mechanical Analysis was used to measure the actual values. A fresh board had CTE values of 13.6 and 13.4 in the x and y directions, respectively. However, after 2000 thermal cycles (-55/125°C) the CTE values changed to 13.2 and 15.6 in the x and y directions. The expansion vs temperature curve for this board material was linear throughout the -55/125°C temperature cycling range. These were four layer boards (62 mils thick) with dummy

**Table 2. Previous board level thermal cycle results for 29mm, 340i/o TBGA carriers using standard FR4 boards.**

TBGA Sample Type	Ball Opening Diameter	Test Condition	# Samples	$\alpha$ ( $N_{63\%}$ )	$\beta$	$N_{0.01\%}$ 100ppm
304 stainless steel stiffener	400 µm	-40/125C	11	2913	3.9	275
“	500 µm	“	8	4080	5.0	647
“	600 µm	“	7	4600	3.6	356
“	400 x 600µm	“	9	3765	5.9	790
304 stainless steel stiffener	400 µm	0/100C	11	>17500	-	-
“	500 µm	“	11	>17500	-	-

copper planes in the center. An 8 mil stencil with 19 mil openings was used for depositing the solder paste onto the board pads. The TBGA packages were placed by hand and reflow attached using a Vitronics SMR400 conveyor oven with a standard profile which reached 220°C.

The daisy chain test board layout is shown in Figure 7. This design allowed the testing of individual nets by row with a four point probe resistance reading and was designed to do so without use of any through hole vias, which assured that any high resistance readings were caused only by the solder ball connections. Three components were mounted on each card and gold plated card edge fingers were used for electrical readings. The solder ball pads were solder mask defined with 19 mil openings. This is smaller than the 24-28 mil openings more typically used in PBGA testing. The drive, however, is to reduce the ball pad diameter to enable additional routing of lines through these channels on the mother board. Smaller board pads enable routing with coarser pitch circuit traces, thereby reducing the overall cost of the mother board.

**Test Conditions**

The samples were tested in an air to air thermal shock chambers (-55/125°C) at a rate of 3 cycles an hour with 5 minute ramps and 5 minute dwells. The chambers were set at -57 and 133°C to ensure the full five minutes of dwell time below -55 and above 125°C. After each 5 hours of cycling the samples were held in the 133°C chamber while the other chamber defrosted for one hour. This significant period of dwell time will certainly have an adverse effect on cycle life, as there is ample time for full creep to take place. Sets of samples were also placed in a 0/100°C thermal cycle chamber which cycled at a rate of 2 cycles/hour with 10 minute transitions and 5 minute dwell times. The samples were pulled from the ovens and resistance readings taken at intervals of 500-1000 cycles. Any resistance change of over 1 ohm were considered a failure. This is a conservative approach to determining failure since continuous monitoring systems typically allow the samples to go full open before recording as a failure. Although it is preferable to continuously monitor devices, it is felt that interval testing is still fairly accurate since it is cumulative failure data which is being gathered, and the data usually tends to behave well (closely following the Weibull distribution.).

**RESULTS**

The results of the -55/125°C testing is shown in Table 3 and Figure 8 and 9. The results were fit to a two parameter Weibull distribution which is characterized by the equation:

$$F(t) = 1 - \exp(-(t/\alpha)^\beta)$$

where,  
 $\alpha$  is the characteristic life  
 (cycles to 63.2% failed devices)

$\beta$  is the shape parameter (slope)  
 t is the number of cycles

A Weibull distribution indicates a slow and non accelerating crack growth rate, which has been shown to be appropriate for plastic ball grid arrays. Ceramic BGAs, on the other hand, often exhibit a better fit to a log normal distribution which is an indicator of a more brittle joint in which the crack rate accelerates with increasing size<sup>8,16,17</sup>. Similar samples are also currently being subjected to 0/100°C cycling with no failures yet detected at 8500 cycles.

Solder ball pad sizes of 400, 500, and 600µm diameter were evaluated. Even the smallest pads had respectable results with a characteristic life of 5046 cycles (for the copper stiffener samples). Increasing the pad size to 500µm resulted in a 15% increase in life. A further pad size increase to 600µm resulted in only an 8% characteristic life improvement. A model by Darveaux has predicted a 50% improvement in fatigue life by increasing pad size from 500 to 600µm<sup>10</sup>. Upon cross sectioning and dye penetrant testing of these largest joints (a process whereby ink is allowed to penetrate the joints to reveal the fractures<sup>13</sup>), it was found that all the failures occurred at the smaller 475µm board pad interface which appeared to be the limiting factor. One would therefore expect the reliability to significantly improve with a larger board pad size to match that on the component. However, an interesting observation is the large (over 80%) increase in the shape parameter (or slope) of the Weibull distribution. A larger slope is favorable since it results in a higher reliability for small failure rates. Cycles to 0.01% failed components is usually of greatest interest to computer manufacturers since this is closer to what may be encountered in the field. There is a 63% improvement in  $N_{0.01\%}$  as the pad size is increased from 500 to 600µm.

The previously discussed samples were fabricated with copper stiffeners. The Weibull distribution for TBGA samples constructed with stainless steel stiffeners is shown in Figure 9. Although these characteristic life values are a bit lower than what was recorded for the copper stiffeners they are still quite attractive. A 19% decrease in characteristic life was found for SS stiffeners with the 500µm pad size and a 14% decrease for the 600µm pad size. Samples with the two piece SS stiffeners were found to be equivalent to the cavity formed stiffener. The TBGAs with stainless steel stiffeners likely did not perform quite as well due to their slightly higher CTE of 17ppm/°C compared to 16.3ppm/°C for 194 copper (recall that these particular test boards had a CTE of near 14ppm/°C). A sample set of carriers with no die attached (similar to those previously tested and shown in Table 2) were also evaluated to determine the effect of testing with the higher temperature FR4 boards compared to the standard FR4. These samples had a characteristic life of 6696 cycles

**Table 3. Most recent board level thermal cycle test results for a 29mm 340i/o TBGA with encapsulated die and high temperature FR4 board material.**

TBGA Sample Type	Ball Opening Diameter	Test Condition	# Samples	$\alpha$ ( $N_{63\%}$ )	$\beta$	$N_{0.01\%}$ 100ppm	Fit %
Cu cavity stiffener w/ encapsulated die	400 $\mu\text{m}$	-55/125C	40	5046	11.2	2219	99.4
“	500 $\mu\text{m}$	“	69	5776	10.0	2300	99.9
“	600 $\mu\text{m}$	“	35	6239	18.2	3760	98.9
SS cavity stiffener w/ encapsulated die	500 $\mu\text{m}$	“	22	4653	7.6	1396	98.7
“	600 $\mu\text{m}$	“	21	5370	11.4	2400	99.9
2 pc SS stiffener w/encapsulated die	500 $\mu\text{m}$	“	20	4827	6.9	1270	99.3
SS stiffener frame (no die)	500 $\mu\text{m}$	“	24	6696	13.4	3368	99.4
Cu cavity stiffener w/ encapsulated die	400 $\mu\text{m}$	0/100C	24	>6000 in prog			
“	500 $\mu\text{m}$	“	36	>8500			
“	600 $\mu\text{m}$	“	24	>8500			
“ w/ NSMD board pads	500 $\mu\text{m}$	“	36	>8500			
SS cavity stiffener w/ encap die	500 $\mu\text{m}$	“	24	>8500			
2 pc SS stiffener w/encapsulated die	500 $\mu\text{m}$	“	24	>8500			

which was 60% higher than the 4080 cycles recorded with standard FR4. The slope was also considerably higher (almost 3x). This difference demonstrates the strong effect of circuit board material on package solder joint reliability.

Although this -55/125°C cycling was performed with air to air thermal shock, the failures were still through the solder at the joint interfaces (primarily the board side interface). Examples of these joints are shown in Figure 10. Previous studies have shown that faster ramp rates and longer dwell times increases the stress on the solder joints. Consequently, the fatigue life is typically shorter for a thermal shock test than for a slower thermal cycle test (ramp rates less than 20°C/min). This effect is due to the yield strength of solder being highly strain rate sensitive, thus more rapid temperature transitions result in higher stress build up, which in turn results in larger amounts of creep deformation. However, a thorough investigation by Darveaux has concluded that as long as the failure mechanism is the same (namely fatigue of the solder), modeling can be done to predict the life in actual operating conditions<sup>10</sup>.

A two parameter Weibull distribution was used for this data since too few data points were available to justify a 3 parameter Weibull. Although characteristic life values are typically similar for the two models, the 2P Weibull is considerably more conservative in its estimates for  $N_{0.01\%}$  (cycles to 0.01% failures). As a result, even though the data shown in Table 3 is quite favorable it could still be considered conservative.

For comparison purpose, the results of thermal cycle testing of various other electronic packages reported in the literature are shown in Table 4. The -55/125°C thermal shock results generated from the TBGA package compare quite favorably to other packages cycled in the range -40/125°C. The TBGA values for  $N_{0.01\%}$  were considerably better than those reported for PBGA and CCGA packages and comparable to the small (132i/o) ceramic and plastic QFPs. The 340i/o TBGA was significantly better than the 208 and 256 i/o plastic QFPs.

### Life Predictions

The most commonly used transform used to extrapolate accelerated test results into real life cycles is a modified form of the Coffin/Manson model known as the Norris/Landzberg relation<sup>19,21</sup>. This relation defines the appropriate acceleration factor for thermal cycle fatigue as,

$$\eta = (f_o/f_t)^{1/3} (\Delta T_t/\Delta T_o)^2 (\theta_t/\theta_o)$$

where,

$f_o$  is the cycle frequency in the actual use conditions

$f_t$  is the accelerated test cycle frequency

$\Delta T_t$  is the temperature range in test

$\Delta T_o$  is the temperature range in use condition

$\theta_o$  is the plastic deformation of the solder joint at maximum operating stress

$\theta_t$  is the plastic deformation of the solder joint at maximum test stress

The acceleration factor is used to predict values for  $\alpha$  and  $N_{0.01\%}$  in actual use conditions (the  $\beta$  value is typically assumed to remain constant). For example, the

**Table 4. Comparison thermal cycle test results of various packages reported in the literature.**

Device	Source	Cycle Condition (°C)	$\alpha$ ( $N_{63\%}$ )	$\beta$	$N_{0.01\%}$ 100ppm
72 i/o PBGA	Motorola <sup>11</sup>	-40/125, 1 cph	2260	9.1	821
68 i/o PLCC	Motorola <sup>11</sup>	-40/125, 1 cph	7332	3.3	450
208 i/o PQFP	Motorola <sup>11</sup>	-40/125, 1 cph	9111	2.6	263
132i/o CQFP	Motorola <sup>11</sup>	-40/125, 1 cph	3967	18	2378
132 i/o PQFP	Motorola <sup>11</sup>	-40/125, 1 cph	9890	8.1	3170
625 i/o CCGA	Motorola <sup>8</sup>	-40/125, 1 cph	779	10.8	332
256 i/o PQFP (no clean paste)	HP <sup>15</sup>	-40/125, 1.3 cph	12114	2.1	150
225 i/o PBGA	Compaq <sup>18</sup>	-25/100, 2 cph	2937	8.1	942
225 i/o PBGA (SMD pads)	Compaq <sup>19</sup>	-25/100, 2 cph	6268	4.1	663
225 i/o PBGA (NSMD pads)	Compaq <sup>19</sup>	-25/100, 2 cph	5698	8.0	1800
119 i/o PBGA	Motorola <sup>9</sup>	0/100, 2.4 cph	10221	8.2	3311
361 i/o PBGA	Motorola <sup>9</sup>	0/100, 2.4 cph	11886	10.9	5119
225 i/o PBGA	Motorola <sup>9</sup>	0/100, 2.4 cph	10429	14.2	5450
225 i/o PBGA	Motorola <sup>9</sup>	0/100, 2.4 cph	7956	13	3926
169 i/o PBGA	AT&T <sup>20</sup>	0/100, 2 cph	4651	8.7	1610
225 i/o PBGA	AT&T <sup>20</sup>	0/100, 2 cph	3960	6.7	1000
625 i/o CCGA	Motorola <sup>8</sup>	0/100 1.3 cph	2490	6.8	640

characteristic life in an application would be equal to the acceleration factor multiplied by the characteristic life in test ( $\alpha_o = \eta\alpha_t$ ).

Ideally, a finite element model should be performed to determine the most accurate value for the plastic strain in the solder joint during cycling. However, in lieu of such a model at this time, a rougher estimate will be made using the maximum distance from neutral point (DNP). The total shear strain in the outermost solder ball can be written as,

$$\theta_t = (\text{DNP} \times \Delta T \times \Delta \text{CTE})/h$$

where ,

DNP is the diagonal distance from the center to the outermost ball (19mm)

$\Delta T$  is the temperature cycle range

$\Delta \text{CTE}$  is the difference in CTE between the package and the board (2ppm in this case)

$h$  is the standoff height of the package (0.96mm)

A -55/125°C cycle with this package and board configuration results in a total shear strain of 0.71% (assuming the stiffener and board are rigid materials). The portion of this value which is plastic strain can be estimated with knowledge of the solder yield strength and shear modulus. The shear modulus is given by the relation,

$$G = \tau/\theta = E/2(1+\nu)$$

where,

$\tau$  is the elastic shear stress

$\theta$  is the elastic shear strain

$E$  is the elastic modulus

$\nu$  is poisson's ratio (0.4 for solder)

The elastic modulus decreases with temperature and is estimated to be 2000ksi at a temperature of 125°C<sup>10</sup>. The shear modulus is therefore 714ksi. The shear strength of 62/36/2Ag solder is reported as 1.8 ksi at a temperature of 100°C and 4.1ksi at 20°C; this is at a strain rate of 0.05mm/min<sup>22,23</sup> which is near that of our system (0.0014 mm/min). Assuming a linear relationship of shear strength with temperature would suggest a shear strength of 1.08ksi at 125°C. The yield strength is estimated to be one third of the fracture strength, or 0.36 ksi. The elastic strain is simply  $\tau_y/G$  or 0.050% which leaves a plastic strain of 0.66%. When calculating the plastic strain in actual applications the shear modulus and shear strength for the maximum use temperatures will be used. Appendix A shows calculations performed using the Norris/Landzberg equation to estimate the acceleration factor for various operating temperature ranges. The resulting estimated life values are provided in Table 5. Note that the data in this table is generated for a TBGA package with a relatively small package pad diameter of 500 $\mu\text{m}$ . Use of 600 $\mu\text{m}$  pads would result in  $N_{0.01\%}$  values 1.63x larger.

A temperature change of 80°C or less is typically experienced in computer applications. Assuming one cycle per day, the life of the package (point at which 100ppm of the components fail) is estimated to be over 21 years. This is beyond the expected lifetime of most computers.

Although these predicted life expectancies are very positive, they are still believed to be quite conservative. Recall the analysis by Darveaux which concluded that a more rapid thermal cycle rate actually causes more solder joint damage than slower rates. The Norris/Landzberg

**Table 5. Estimated life of TBGA with copper stiffener and 20 mil diameter ball pads.**

Temp Range of Application	Cycle Freq	Max Plastic Strain in Joint	Acceleration Factor ( $\eta$ )	Estimated $N_{0.01\%}$	Estimated Life to 100ppm Failures
20/50°C	365 cycles/year	.00045	135	311000	850 years
20/75°C	365 cycles/year	.00139	13.0	29900	81.9 years
20/100°C	365 cycles/year	.00250	3.42	7866	21.6 years
0/100°C	365 cycles/year	.00329	1.66	3820	10.5 years
-20/100°C	365 cycles/year	.00427	0.84	1930	5.3 years

relation treats this as the inverse (slower cycles causing more damage), consequently life estimates using this relation may be underestimated. In addition, the two parameter Weibull equation had been used to generate  $N_{0.01\%}$  which was a conservative estimate in its own right. Finally, the elastic deformation of the polyimide substrate and the circuit board material were not taken into account. If this were done, the plastic strain in the joint would be less than what was predicted, and for the lower operating temperature ranges there would be no plastic deformation at all in the bulk of the joint (only localized at the crack tip).

Future work will be performed to provide a more detailed FEA model of the plastic deformation and thus obtain more accurate life predictions.

### CONCLUSIONS

The characteristics and reliability of a new wire bondable tape ball grid array package has been discussed. There are many benefits to using fine pitch flexible circuitry in fabrication of a BGA. The capability for positioning the wire bond pads close to the die lowers the inductance of the wire and allows the possibility for die shrink on pad limited devices. The thermal capability of this TBGA design is excellent since much of the heat can be dissipated through all the solder balls and into the motherboard. Board level thermal shock testing (-55/125°C) and thermal cycling (0/100°C) has been carried out with very favorable results. Over 15000 cycles of 0/100°C testing have taken place thus far with no failures yet detected. Weibull plots of thermal shock tested samples showed very favorable characteristic life values and fairly steep slopes ( $\beta$  values greater than 10). Life predictions for operating conditions were very favorable as well, with the component life far exceeding the life expectancy of most computers.

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**APPENDIX A**  
**Calculations for life expectancy of TBGA**

Total shear strain in solder joint is,  
 $e_t = \text{DNP} \times \Delta T \times \text{CTE}/h = 19\text{mm} \times 180^\circ\text{C} \times 2\text{ppm}/.96\text{mm} = .0071$

Shear modulus is written,  
 $G = \tau/\theta = E/2(1+\nu) = 714\text{ksi}$  for solder at  $125^\circ\text{C}$

Shear strength of solder at  $100^\circ\text{C}$  at strain rate of  $0.05\text{mm}/\text{min}$  is  $12\text{MPa}$  or  $1.8\text{ksi}$ . The strain rate of our system is  $.0068\text{mm}/5\text{min} = .0014\text{mm}/\text{min}$  which is close to the lower stated value.

Shear strength at  $20^\circ\text{C}$  is  $4.1\text{ksi}$  and at  $100^\circ\text{C}$  is  $1.8\text{ksi}$ . Assume a linear relationship with temp for calculating the shear strength at various use temperatures (example, at  $125^\circ\text{C}$   $\tau = 1.08\text{ksi}$ ). Assume the yield strength is  $1/3$  of the shear strength or  $0.36\text{ksi}$ .

Then the elastic strain in the joint is  $\theta_e = 0.588\text{ksi}/714\text{ksi} = 0.00050$

Therefore, the plastic strain in the joint is,

$$\theta_p = \theta_t - \theta_e = .0071 - .00082 = .0066$$

Assume no elastic deformation of the polyimide substrate or the PC board material. If this were taken into account the plastic strain would decrease further to where in many use applications there would be no plastic deformation in the solder joint (only at the crack tip).

Use temperature range of  $20$ - $50^\circ\text{C}$ .

$$\begin{aligned} \tau &= 3.23 \text{ so } \tau_y = 1.07\text{ksi} \\ G_{50\text{C}} &= 4\text{MPa}/2.8 = 1.43\text{Msi} \\ \theta_t &= 19 \times 2\text{ppm} \times 30\text{C}/.96\text{mm} = .0012 \\ \theta_e &= 1.07/1430 = .00075 \\ \text{therefore } \theta_p &= .00045 \\ \eta &= (f_o/f_t)^{1/3} (\Delta T_t/\Delta T_o)^2 (\theta_o/\theta_t) \\ \eta &= (1/60\text{cycles/day})^{1/3} \times (180^\circ\text{C}/30^\circ\text{C})^2 \times (.0066/.00075) = 135 \end{aligned}$$

Use temperature range of  $20$ - $75^\circ\text{C}$ .

$$\begin{aligned} \tau &= 2.52\text{ksi so } \tau_y = 0.84\text{ksi} \\ G_{75\text{C}} &= 3\text{MPa}/2.8 = 1.07\text{Msi} \\ \theta_t &= 19 \times 2\text{ppm} \times 55\text{C}/.96\text{mm} = .00217 \\ \theta_e &= 0.84\text{ksi}/1070\text{ksi} = .000785 \\ \text{therefore } \theta_p &= .00139 \\ \eta &= (1/60\text{cycles/day})^{1/3} \times (180^\circ\text{C}/55^\circ\text{C})^2 \times (.0066/.00139) = 13.0 \end{aligned}$$

Use temperature range of  $20$ - $100^\circ\text{C}$ .

$$\tau = 1.8\text{ksi so } \tau_y = 0.60\text{ksi}$$

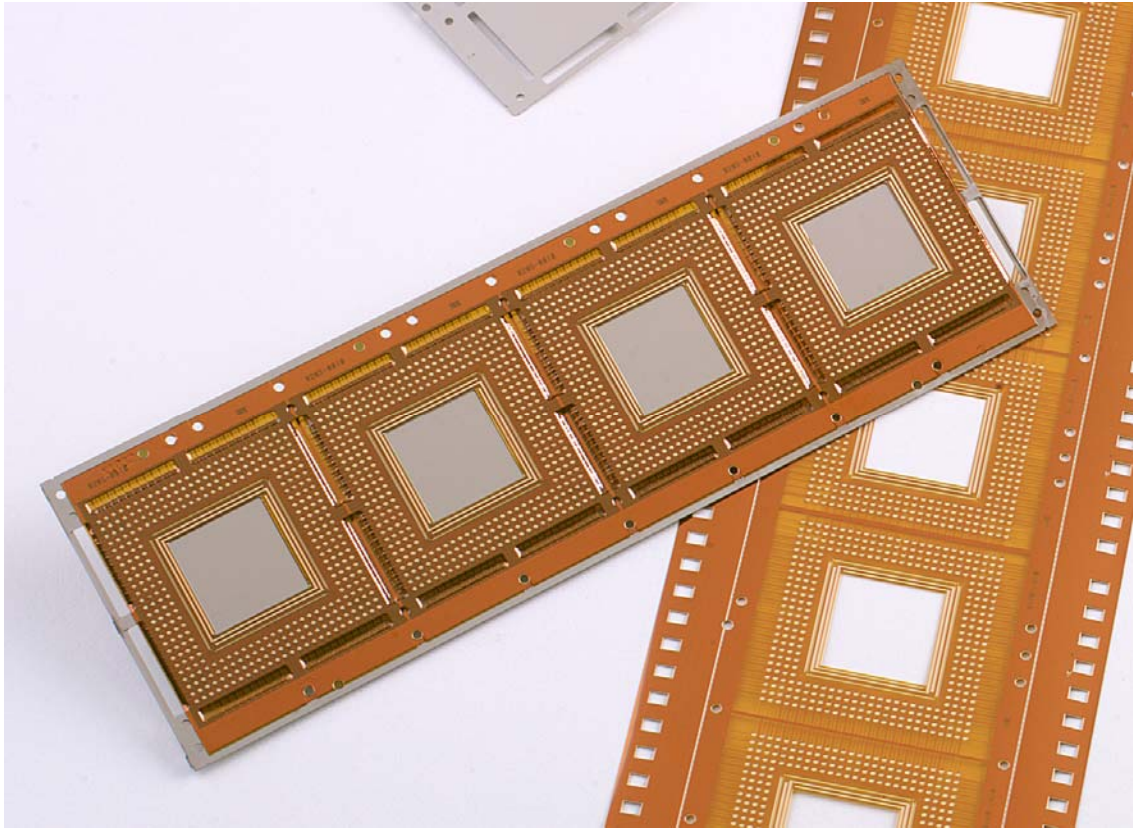
$$\begin{aligned} G_{100\text{C}} &= 2.5\text{MPa}/2.8 = 0.89\text{Msi} \\ \theta_t &= 19 \times 2\text{ppm} \times 80\text{C}/.96\text{mm} = .00317 \\ \theta_e &= .6/890 = .000674 \\ \text{therefore } \theta_p &= .00250 \\ \eta &= (1/60\text{cycles/day})^{1/3} \times (180^\circ\text{C}/80^\circ\text{C})^2 \times (.0066/.0025) = 3.42 \end{aligned}$$

Use temperature range of  $0$ - $100^\circ\text{C}$ .

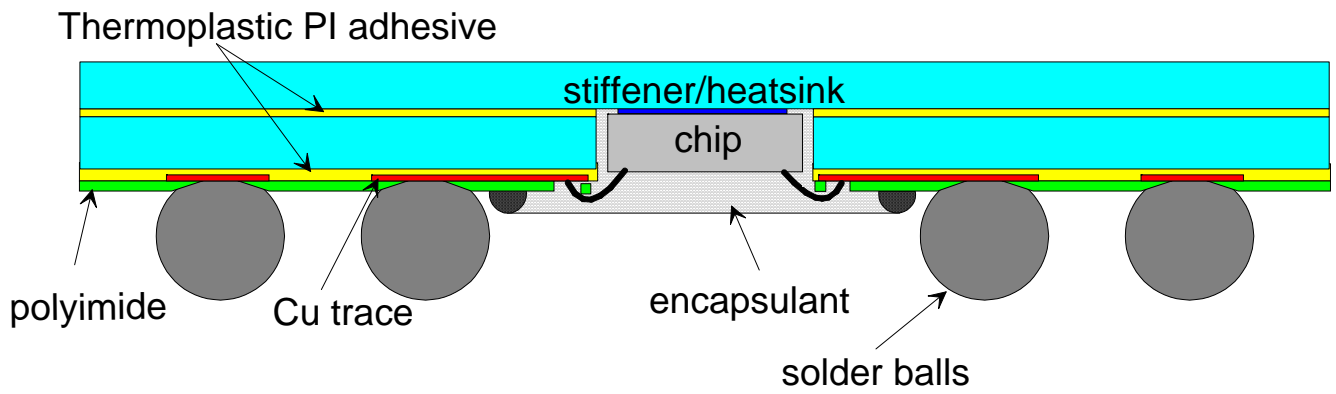
$$\begin{aligned} \tau &= 1.8\text{ksi so } \tau_y = 0.60\text{ksi} \\ \theta_{100\text{C}} &= 2.5\text{MPa}/2.8 = 0.89\text{Msi} \\ \theta_t &= 19 \times 2\text{ppm} \times 100\text{C}/.96\text{mm} = .00396 \\ \theta_e &= .6/890 = .000674 \\ \text{therefore } \theta_p &= .00329 \\ \eta &= (1/60\text{cycles/day})^{1/3} \times (180^\circ\text{C}/100^\circ\text{C})^2 \times (.0066/.00329) = 1.66 \end{aligned}$$

Use temperature range of  $-25$ - $100^\circ\text{C}$ .

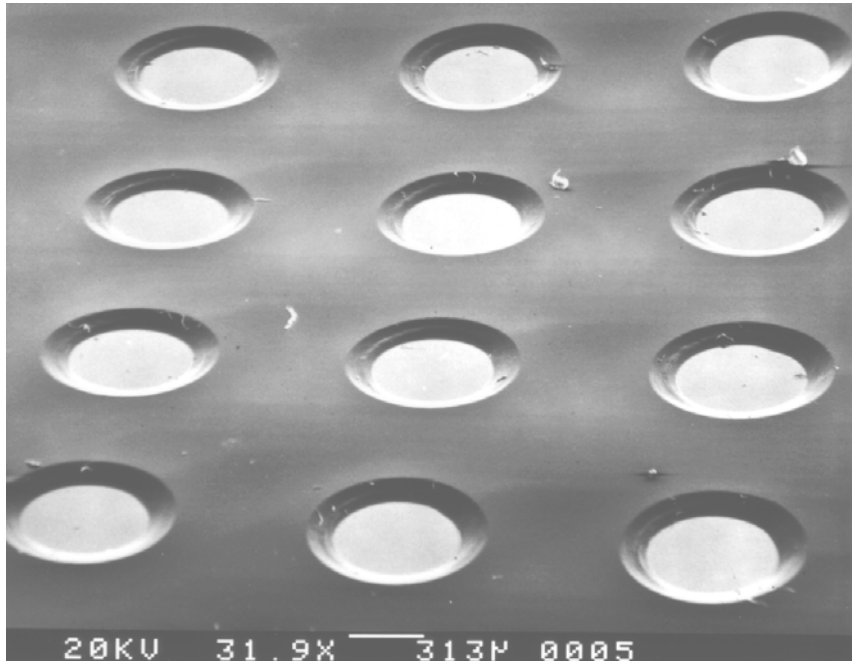
$$\begin{aligned} \tau &= 1.8\text{ksi so } \tau_y = 0.60\text{ksi} \\ \theta_{100\text{C}} &= 2.5\text{MPa}/2.8 = 0.89\text{Msi} \\ \theta_t &= 19 \times 2\text{ppm} \times 125\text{C}/.96\text{mm} = .00495 \\ \theta_e &= .6/890 = .000674 \\ \text{therefore } \theta_p &= .00427 \\ \eta &= (1/60\text{cycles/day})^{1/3} \times (180^\circ\text{C}/125^\circ\text{C})^2 \times (.0066/.00427) = 0.84 \end{aligned}$$



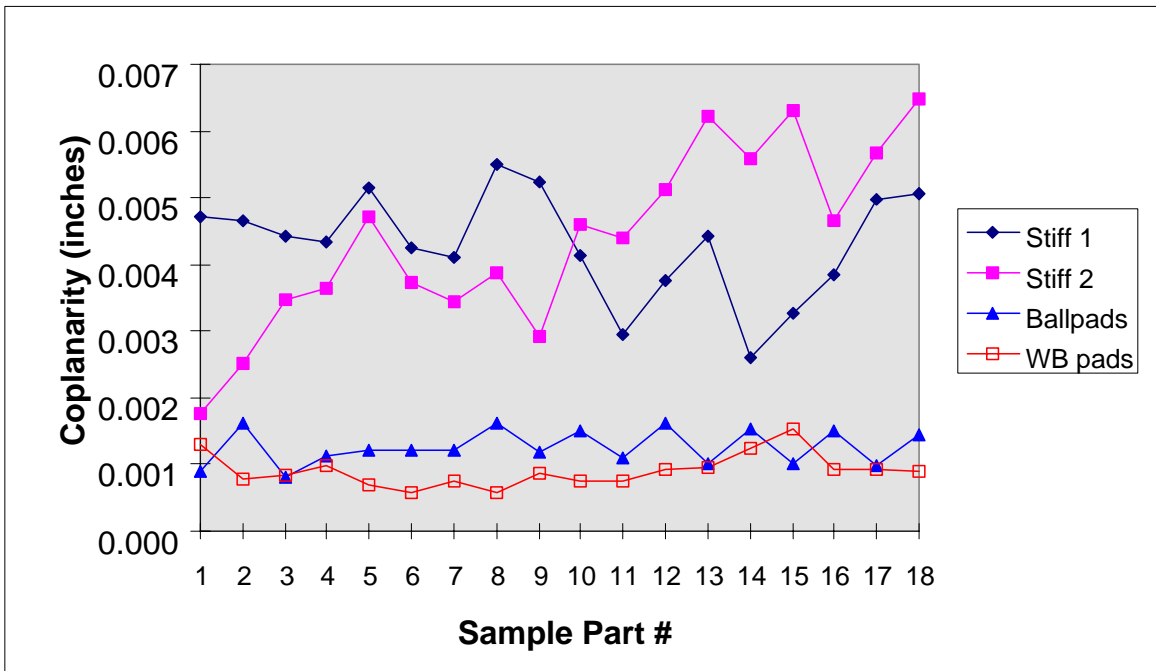
35mm, 352i/o, TBGA carrier strip.  
Figure 1.



Cross section schematic of a completed TBGA with a two piece stiffener.  
Figure 2.

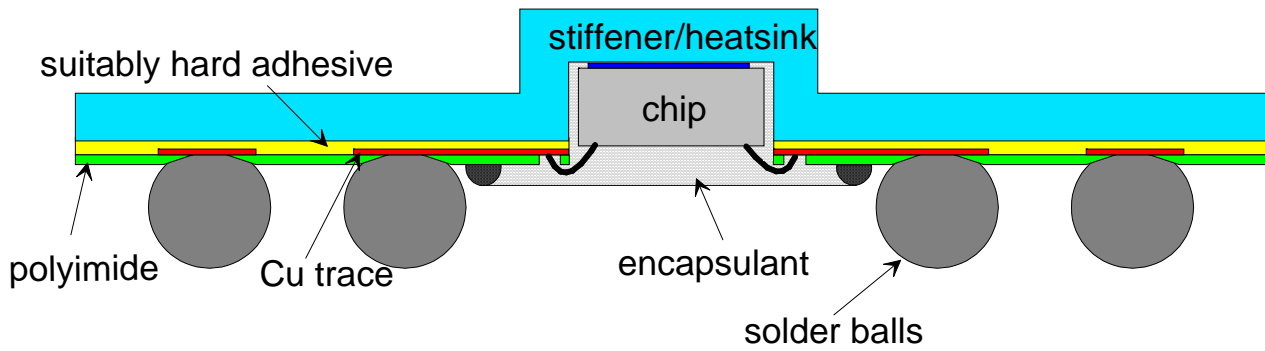


Uniformly etched PI substrate to expose solder ball pads.  
Figure 3.

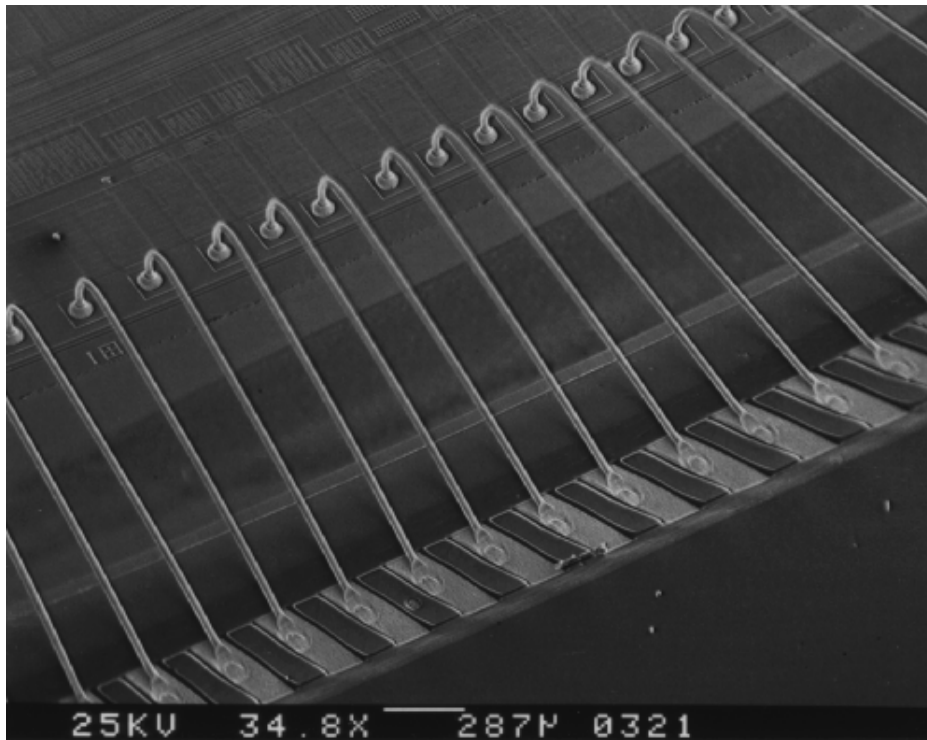


Coplanarity of 35mm 352i/oTBGA samples. The coplanarity of the final laminated unit is significantly better than the individual pieces prior to lamination. The coplanarity of the solder ball pads and wire bond pads is shown.

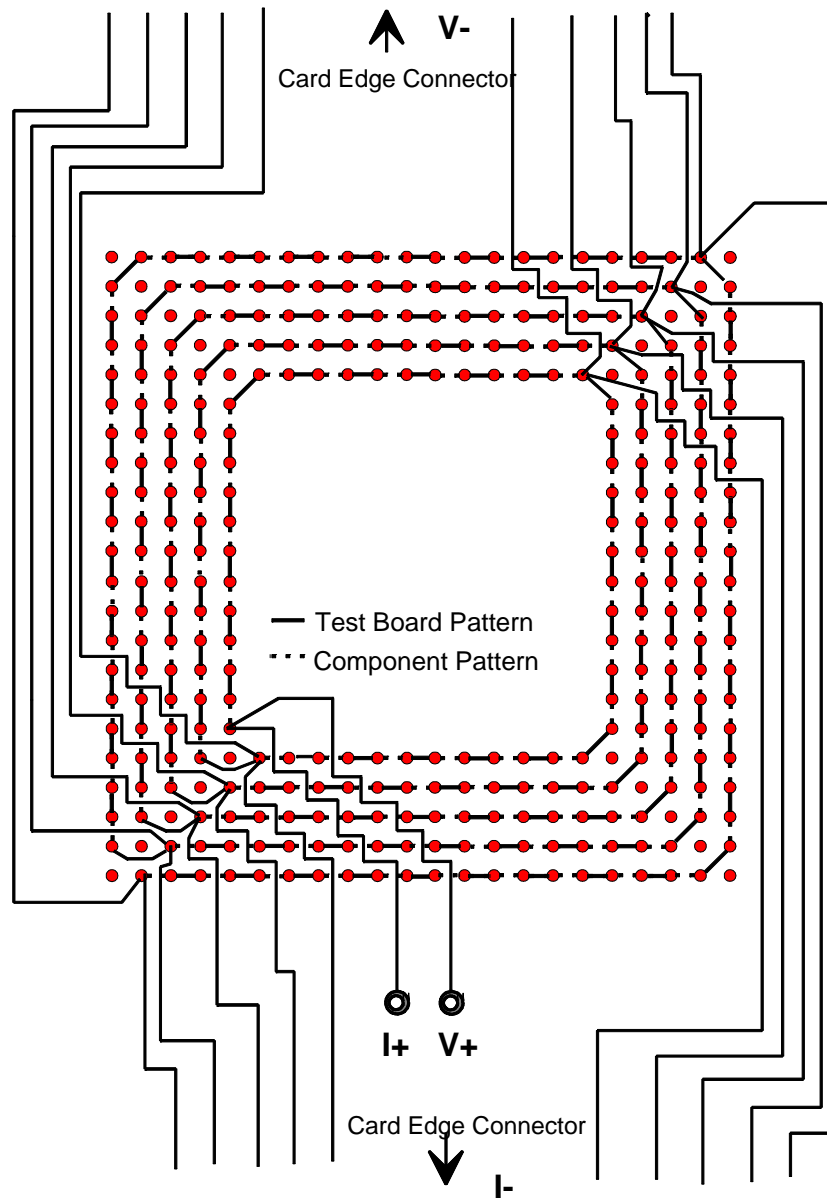
Figure 4



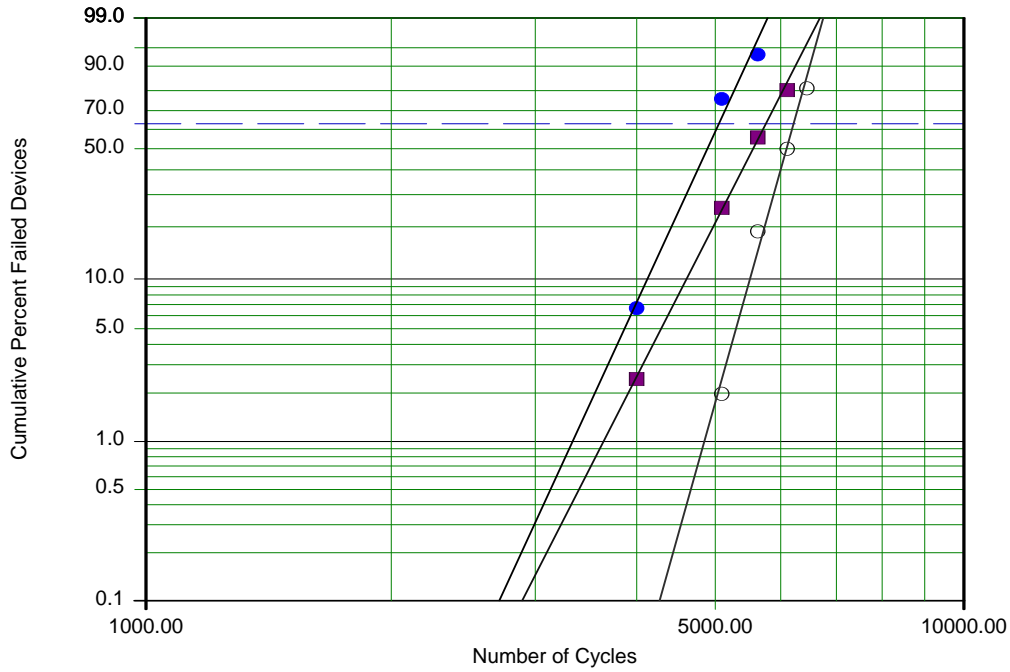
A TBGA utilizing a single stiffener with a cavity formed for the die.  
Figure 5.



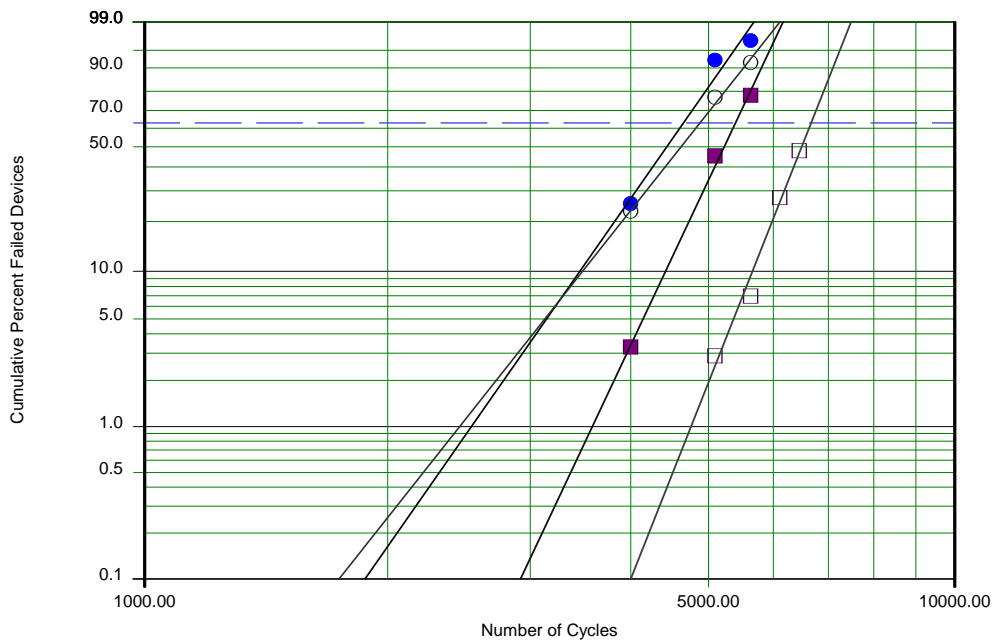
A die wire bonded to a TBGA carrier (note the short wire lengths).  
Figure 6.



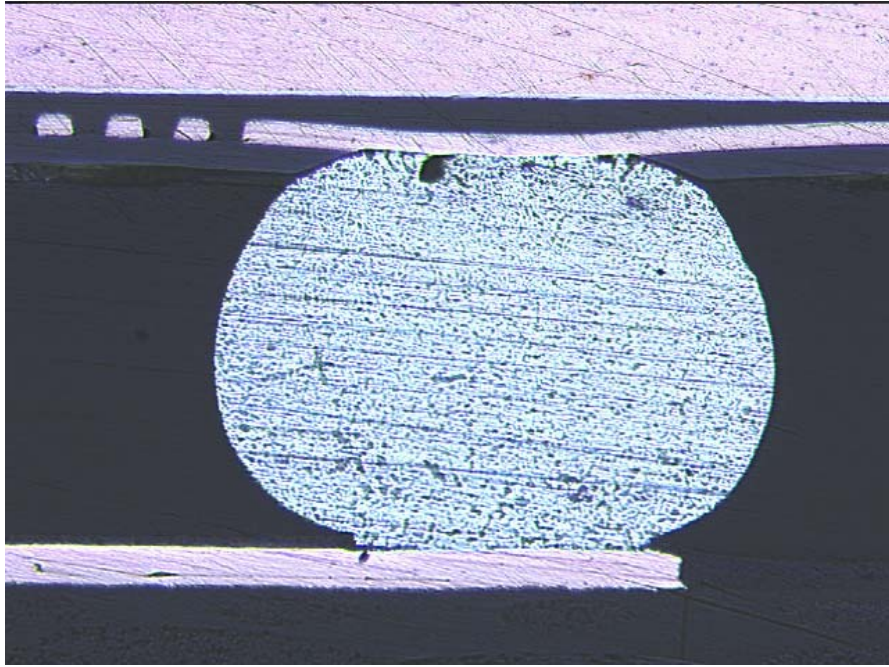
Daisy chain test board layout. Enables 4 pt probe readings with no through hole vias.  
Figure 7.



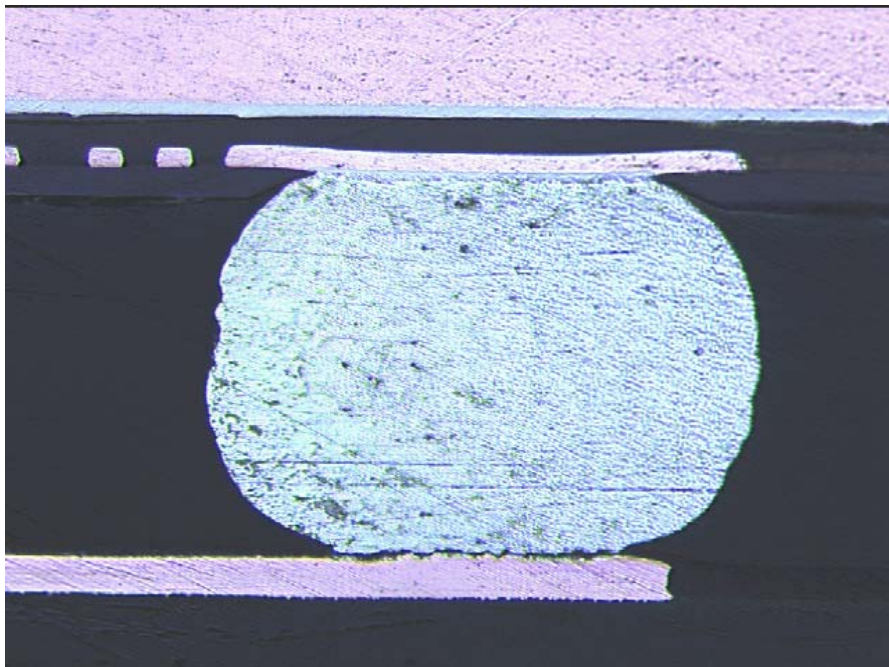
Results of -55/125°C board level thermal shock testing. Ni/Cu stiffeners with ● 400µm, ■ 500µm, and ○ 600µm solder ball openings. Figure 8.



Results of -55/125°C thermal shock testing. Stainless steel stiffeners with ● 500µm and ■ 600µm pads; ○ 2pc stiffener with 500µm pads; □ SS stiffener with no die attached (500µm pads). Figure 9.



An example of a solder joint with a 400 $\mu$ m diameter pad on the package side.  
Figure 10a



An example of a solder joint with a 500 $\mu$ m pad. The failure in this joint was  
at the board pad interface.  
Figure 10b.