

## A New Enhanced Flex Based Chip Scale Package with Improved Board Level Reliability

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### Abstract

*This paper outlines a few of the more promising chip scale package configurations and discusses where they stand with respect to some of the ideal requirements for a CSP. These criteria being, low cost, a good fit to the infrastructure, and excellent board level reliability. Measured against these criteria, none of these packages has emerged as a clear winner. This paper will address a new patent pending chip scale package concept which has low cost potential, uses conventional wire bonding and overmolding processes and has been predicted through mechanical modeling to have excellent board level reliability. Instead of using an elastomeric interposer which decouples the stress of the die from the board, the strategy is to minimize the solder joint stress by instead incorporating a copper interposer which has a matching CTE to that of the board. The die is directly attached to the copper interposer using a standard low stress die attach adhesive. The carrier is supplied in a rigid strip format which can be easily handled with the conventional industry infrastructure. This package is currently being assembled for both a cavity up configuration (peripheral wire bonding to the die) and a cavity down variety (central bonding to the die, ex. DRAM).*

**Keywords:** CSP, chip-scale packaging, BGA, ball grid array, flex circuitry

### Introduction

The high demand for small form factor packaging is well recognized in the industry and is being driven by the continual shrinkage in size of products such as cellular phones, pagers, personal digital assistants, digital cameras, disk drives, etc. Such applications also demand high reliability and low cost from the IC package. A decade ago the common theory was that flip chip to board would be the dominant small scale method of surface mounting ICs. With the anticipated cost reductions of bumping die it was felt that this elimination of the package would produce the lowest cost solution. While the cost of bumping die has indeed decreased, with continued improvements on the way [1,2,3], the trend toward surface mounting of flip chips has not taken place except for primarily very low cost, low i/o and low performance applications such as watches and games (although there are some exceptions). Flip chip attach directly to the board is not as straightforward as once thought due to the poor reliability of the solder joint connections when mounting the chip with low CTE (2 ppm/°C) to a circuit board with CTE of 15-18 ppm/°C. Adequate reliability can be achieved by underfilling the die with an epoxy compound but the infrastructure for this process is limited at the board mount shops and there does not appear to be much incentive to invest the resources to expand it. This resistance stems from the fact that board shops are accustomed to mounting components at rates of thousands an hour whereas it can take 30 seconds or longer to underfill just one die. In addition, it is very difficult and costly to rework an underfilled die if there is a defect.

Consequently, the whole board oftentimes needs to be thrown out. At the modest profit margins with which these shops operate, such losses would be very painful in those frequent cases where the board is of significant value [4].

Consequently, elimination of the package is not as easy as once thought. The accumulation of the above factors is the reason for the rapidly rising popularity of chip scale packages. In the past 5 years there have been over 36 different chip scale package concepts proposed worldwide to satisfy the need for reduced size and weight in portable systems [5]. Charles Lassen summed it up nicely when he suggested that 3 main criteria must be met for a particular CSP to win out as the dominant package [6].

- 1). The first requirement is to have good board level reliability (able to achieve 1000 cycles from -25 to 125°C on FR4). Many others in the industry also demand a JEDEC level 2 or 3 moisture resistance.
- 2). The second requirement is that the package have high volume availability which typically indicates that it must utilize existing infrastructure for assembly.
- 3). Finally the package must be able to achieve low cost, reaching 0.8 cents/pin for unit volumes of 1 million/month.

When judged against these criteria, no CSP solution has yet to emerge as a clear winner, although there are a few

leaders. This paper will discuss a new package option which holds promise for satisfying each of these demands and offers other advantages as well.

### Review of Main CSP Approaches

The Tessera  $\mu$ BGA<sup>TM</sup>, the most publicized and recognized of all CSPs, uses a layer of elastomer between the die and the flexible substrate to absorb the CTE mismatch strains between the die and the board (as shown in Figure 1) [7,8,9,10]. Of the currently available CSPs, it may be the best positioned to meet the first criteria of board level reliability. Meeting the cost targets suggested by Lassen remains to be seen but the potential is certainly there for high volume applications in which there is no change to the die size and layout. Because the  $\mu$ BGA<sup>TM</sup> requires bonding of preformed leads on the flex circuit, a new circuit is required with each die shrink or change in pad layout (meaning additional time and tooling costs). The

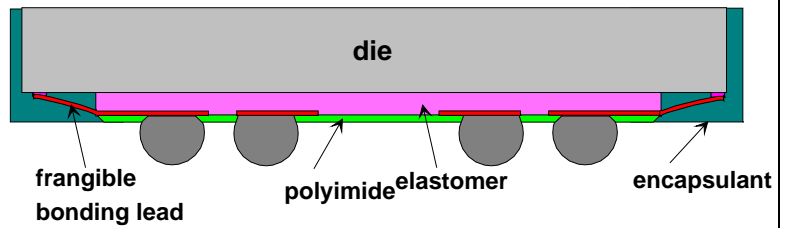


Figure 1: Tessera  $\mu$ BGA. Elastomer layer is used to absorb the CTE mismatch strain.

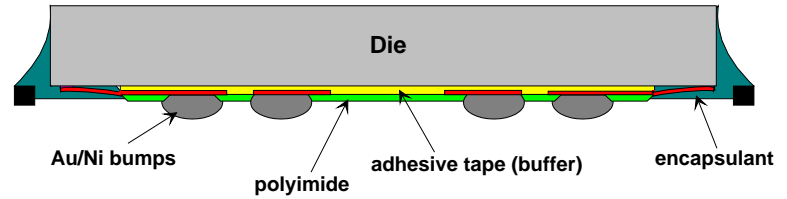


Figure 2: Sony NT-CSP. Similar to the Tessera version with adhesive substituted for the elastomer.

largest shortcoming of the  $\mu$ BGA<sup>TM</sup> may lie in the area of infrastructure fit. New equipment and training is required for the lead forming and bonding process, the elastomer deposition process, as well as the encapsulation process. In order to reach very large volumes and wide spread acceptance, significant capital equipment and training is required in the industry.

Sony has introduced a CSP called NT (New TAB)-CSP [11] which is quite similar to the Tessera  $\mu$ BGA<sup>TM</sup>, however instead of an elastomer interposer they use an adhesive tape which provides less compliance. From Figure 2, one can see that the lead bonding method and encapsulation process are quite similar. This package will therefore have many of the same characteristics as discussed with the  $\mu$ BGA<sup>TM</sup> above.

Another CSP that is gaining in popularity is one which uses a BT circuit board as the substrate, such as in the Amkor/Anam ChipArray<sup>TM</sup> package (actually a mini PBGA). Several others in the industry are also looking into a similar structure. This package, shown in Figure 3, uses conventional die attach to a circuit board, standard wire bonding and then uses encapsulation or overmolding of the die, followed by dicing from the board. The author is unaware of the reliability of such a package but would surmise it to be marginal to good (similar to the life of solder joints beneath the die of a PBGA). The shortcoming of this package may lie in the cost. With CSPs demanding ball pitches of 0.5 to 1.0 mm, the

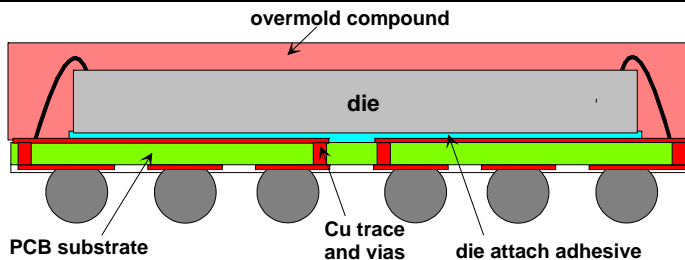


Figure 3: CSP using a BT circuit board as the substrate

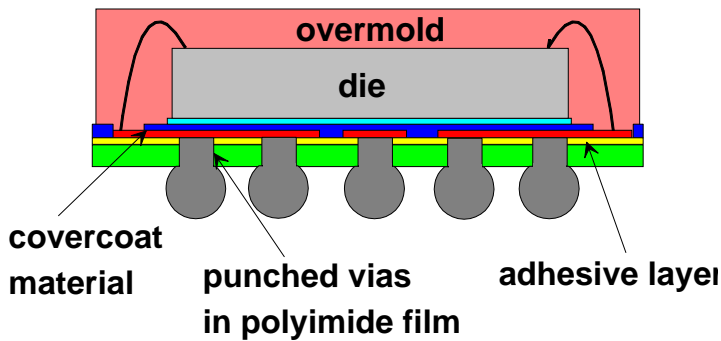


Figure 4: TI  $\mu$ Star CSP. Die is attached directly to covercoated flex circuit with punched vias.

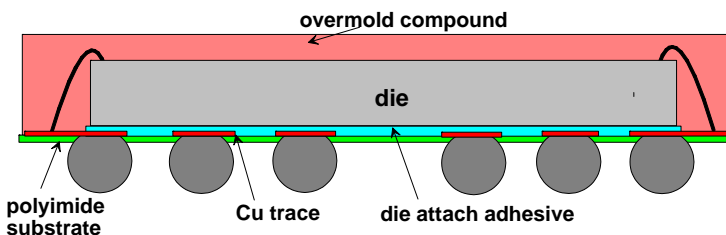


Figure 5: Cavity up TBGA (reduced to a CSP size).

circuit routing required to address mid to high pin counts (over 100) may well require 4 or more layers of board thus driving up the cost [5].

There are also several packages which have been introduced which have a similar structure to that described above with the exception that flex circuitry is used instead of a BT board. Those preparing to build such a structure include TI with their  $\mu$ Star<sup>TM</sup> (shown in Figure 4) [12] and Amkor/Anam with their *flexBGA*<sup>TM</sup> (shown in Figure 5). The finer pitch capability of flex circuitry enables routing on one metal layer for high pin counts thus providing the lowest cost substrate [5]. Once again, conventional processes are used for assembly, however the flexible nature of the tape can make it difficult to handle the material as a conventional leadframe. These handling issues can be overcome with special fixturing or by attaching a metal frame on the edge of the strip. This is a very attractive package structure, however its weakest area may be in board level reliability. With the rigid die so close to the solder joints, and only a thin die attach adhesive and a flex circuit separating them, the stress on the joints will be somewhat high.

In January of this year, the TI  $\mu$ Star<sup>TM</sup> was published to survive approximately 500 cycles of -25 to 125°C on a board [6]. Due to this limited level of reliability it had to be underfilled or mounted to an interposer for many applications, neither of which are desirable alternatives. For instance, when this package was used in the Sony DCR-PC7 digital camcorder it was first surface mounted to a 425 $\mu$ m thick circuit board and underfilled. The package was then cut out of the board and surface mounted to the motherboard in the unit. This added processing was presumably performed to improve board level reliability [13]. It was reported in a more recent paper [19], that improvements have been made to the solder alloy in the TI  $\mu$ Star<sup>TM</sup> package and that this improvement enabled passing 1000 thermal cycles from -40 to 125°C for a 0.8mm pitch ball layout. This capability will likely allow usage of this package in many hand held applications without the need for underfill but still may not be adequate for some of the more demanding environments such as personal computers and automotive applications.

The packages mentioned above are good constructions which should withstand the test of time and see a lot of use, however, each has its intrinsic limitations. This paper will disclose a new patent pending CSP package concept which was designed to address all the criteria mentioned above as well as others. Additional considerations with varying degrees of importance (depending on the application) would include electrical and thermal performance, moisture resistance, and the ability to shrink the die without having to change tape layout or the board foot print. These characteristics will be discussed as well as those described previously.

### Small Enhanced Flex Array Package

The package proposed in this paper utilizes a flexible circuit as the substrate to take advantage of the fine pitch capability for routing the dense ball arrays on a CSP at low cost. Current design rules allow 35 $\mu$ m lines and spaces with development underway for 25 $\mu$ m widths. In addition to routability, the fine pitch flex circuit enables the wire bond pads to be positioned as closely as possible to the die to enable minimization of the both the die size and the package size. For instance one may design a 90 $\mu$ m wide pad with a 35 $\mu$ m space for a total pitch of 125 $\mu$ m. The minimum pitch on a BT substrate using a 90 $\mu$ m pad would be approximately 165 $\mu$ m. The finer pad pitch enables die shrink while keeping the length of the bond wires relatively short. Electrical self inductance is also reduced considerably by minimizing the wire length in this manner.

The novel aspect of this new package structure is that a thin 5 mil copper leadframe is laminated to the flex circuit in the manner shown in Figure 6 and 7. Slots are formed in the leadframe and in the adhesive layer to enable wire bonding to the bond pads on the flex. Solder ball locations are formed by chemical etching of holes in the polyimide to expose the ball pads. This process eliminates the need for a soldermask material in the product. In addition, the tapered sidewalls of the polyimide eliminates any stress points in the solder ball itself which has been found to improve the shear strength and the fatigue life, as documented in a recent paper [14]. This aspect will be discussed in more detail in the mechanical modeling section. An actual laminated strip of this product is shown in Figure 8 and an SEM micrograph of the etched ball pad openings is shown in Figure 9. Figure 10 reveals the slot region next to the die pad in which the wire bond pads are located.

Although many applications would call for a configuration in which the die faces upwards (away from the circuit board), there are some applications which would benefit from a die face down configuration. For example, in the case of DRAM devices the bond pads tend to run down the center of the die as opposed to the perimeter. The copper interposer in strip format can be used in this situation as well, see Figure 11. In this case a slot is left open down the center of the substrate so when the die is mounted, wire bonding can be performed in the slot region. This slot region is then encapsulated with resin, solder balls are attached, and the package is diced from the strip. Those familiar with the 3M TBGA [15,16,17] will notice that the structure described is basically the same technology except on a smaller scale. Once again the substrate can be handled in standard strip format with the copper layer providing CTE matching to the circuit board for improved board level reliability. An additional benefit is that the copper layer shields the sensitive die face from alpha particles emitted from lead in the solder balls.

### Infrastructure Fit

This proposed CSP construction fits the existing assembly infrastructure since the substrate is rigid enough to be handled in a strip form similar to conventional QFP leadframes. In addition, conventional processes are used for assembly. With the cavity up configuration, the die is attached directly to the copper die pad using commercially available low modulus die attach adhesives. These are the same adhesives typically used for most PBGAs or QFPs today. Standard wire bonding is performed from the perimeter of the die to the pads on the edge of the flex circuit. The path of the bonding tip is programmed such that the wire does not contact the edge of the copper pad. Finally, conventional overmolding or encapsulating is performed followed by ball attach and excise from the strip. Excise can be accomplished by either a standard punching process or by dicing with a saw. No undesirable silicone materials are present in the system.

For the cavity down configuration, the die is attached to the copper strip with standard adhesives used for lead on chip assembly. Wire bonding is performed and the cavity is filled with encapsulant followed by ball attach and excise.

### Board Level Reliability

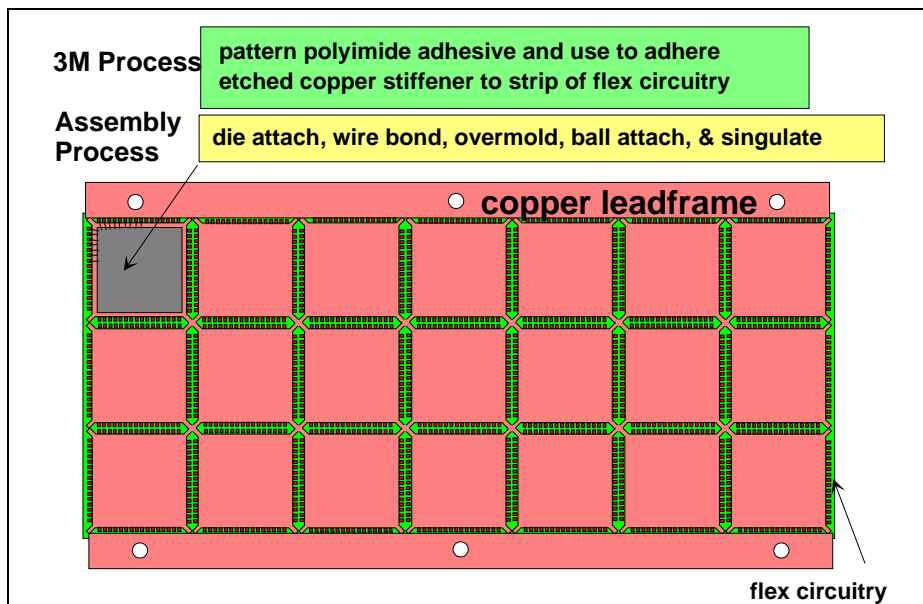


Figure 6: Flex circuitry laminated to copper strip with windows for wire bonding. Die is attached to copper with standard low stress leadframe adhesives.

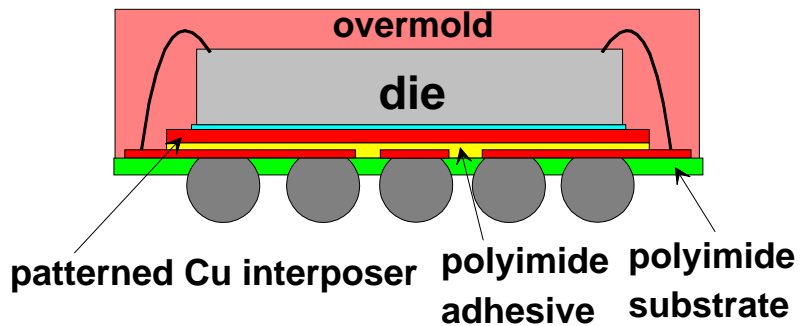


Figure 7: Cross sectional drawing of the assembled small enhanced flex array package with copper interposer.

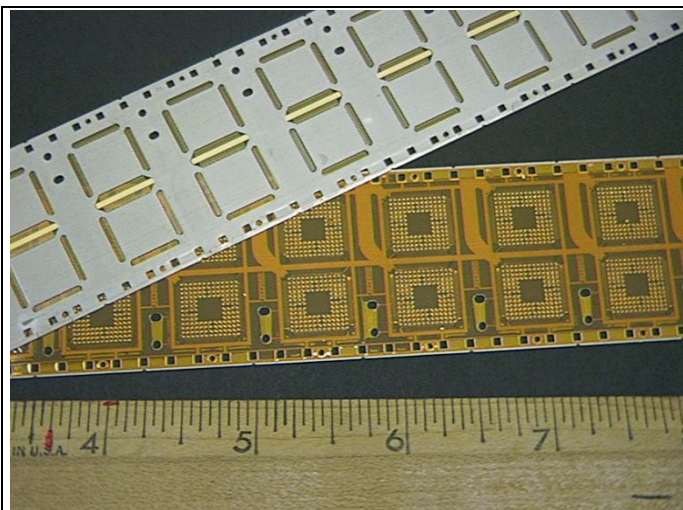


Figure 8: Front and back of the enhanced flex CSP carrier strip for a 12mm 144i/o package.

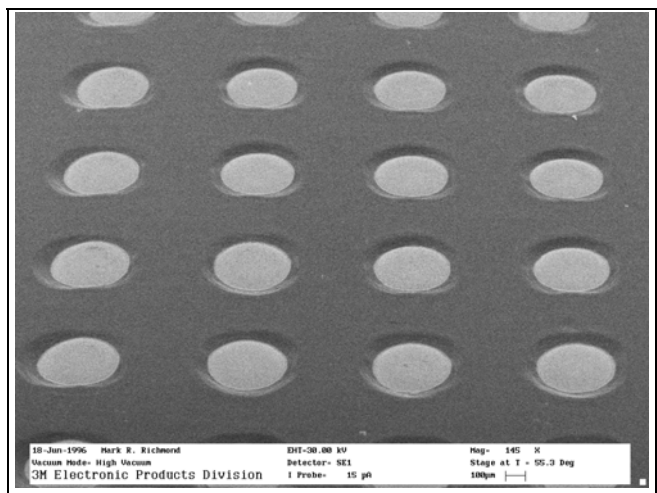


Figure 9: Ball pad openings etched in the poly-imide substrate (375µm opening on 800µm pitch).

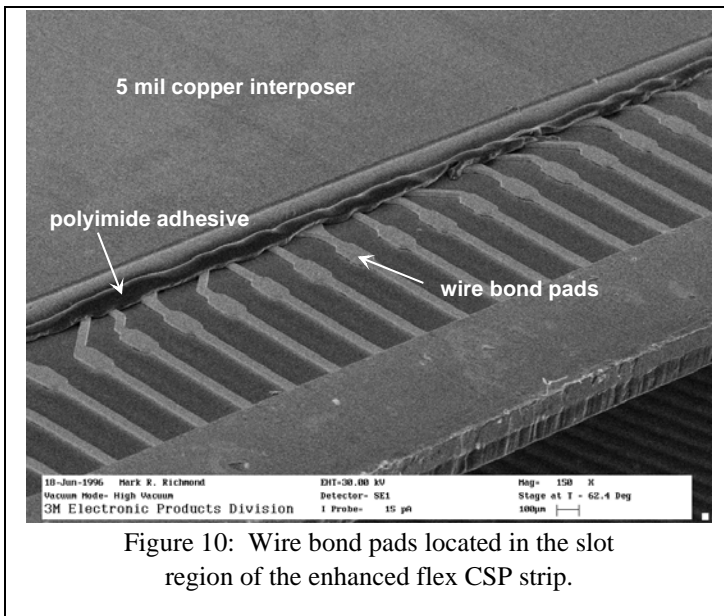


Figure 10: Wire bond pads located in the slot region of the enhanced flex CSP strip.

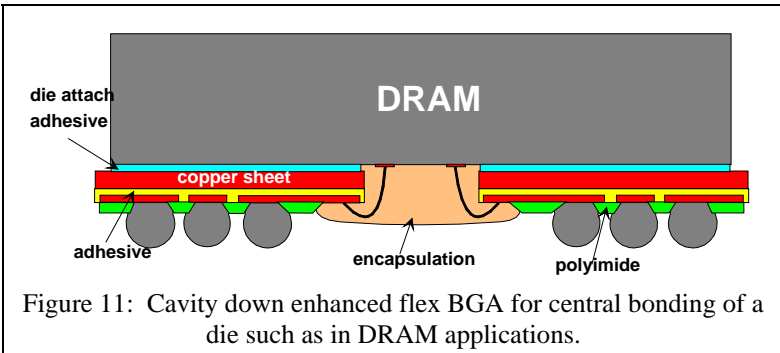


Figure 11: Cavity down enhanced flex BGA for central bonding of a die such as in DRAM applications.

The requirement for good board level reliability is achieved with a combination of the copper interposer and the chemically etched solder ball pad openings. While the strategy behind the  $\mu$ BGA<sup>TM</sup> is to use a compliant material to absorb the CTE mismatch strain between the die and the board, this new package uses the 5 mil copper layer to significantly reduce the strain by achieving better CTE matching between these materials. The copper layer has a CTE of 16.6 ppm/°C which matches closely with most circuit boards which are typically in the range of 15-19 ppm/°C. The largest CTE mismatch therefore occurs between the die and the hard spring temper copper layer. This mismatch is accommodated by the low modulus die attach adhesive. Mechanical modeling has been performed to estimate the stresses on the solder joints with this enhanced design compared to a design without the copper interposer. Such results will be discussed in more detail later.

The other important aspect of reliability is moisture resistance. Many users are requiring CSP packages to pass a JEDEC Level 2 moisture condition. This condition entails soaking the package for 168 hours at 85°C and 60%RH, followed by 3 reflow cycles which reach 220°C for 60 seconds. The packages are considered failures if moisture induced voids form in the adhesive, the die delaminates, or

the encapsulant material cracks. As of the writing of this paper, fully assembled packages have not yet been tested for moisture resistance. However, the substrate material itself has been tested and passes a JEDEC Level 1 condition. The excellent moisture resistance of the substrate is due to the high Tg and high modulus of the adhesive used for laminating the flex to the stiffener. The material used is a thermoplastic polyimide with a Tg near 220°C. This property combined with the excellent adhesion to the substrate and stiffener enables moisture taken up by the polyimide substrate to escape out the surface of the tape during reflow conditions rather than creating voids at the adhesive/substrate interface. The copper plane interposer also prevents moisture in the polyimide substrate from creating voids at the die attach adhesive interface. With the proper selection of die attach material and mold compound, a Level 2 or better is expected for this package.

Pressure cooker testing is also a fairly difficult requirement for IC packages. Exposure to 121°C at 2 atmospheres of pressure for up to 240 hours will expose weaknesses in adhesion between layers of materials in a package. Materials such as soldermasks have been known to have difficulty passing this type of test as have various adhesive interfaces. Again, as of this writing fully assembled packages have not completed testing of this nature, however, this combination of materials and interfaces has previously been demonstrated to pass such testing in the TBGA structure<sup>14</sup>. For instance, this enhanced laminated substrate has been shown to pass 240 hours of PCT without delamination and die attach and overmolding to copper leadframes are well known materials and interfaces in standard QFPs. Consequently, no trouble is expected with this type of test, however, this will be verified with testing in the months ahead.

### Package Cost

The third requirement was to achieve a package cost of 0.8 cents/pin at high volume which would enable the package to compete favorably with TSOPs. When end users grow accustomed to paying a certain price for small packages like TSOPs they are very reluctant to pay more for a CSP even though it may bring more value in the form of higher density and improved reliability. As the cost of CSPs continues to decrease towards 0.8 cents/pin they will displace more and more TSOPs and those CSPs that lead the way will gain most of the market share. Packages such as the *flexBGA*<sup>TM</sup> and  $\mu$ Star<sup>TM</sup> are positioned well in this respect. Although the enhanced CSP presented in this paper would be slightly more costly than these due to the added copper interposer, it can still achieve the low package cost target at sufficient volume. Afterall, it is simply composed of a flex circuit adhered to a standard leadframe material. The only raw

materials in the substrate are copper and polyimide; materials such as an epoxy soldermasks have been eliminated. By keeping the structure as simple and manufacturable as possible and by maximizing the number of packages per unit area in a strip, the identified target can be met (of course, this will also depend on the number of i/o and the size of the package).

An important factor to consider in the total cost of a package is the versatility of a single package layout to fit various sized die. As line width capabilities on the silicon continue to shrink from 0.35um to 0.25um and below, die designers continually strive to shrink the size of the die itself to reduce its cost. The enhanced flex CSP package enables the die to be shrunk while still using the same package layout. The ball pattern remains the same and the same wire bond pad layout on the flex can still be used. Other CSP solutions such as the  $\mu$ BGA<sup>TM</sup> must have the tape redesigned to ensure that each frangible lead lines up with the new pad locations on the die. The ball locations may even need to be moved resulting in expensive changes to the circuit board. To minimize cost with flex circuit substrates, high volumes of material must be run. This economy of scale is more easily accomplished if the same circuit pattern can be used for various sized die with different wire bond pad locations and if some ball locations are allowed to fall outside the edge of the shrinking die.

**Electrical and Thermal**

Improvements in electrical and thermal performance are required in an increasing number of IC package applications. The copper plane in this enhanced flex CSP lies only 25um away from the signal traces on the flex and therefore provides an excellent reference plane which reduces inductance on the traces and the cross talk between them [18]. Future high speed applications could also employ wire bonding directly to the copper interposer to create an active ground plane.

For many ICs such as memory or low end DSPs which run at 1 watt of power or less almost any CSP package will suffice. However, for ICs such as high end DSPs or microcontrollers which are above 1 watt, one needs to take into account the thermal efficiency of the package. A package such as the  $\mu$ BGA<sup>TM</sup> has the die isolated from the solder balls by the thick elastomer layer, therefore, the heat must escape from the backside of the die. This is not a thermally efficient design unless a heat sink is utilized, but then issues such as added cost and the effect on package size and reliability would need to be taken into account. For instance, if a heat sink were to increase the area of the package then it may be more advantageous to simply use a larger package which can handle the heat.

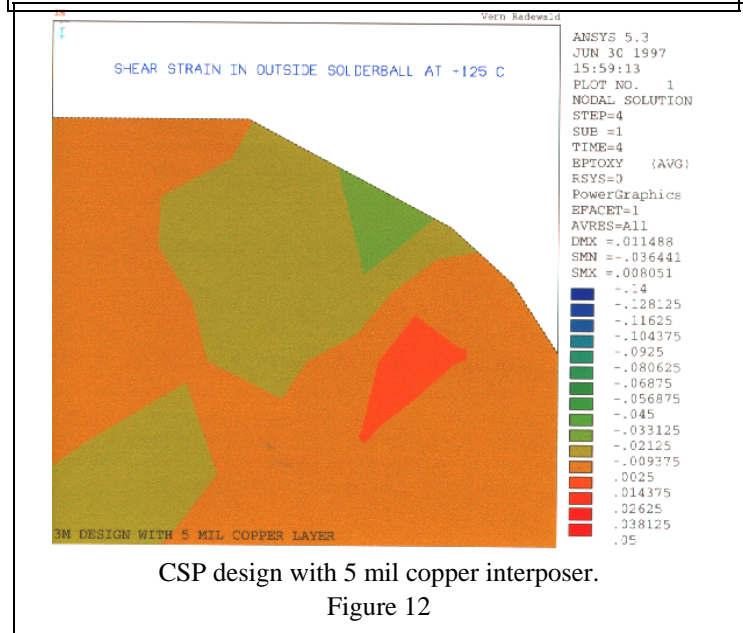
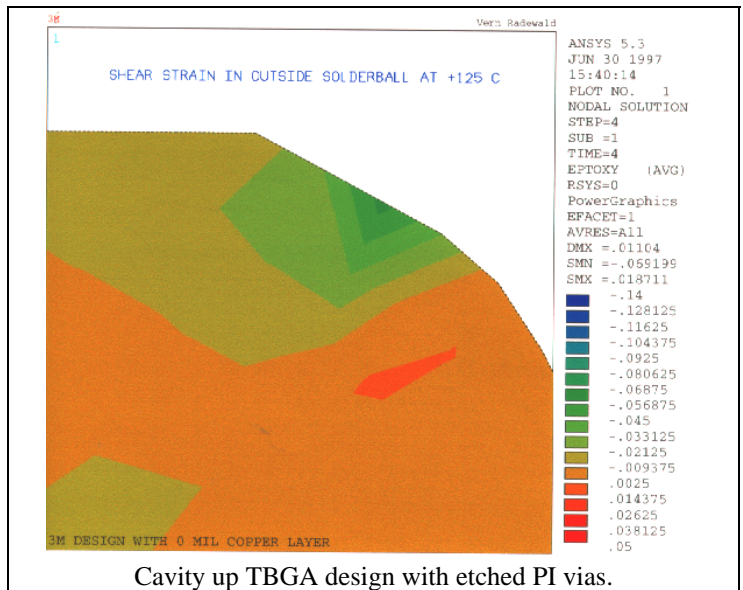
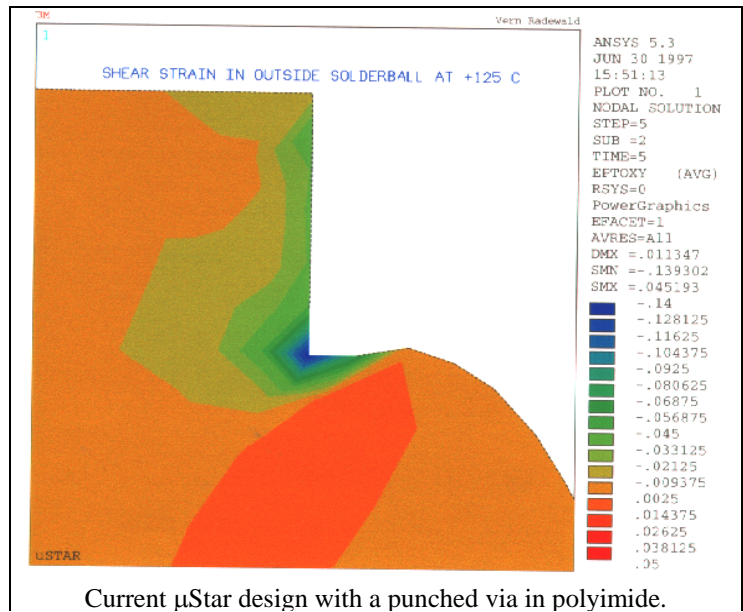


Figure 12

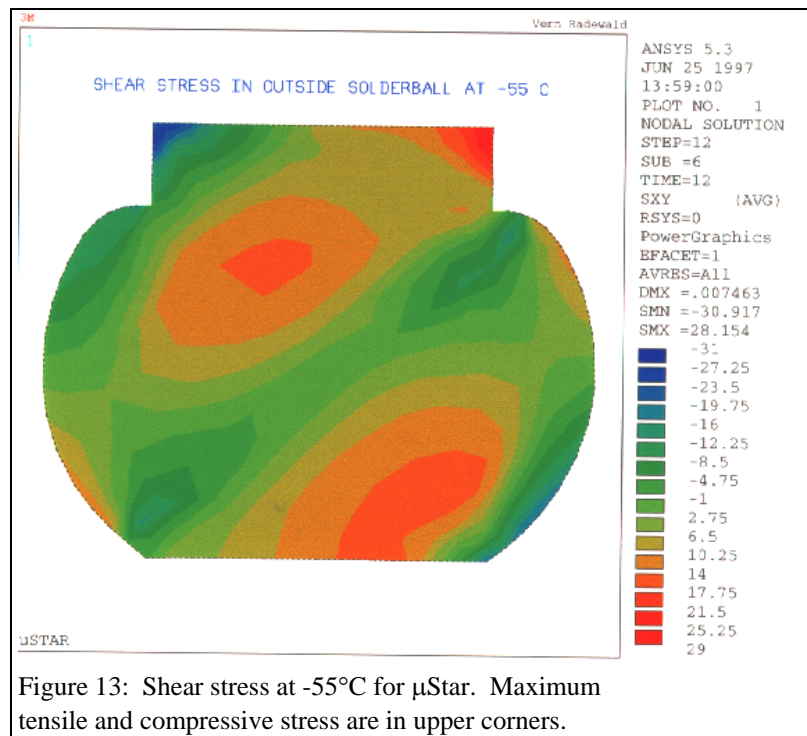
The new enhanced CSP with copper interposer enables most of the heat from the die to be dissipated into the circuit board through the solder balls thereby making the package intrinsically more thermally efficient. When a thermally conductive die attach adhesive is used the only non conductive dielectric layer is the 25 $\mu$ m of polyimide adhesive between the stiffener and the solder ball capture pads. Therefore, the heat is spread efficiently along the copper interposer and down into the circuit board.

### Mechanical Modeling

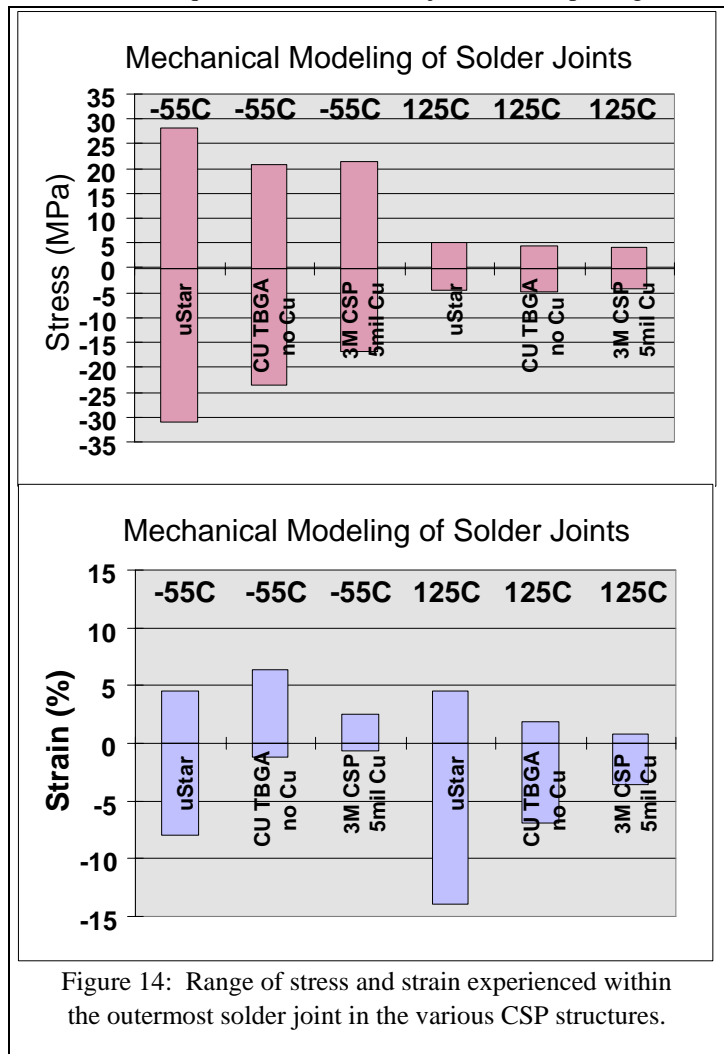
In lieu of actual board level thermal cycle reliability data at this time, mechanical modeling was performed to determine the maximum solder joint stresses and strains one might expect with this enhanced CSP package. Ansys 5.3 software was used to generate the models. Models were created to compare the stresses and strains in the solder joints of a package mounted to a standard circuit board (CTE of 15ppm/ $^{\circ}$ C). The enhanced CSP was modeled with a 5 mil (125 $\mu$ m) thick copper interposer. In addition, a small cavity up TBGA without the copper interposer (i.e. *flexBGA*<sup>TM</sup>) and a standard TI  $\mu$ Star<sup>TM</sup> construction were modeled for comparison.

The package modeled in each case was a 12 x 12mm package with 144 solder balls at a 0.8mm ball pitch. A two dimensional nonlinear model was created along the diagonal axis of the package. Therefore the solder joints evaluated were those with greatest stress at the furthest distance from the neutral point. A 500 $\mu$ m (20 mil) solder ball was modeled with a 375 $\mu$ m ball pad diameter on both the package and the circuit board. Table 1 shows other important properties such as CTE and elastic modulus values used in the model. Stress strain curves for eutectic solder at temperatures ranging from -65 $^{\circ}$ C to 125 $^{\circ}$ C were inputted so the nonlinear plastic characteristics of the solder would be taken into account. In creating the model, the boundary conditions were set such that the package was constrained from movement at its center and the package and board were constrained from bending in the Z-direction during thermal cycling to ensure that the primary forces were shear in nature. With each model the temperature was cycled from 20 $^{\circ}$ C to 125 $^{\circ}$ C and then down to -55 $^{\circ}$ C. The stresses and strains in the outermost solder joint (furthest from neutral point) at the temperature extremes were plotted to determine the location and magnitude of the maximum tensile and compressive values with each design modeled.

An example of a shear strain model at 125 $^{\circ}$ C for the various designs is shown in Figure 12. This figure only



shows one quadrant of the solder joint (on the package side)



in order to better distinguish the strain contours. From these results it is apparent that when a punched via is used as with the current  $\mu$ Star<sup>TM</sup> product, the sharp edge of the punched hole creates a stress concentration site. With concentration of stress and strain at this location, one might expect a fatigue crack to form here during thermal cycling and progress through the joint to failure. Chemical etching of the via through the polyimide substrate creates a tapered slope which eliminates any dielectric material from impinging into the solder ball and causing a stress riser. Consequently the stress and strain is spread over a larger area and is considerably less at these temperature extremes. This effect is readily apparent by comparing the CU TBGA structure to the  $\mu$ Star<sup>TM</sup>. In both cases the die is effectively mounted directly to the surface of the flex, however, the percent strain values are considerably less with the CU TBGA structure due to the chemically etched vias. The strain is reduced further by the 5 mil thick copper interposer in the proposed design.

In addition to stress riser at the bottom corner of the punched hole, one also exists at the top corner where the solder ball is attached to the copper pad. This is apparent from the shear stress model at -55°C shown in Figure 13. Thus one would also expect to see some cracks initiating at the solder to pad interface.

Instead of showing the stress and strain diagrams of each individual model at the temperature extremes, a bar chart was used to capture the maximum tensile and compressive values in the solder joint for each condition, as shown in Figure 14. It can be seen that the addition of the 5 mil thick copper interposer, produces the overall lowest values of tensile and compressive stress and strain in the solder joint. Note that the range of stress in the solder joint at a temperature of 125°C is nearly identical for each structure. This effect is due to the low yield strength and high plasticity of solder at this elevated temperature. Since very little displacement causes plastic deformation, the more important component to note at 125°C is the range of strain experienced.

Although this modeling provides good insight of the magnitude and location of stresses in the system, it will not reveal exactly how many temperature cycles a product will survive on a circuit board. This is due to the large number of variables involved in taking the next step from calculating the maximum stress and strain in the solder joint to determining the fatigue life. The total fatigue life is the sum of the cycles required to initiate a crack and the cycles required to progress this crack to failure. It is very difficult to reliably calculate precisely how many thermal cycles are required to initiate a fatigue crack and this initiation may account for a large portion of the total fatigue life of the joint.

Even though this model certainly seems to indicate superior board level thermal cycle reliability with this enhanced CSP structure with copper interposer, actual testing is required to determine its life. To be used in applications such as portable computers or automobiles, one would expect board level performance on par with PBGA or QFP packages (i.e. greater than 3000 cycles -40/125°C). There is a good chance of achieving this goal considering that the enhanced CSP appears to offer a significant improvement over the current  $\mu$ Star<sup>TM</sup> configuration which had been reported to survive over 1000 cycles of -40/125°C at board level [19]. Since the copper interposer also reduces the stresses and strains from a comparable package without the interposer (i.e. cavity up TBGA) one would expect the enhanced CSP to show some board level performance improvement over this package structure as well. Actual testing will be taking place in the months ahead.

### Assembly

These 12mm 144I/O enhanced CSP packages have been assembled with 9.8 mm daisy chain test die. The die were attached with a standard die adhesive and were wire bonded with 30 $\mu$ m gold wire. They were overmolded and 0.5mm eutectic solder balls were attached to the 375 $\mu$ m pads, as shown in Figure 15 and 16. The initial units were singulated from the strip by sawing. The mean shear strength of 100 balls (20 from 5 separate packages) was 676 grams with a standard deviation of 48 grams. Solder ball coplanarity was measured on 77 parts with a mean of 1.436 mils and a standard deviation of 0.033 mils. Thus the coplanarity appears to be very good and tightly controlled.

### Discussion

The field of chip scale packaging has been incredibly active in the past couple years with many new product concepts being revealed each month. As with standard IC packaging, it is unlikely that any single CSP will win out completely. If there is anything that history has taught us it is this, the packages that will be most successful will be those that best fit the existing infrastructure for both package assembly and board assembly. The packages that meet these objectives and are reasonably low cost and reliable will have a bright future. Those that do not will primarily be used for niche applications where their specific strengths are of greatest value. Keep in mind that some of these niche markets may be quite substantial. For instance the  $\mu$ BGA<sup>TM</sup> is well positioned to capture the flash memory business since it offers a true chip size package (the smallest possible). It also fits well in this area since this type of die does not undergo as many modifications (die shrinks) and the size of the business is large enough to drive the necessary infrastructure changes. However, in more standard IC markets where one more regularly sees changes in die shape, size, and bond pad layout, the  $\mu$ BGA<sup>TM</sup> package may not be the package of choice due to the tooling changes and associated lead times required for each new circuit configuration.

Table 1: Parameters used in mechanical model of solder joints.

<b>μStar</b>							
Item	Material	Dimensions	CTE (ppm/oC)	Thickness	Pitch	Poissons	Modulus (MPa)
Base	UPILEX-S	12mmx12mm	8	75μm		0.34*	8240
Copper	VLP Cu	12mmx12mm	16.6	25μm		NA	118590
Adhesive	TOMOEGAWA X Type	12mmx12mm	60/C@25C 160/C@104C	12μm		0.467	1961 118590
Capture pad	Au over Ni over Cu	478μm X 478μm	16.6	.5μm Au/Ni 1milCu	800μm cen. to cen.	NA	NA
Resist	CCR 240GS	NA	100	25μm		0.3*	4903
Array	NA	13x13 4row pop.	NA	NA	800μm	NA	NA
Via (punched)	NA	375μm	NA	NA	800μm	NA	NA
Solder ball	Eutectic 63/37	500μm	24.7	NA	800μm	NA	See Attached Stress/Strian Curve
Test Board	FR4		15	1.6mm		NA	36124
Die Attach		NA	40	25.4μm		0.3	**
Die	Silicon	10mm X 10mm	2.1	279μm		NA	130312
Overbold		12mmx12mm	17.1	800μm			25924
<b>3M CSP</b>							
Item	Material	Dimensions	CTE (ppm/oC)	Thickness	Pitch	Poisson's	Modulus (MPa)
Base	Polyimide E-film	12mmx12mm	13	50μm	NA	0.34*	5515
Copper	EHS 194 alloy	12mmx12mm	16.6	25μm & 125μm		NA	118590
Adhesive	KJ	12mmx12mm	60	50μm		0.34*	2758
Capture pad	Au over Ni over Cu	478μm X 478μm	16.6	.5μm Au/Ni 1milCu	800μm cen. to cen.	NA	118590
Array	NA	13x13 4row pop.	NA	NA	800μm	NA	NA
Via	NA	375μm	NA	NA	800μm	NA	NA
Solder ball	Eutectic 63/37	500μm	24.7	NA	800μm	NA	See Attached Stress/Strian Curve
Test Board	FR4		15	1.6mm		NA	36124
Die Attach		NA	40	25.4μm		0.3*	**
Die	Silicon	10mm X 10mm	2.1	279μm		NA	130312
Overmold		12mmx12mm	17.1	800μm		NA	25924

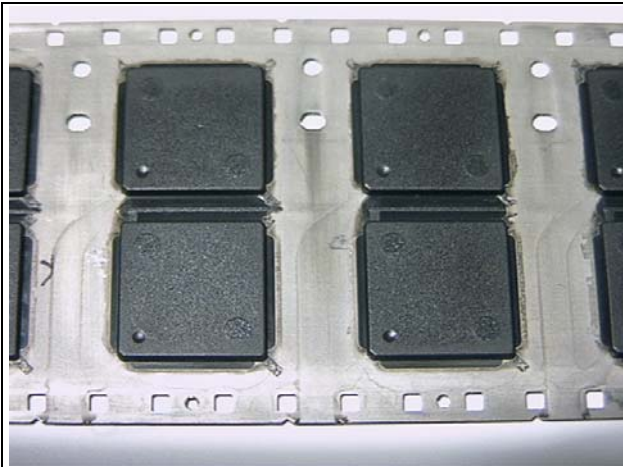


Figure 15: Overmolded side of enhanced CSP.

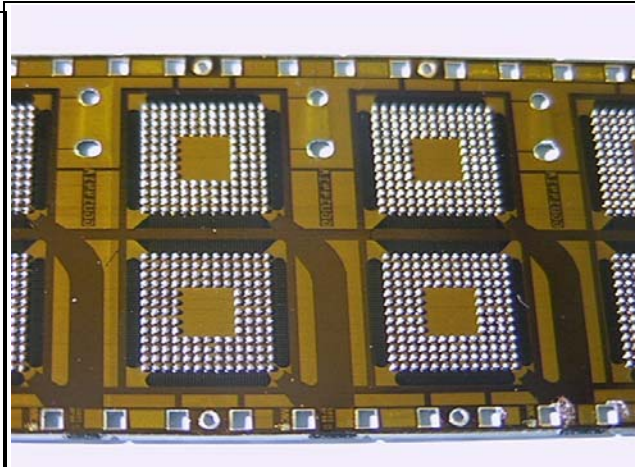


Figure 16: Solder ball side of assembled CSP.

Since cost is of high importance in most chip scale package applications, we may also see product groups make packaging decisions based more on what level of reliability performance is required for a particular application. For instance, if a CSP without the copper interposer meets the lower performance requirements of a pager application and is slightly lower cost than a more reliable product with the interposer, then the decision may be to go with the lower cost package and only use the enhanced package where it is truly needed. Other product groups may decide that simply sticking with an enhanced CSP which will meet all levels of performance is the desirable path, since saving a few cents on the package for some applications doesn't justify having an increased package mix to deal with. The message here is simply that although the number of viable CSPs will

certainly begin to decrease over the next few years due to economic Darwinism, it is unlikely the number will go to one or two. A number in the range of 5 to 10 is more likely.

#### Future Work

The laminated carrier strip is currently being produced in prototype volumes for both a cavity up configuration and a cavity down configuration (DRAM). These strips are being assembled with wire bonded die and will be subjected to reliability testing in the coming months. Initial qualifications should be complete by the of 4Q97 and it is expected that this product will be available for limited release by early 2Q98.

## Conclusion

If the level of interest shown today is at all indicative of future usage of CSPs, this portion of the packaging industry has many bright days ahead. An increasing number of people in the industry are recognizing the value of chip scale packages over direct flip chip attach to the board due to the better infrastructure fit. Since there are a large number of factors which are considered when selecting a package for a specific application, it is clear that no single package configuration will win all of the market. However, for a package to be among the most popular it must have a reasonably low cost, be reliable, and enable package assembly with existing infrastructure. Second tier considerations may include factors such as improved electrical/thermal characteristics or having the versatility to use the same package for different die sizes (to accommodate die shrink). The package concept outlined in this paper has the potential of meeting all these criteria and therefore shows tremendous promise for a great number of applications.

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