

Cunningham, J, Valentin, R., Hillman, C., Dasgupta, A., and Osterman, M., "A Demonstration of Virtual Qualification for the Design of Electronic Hardware", ESTECH 2001, IEST, Phoenix, AZ, April 2001.

A Demonstration of Virtual Qualification for the Design of Electronic Hardware

J. Cunningham - *Honeywell Corporation, Tucson, Arizona*
 R. Valentin, C. Hillman, A. Dasgupta, and M. Osterman - *CALCE Electronic Products and System Center, University of Maryland.*

Abstract

This paper presents a demonstration of a process and software for evaluating the ability of an electronic product to operate with out failure under anticipated life cycle loading conditions. For this purpose, a preliminary design for an electronic module that is being developed to support aircraft engines was selected and evaluated. The process included developing a model of the physical hardware, characterizing the anticipated operating conditions, performing load transformation, and conducting failure assessment. Results indicate that preliminary design would not meet design objectives and these results were confirmed by physical testing. As a result, design changes are being pursued to ensure a reliable product.

Keywords:

Virtual Qualification, Physics of Failure, Circuit Card Assemblies, Interconnect Failure

Introduction

Computer simulations have been used in the development products for over two decades. However, the electronic industry has been slow to adopt the methodology for assessing the reliability of electronic products. Instead, statistical reliability standards, based on questionable data tables have been applied. While this process seeks to quantify product reliability, the validity of the results and the usefulness of the process has been seriously questioned because it does not address the fundamental physics involved in the failure of electronic products [1]. Accurate evaluation of product reliability requires the application of scientific principles and an understanding of the physical process that produce failure [2, 3]. This concept extends to physical testing which has been a critical method for assuring that products will meet design requirements.

Improvement in the development time of electronic systems depends upon the increasing use of simulation during the product design phase. This is especially true for circuit card assemblies, which are the major building blocks of all electronic systems. Simulation of electrical behavior of

electronic hardware is commonplace, however simulation of the failure behavior of the hardware is less frequently used. While general-purpose software, such as Ansys, Abaqus, Flotherm and IcePack, are used to evaluate stress within electronic assemblies, time constraints tend to prevent analysis of individual parts and components. Further, stress simulations alone do not reveal product reliability. Significant time savings can be realized when engineers develop a flow-through process of life-cycle characterization, product modeling, load transformation, and failure assessment to qualify electronic systems. This process is termed virtual qualification (VQ).

Over the past several years, the CALCE Electronic Products and System Center (EPSC) at the University of Maryland has demonstrated the use of virtual qualification as part of an overall Physics of Failure (PoF) approach to ensuring product reliability [2]. Virtual qualification is a methodology for assessing and improving the durability of electronic equipment through the use of validated failure models/simulation tools. It is also an important step in developing effective physical tests to verify product reliability. The application of virtual qualification has led to significant cost saving by commercial and military organizations. The technique involves the application of simulation software to model physical hardware to determine the probability of the system meeting desired life goals. At CALCE, virtual qualification is performed using calcePWA software.

This report highlights virtual qualification of an electronic module being designed by the Honeywell Corporation. The electronic module consists of an enclosure that houses three circuit card assemblies. The module is expected to have a field life of 10 years under conditions that include both temperature cycling and vibration. A prototype of the module is depicted in Figure 1.

In the next section, a general background for virtual qualification is presented. This section is followed by a discussion of the process as it is applied to the Honeywell electronic module. Finally, the results of the virtual qualification are confirmed by physical testing.

Background

Traditional test strategies for qualifying products depend on the ability of products to withstand standard industry tests. As a result, a design-build-test-fix methodology was developed to assure that the product could survive the qualification test. This method worked by over designing the structure or by trial and error fixes to enable the product to defeat the specified test conditions. Unfortunately, the process is not cost effective and it does not necessarily ensure that the product will survive under actual use conditions. Further, the strategies have become less feasible given the rapid advancement in materials and technology. Problems also arise because in traditional accelerated testing, failure identification and root-cause analysis are not adequately emphasized [5].

To combat this problem, CALCE has developed an accelerated product qualification process that emphasizes an understanding of the physical process that produce failures in electronic systems [6,7]. Paramount to this process is the application of simulation techniques to rapidly identify potential failure sites and to quantify and rank the potential failure in the order in which they are likely to occur. Over the past 15 years, CALCE EPSC, in collaboration with its industry sponsors, has developed and continues to enhance software for performing virtual qualification on electronic hardware. The software, calcePWA, has been used on multiple programs and has been identified as a being instrumental in improving designs and has resulted in significant cost savings [8-9].

The software has been implemented to provide the following capabilities

1. Thermal analysis
2. Vibration analysis
3. Failure assessment
 - a. Identification of weak-links in the assembly design
 - b. Ranking of potential failure mechanisms
 - c. Estimation of operational lifetime, based upon identified failure mechanisms

The software is meant to provide a rapid assessment. As such, the software has limited capability for conducting parametric studies and is not meant to replace sophisticated general-purpose analysis tools. It is rather designed to evaluate nominal designs. The PoF activities of virtual qualification, as detailed in Figure 2, include information gathering, stress analysis, and damage assessment.

In this age of competitive markets, this software provides the user with the ability to rapidly evaluate product reliability and to design accelerated tests

Virtual Qualification (VQ) Case Study

Virtual qualification was performed on an electronic module composed of an enclosure that houses three circuit card

assemblies (CCAs). The enclosure, which is design to be mounted directly on an aircraft engine, is constructed of aluminum, provides mounting points for the CCAs. The process for conducting VQ on the three CCAs is presented in the remainder of this section.

Modeling Considerations

The goal of this step is to identify and document part information, board architecture and material properties. The accuracy and detail of the information gathered during this step will have a great effect on the accuracy of the results. Architectural details are required for all parts, connectors, and substrates in the assembly. Information can include physical dimensions, functionality, and constitutive elements. Comprehensive documentation, which can include lists of materials, manufacturers' data books, and layout information, is important for accurate PoF analysis.

The PoF methodology accentuates understanding the material behavior and therefore requires that all the intrinsic material properties be identified and documented. This includes part information (substrate material, encapsulants and underfills, leads and platings), interconnects (solder composition, conductive adhesives, socket materials), and the makeup of the printed wiring board (laminates and resin system, metalization, embedded passives). The properties of the identified materials can then be retrieved from the CALCE Materials Database and used for the stress modeling. If certain constitutive properties are not well understood or are missing from the materials database, further characterization of material properties may be necessary.

To facilitate the application of the virtual qualification process, various interfaces are provided to electronic design automation (EDA) software. For this study, the model development was greatly assisted by the use of design files generated by Mentor's Board Station software. The Board Station software is the design tool for generating electronic designs and allows interfacing with computed aid manufacturing tools. While the layout and function of the three CCAs vary, each CCA, shown in Figure 3, has essentially the same board construction and share a number of common parts.

The printed wiring boards were 1.8 mm thick and consisted of ten electrical layers. The epoxy resin was based on IPC-4101/24, which specifies fire retardancy and a glass transition temperature of 150-200°C. Estimated material properties of the printed wiring board are listed in Table 1. The attach material was eutectic solder with a nominal thickness of 5 mils (0.127 mm).

Specification	IPC-4101/24
Type	FR-4
Glass Transition Temp. (T_g)	150-200oC
Coefficient of Thermal Exp. (CTE)	16 x 10 ⁻⁶
Elastic Modulus	27.5 Gpa
Poisson's Ratio	0.15

Table 1: Estimated material properties of the printed board

Life Cycle Load Characterization

The expected life-cycle environment is displayed in Figure 4. Concurrent to the hardware modeling (design capture) process, a separate effort is required to identify and record the operational-use environments of the product. Operational-use environment information requires knowing the environmental loads to which a part is subjected. Examples include temperature cycle limits, average temperature, frequency of temperature cycles, humidity conditions, mechanical vibration, electrical loads, etc. The level of these experienced loads should be accompanied with details of rate of change and duration of exposure. The design, destruct, specification and operating limits of the specimen are determined. Loads experienced by parts during assembly, transportation, storage, handling and rework can also be taken into account. Life cycle loads can be obtained based upon interviews with the manufacturer and the end-user, data from sensors placed on the part during operation, or prior experience with similar hardware and applications.

The life cycle loads¹ used in this study were provided by Honeywell and were taken sensors located in the actual operating environment. The anticipated temperature condition was determined to be rather complex, with a temperature cycle that is expected to occur up to five times a day. For this analysis, the temperature cycle was simplified and divided in two segments (see Figure 4). This approximation is not expected to produce significant variation in the final life assessment. Table 3 describes the life profile that was used in this durability assessment.

¹ Vibration was not considered in this failure assessment

Use Category	T _{min} (°C)	T _{max} (°C)	Ramp time to T _{max} /to T _{min}	Dwell at T _{max} /T _{min}	Time of Cycles	Total time
Section 1	9.5	49	35 min/ 35 min	25 min/30 min	175 min	365 days/ 10 year
Section 2	125	82	50 min/ 15 min	35 min/30 min	160 min	365 days/ 10 year

Table 3. Temperature usage and qualification profiles

Stress Assessment

The calcePWA software was used to evaluate the component and the board temperatures under normal operation. Since the transient temperature variations are not expected to produce significant variations in the final failure assessment results, only the operating temperatures of the individual components at the limits of the temperature cycles were evaluated. Based on a review of the assembly, a pure conduction analysis was performed on each CCA with the edges of the CCAs set to the ambient condition. Under the pure conduction analysis, heat loss from the top and bottom surfaces of the CCA is assumed to be negligible. For this type of evaluation, the temperature results are expected to be conservative (higher than actual).

Power dissipation rates of the components on each CCA were derived from electrical simulation performed by the CCA design team. Figure 5 depicts temperature of the top layer of the CPU CCA as evaluated by calcePWA for an ambient condition of 82 °C. In this study, the CPU board saw up to 12 degrees Celsius rise over boundary conditions. The I/O board and EMI board have a 2.5 degree Celsius rise and 0.5 degree Celsius rise, respectively.

To verify the results of the software analysis, the CCA design team applied thermocouples to various locations on the CPU CCA and electrically powered the card in the module. A comparison of some of the temperatures recorded for various components on the CPU CCA are provided in Table 4. The predicted temperatures were found to match quite well with the experimental measurements.

Component	Experimental °C	CalcePWA °C
U114	89.0	90.3
U90	92.1	93.0
CR47/CR48	92.7	104.7/101.9
CR35/CR38	100.0	100.0/90.3
U34	92.7	88.4
U66	87.8	93.4
U46	86.6	89.8
U56	90.8	85.1

Table 4. Temperature increase over boundary conditions of 82 °C for calcePWA and 83 °C for experiment

Failure Assessment

CalcePWA uses information on architecture, materials, and environmental to develop data models for potential failure sites. This data is then used to identify relevant failure mechanisms. After identifying the potential failure sites and failure mechanism, the software can be used to evaluate and rank the failure sites based on severity. In this study, the preliminary design was found to have insufficient design margins to withstand the anticipated use condition, with a life expectancy of less than six months under continuous operation. The most-likely failure sites based on severity are presented in Table 3.

COMPONENT	PACKAGE TYPE	ESTIMATED CYCLES TO FAILURE
Ceramic Clock Oscillator	Leadless Metal Chip Carrier	778
Bipolar Transistor	Small Outline Transistor (SOT)	4840
Ferrite Bead Inductor	Leadless Chip Capacitor (LCC)	15028

Table 3: Failure Assessment Results

Dimensional specifications and material properties of the three components can be seen in Figure 6 through Figure 8.

Validation of Virtual Qualification

To verify the virtual qualification results an oven temperature cycling test was conducted. The test cycle consisted of temperature limits between -50 to 125°C with the complete cycle lasting 45 minutes with 10-minute dwells. Simulation of this stress condition indicated a life expectancy of less than 300 temperature cycles for the ceramic oscillator. The results of the test closely matched the simulation results. Figure 9 depicts cracks that formed in the solder joint of the ceramic oscillator after less than 300 temperature cycles. A cross-section of this joint (Figure 10) shows that the interconnection has completely failed. Further cracks were also detected in solder joints for the SOT-23 and Ferrite Bead.

Summary

This study evaluated an electronic module that is being developed for an aircraft engine. The study presented the

virtual qualification approach and highlighted the calcePWA software. Analysis results indicated that the preliminary design does not meet the desired design objectives. Experimental testing has confirmed the virtual qualification results. Based on these results, design changes are being implemented to ensure that the electronic module will meet the design requirements. As presented in this paper, virtual qualification is a valuable tool and can be used to identify design deficiencies without the need for extensive physical testing. In this case testing of a preliminary design was performed as a means of building confidence in the application of virtual qualification in the design process. With increased confidence in the application of the virtual qualification, the amount of physical testing and product development can be significantly reduced.

Acknowledgements

The authors would like to thank Honeywell, the US Air Force, and the CALCE Center for supporting this effort. This work was supported in part by the Physics of Failure Approach to Sustainable Electronic Systems (PASES) contract from Air Force Research Laboratory and Wright-Patterson AFB, sponsored by the ManTech Sustainment Initiative, Manufacturing for Sustainment under contract F33615-99-2-5503.

References

- [1] Cushing, M. J., Mortin, D. E., Stadterman, T. J., & Malhotra, A., "Comparison of Electronics-Reliability Assessment Approaches", *IEEE Trans. Reliability*, Vol 42, Dec 1993.
- [2] Pecht, M., Dasgupta, A., & Barker, D., "The Reliability Physics Approach to Failure Prediction Modeling," *Quality and Reliability Engineering International*, pp. 276-273, 1990
- [3] Pecht, M., & Dasgupta, A., "Physics-of-failure: An Approach to Reliable Product Development", *Proceedings of Institute of Environmental Sciences*, Chicago, IL, pp.111-117, August 1995
- [4] Lall, P., and Pecht, M., "An Integrated Physics-of-Failure Approach to Reliability Assessment Advances in Electronic Packaging", *ASME EEP-Vol.4-1*, 1993
- [5] Larson, T., and Newell, J., "Test Philosophies for the New Millennium ", *Journal of the IES*, pp 22-27, May/June 1997
- [6] Caruso, H., and Dasgupta, A., "A Fundamental Overview of Analytical Accelerated Testing Models ", *Journal of IES*, vol 41, no.1, pp 16-30, January/February 1998.
- [7] Hu, J. M., Barker, D., Dasgupta, A., Arora, A., "The Role of Failure Mechanism Identification in

- Accelerated Testing", *Journal of the Institute of Environmental Science*, pp.39-45, July 1993.
- [8] Osterman, M. and Stadterman, T. "Failure-Assessment Software For Circuit-Card Assemblies", *Proc. for the Annual Reliability and Maintainability Symposium*, pp. 269-276, Jan 1999.
- [9] GRCI Inc., "*Reliability Assessment Process Improvement Demonstration (RAPID)*", Contract No: F33615-96-D-5302, Delivery Order 041, Subtask: 3.3, Prepared for ESC/DIT, 1998.

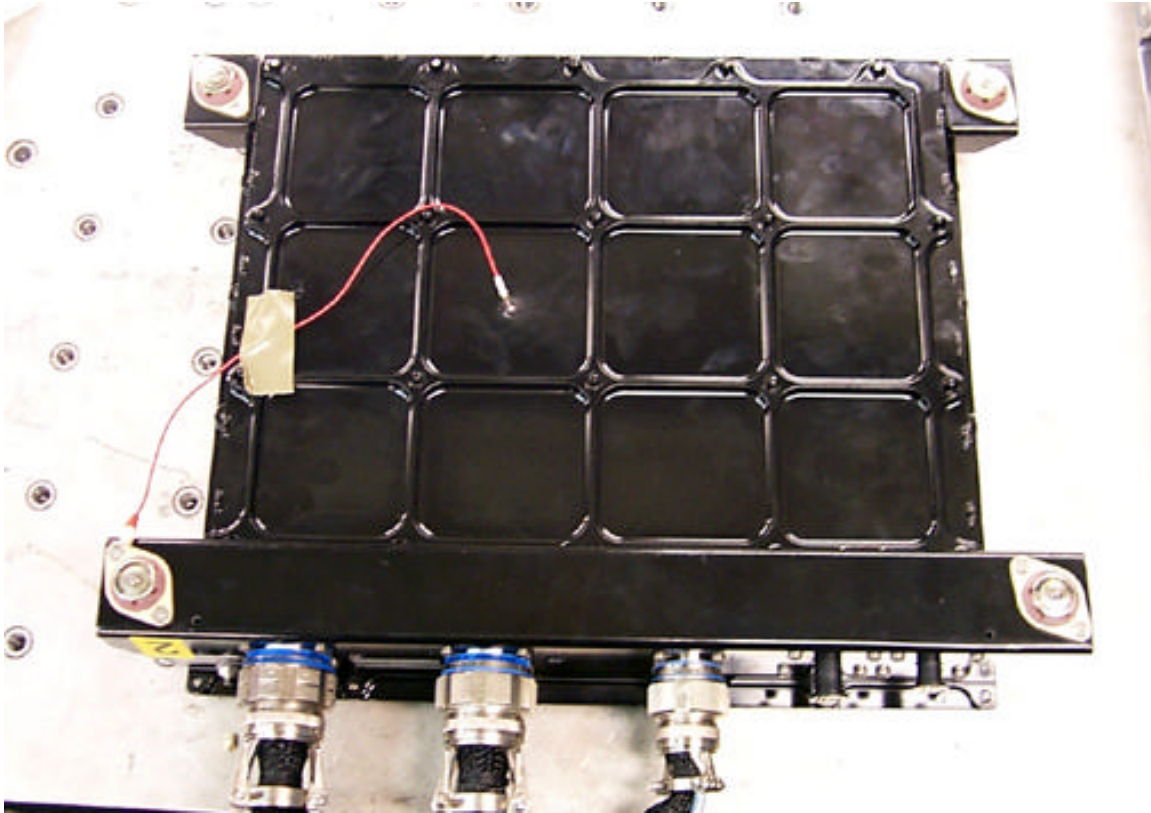


Figure 1: Image of aircraft engine electronic module

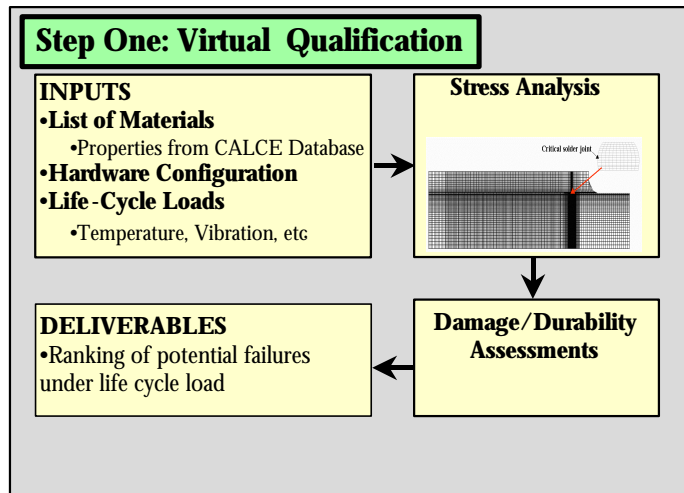
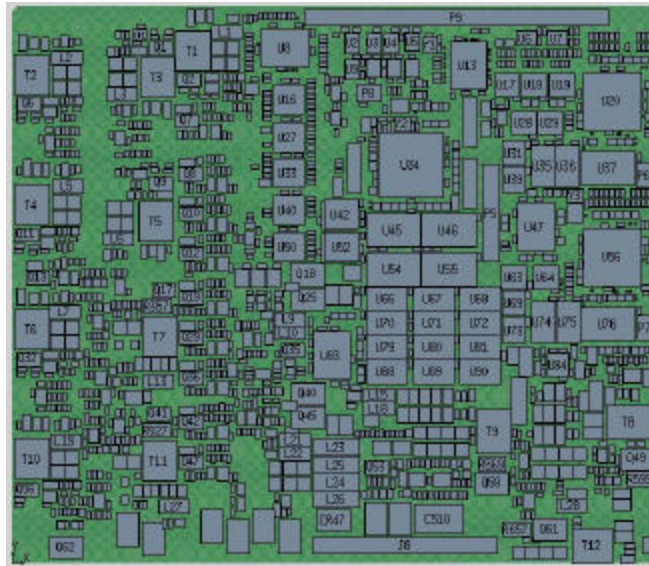
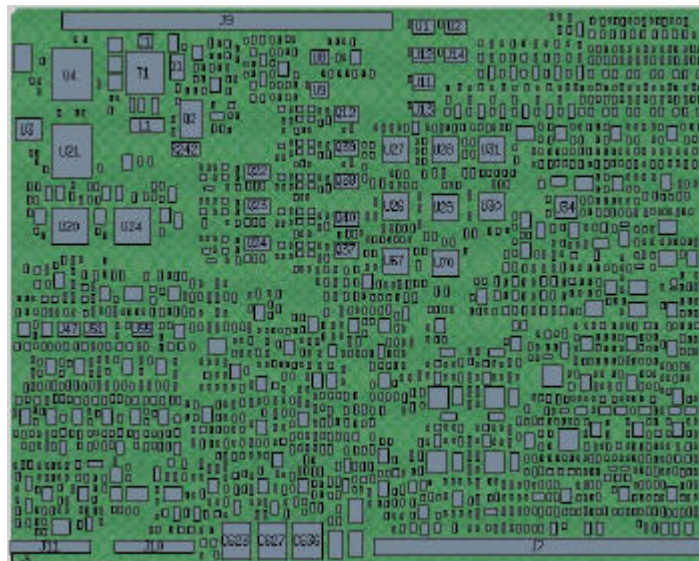


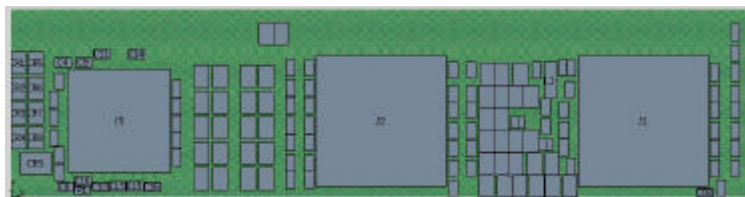
Figure 2: The virtual qualification process developed at CALCE EPSC.



CPU Board



I/O board



EMI board

Figure 3: Circuit Card Assemblies

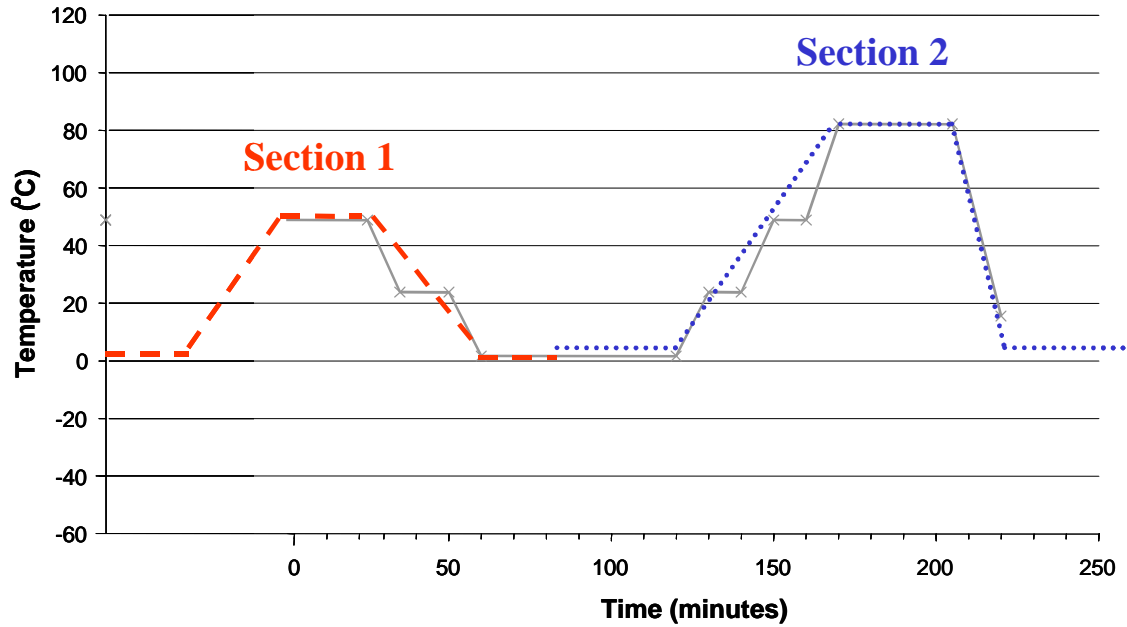


Figure 4: The temperatures shown in Table 3 were taken as inputs to the thermal analysis. Section 1 and section 2 are combined to account for one cycle.

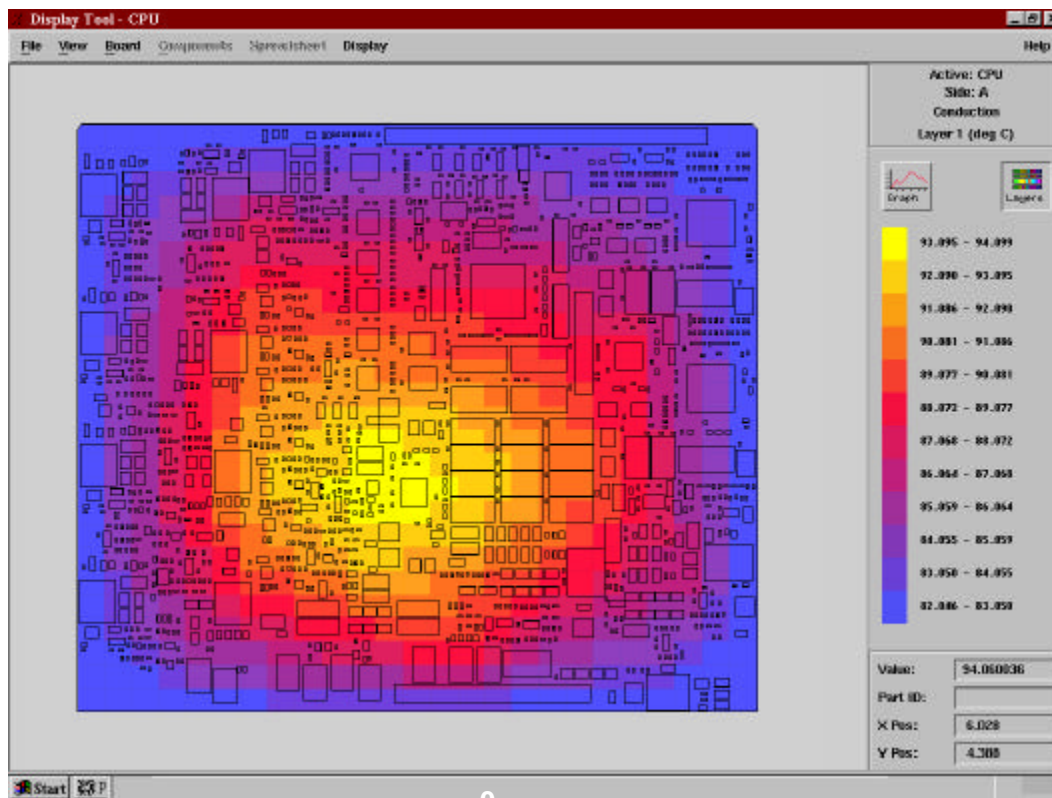


Figure 5: Temperature profile at on-hold power and condition of 82 °C for CPU board.

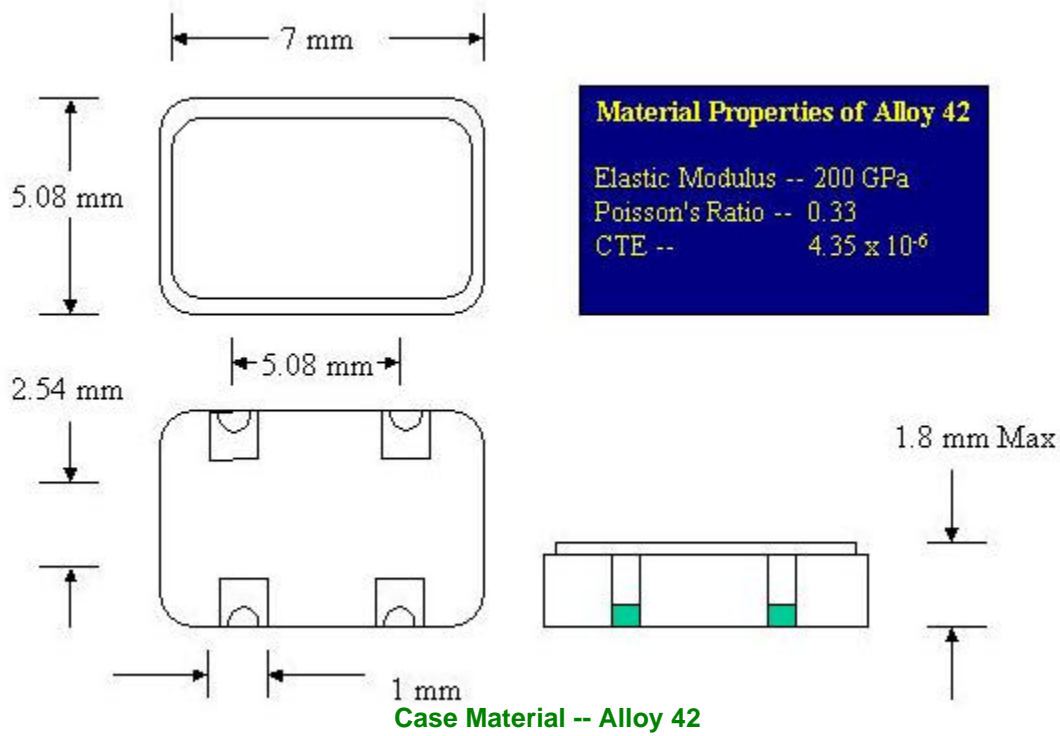


Figure 6: Dimensional specifications and material properties for a Precisions Devices (PDI) 5 x 7 ceramic clock oscillator (dimensions retrieved from <http://www.pdixtal.com/>; material properties retrieved from calcePWA material database).

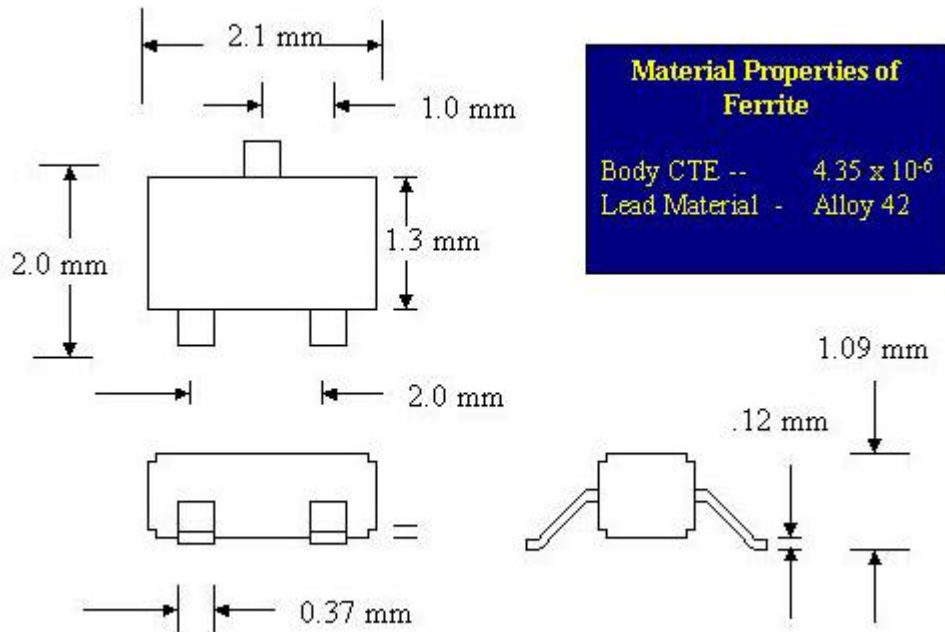


Figure 7: Dimensional specifications for a JEDEC Solid State Product Outline TO-236, issue H, plastic small outline transistor with 3 leads. For each dimension called out, the top number is the minimum length, the middle number is nominal, and bottom number is maximum length. When only two numbers are specified, they relate to the minimum and maximum allowable dimensions.

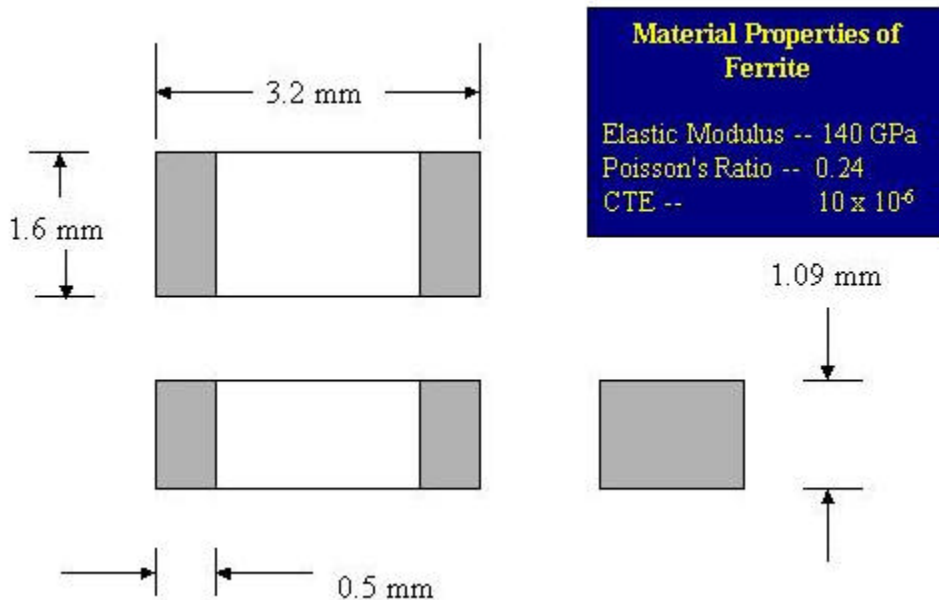


Figure 8: Dimensional specifications and material properties for a Vishay Dale Multilayer Ferrite Bead, part number ILB-1206 (dimensions retrieved from <http://www.vishay.com/>; material properties retrieved from "Soft Ferrites - Properties and Applications," by E.C. Snelling. Published by CRC Press, Cleveland, OH, 1969).

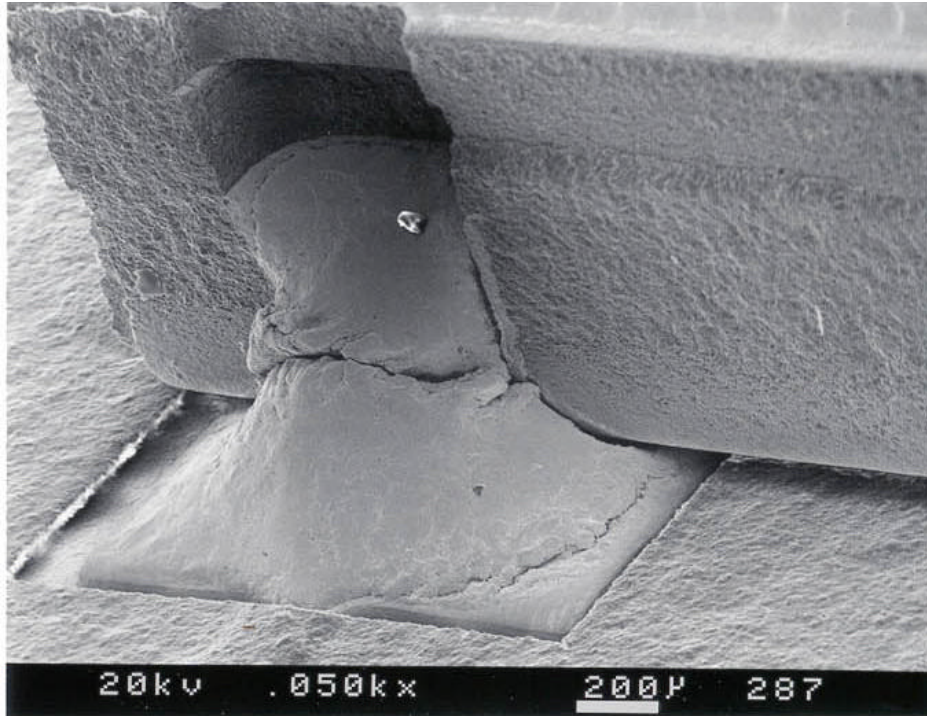


Figure 9 Crack in solder interconnect for the ceramic oscillator

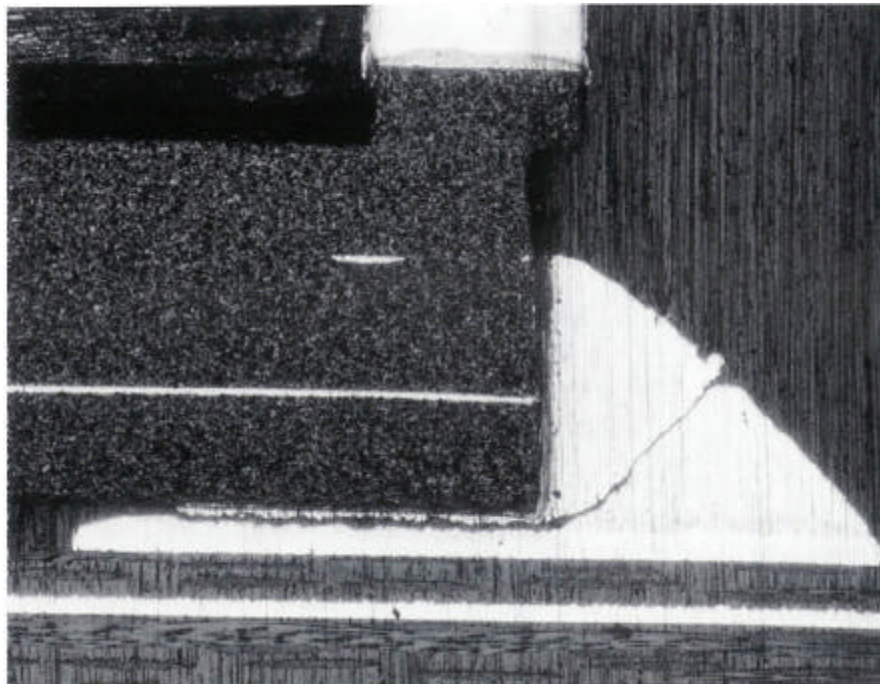


Figure 10 Cross-section of cracked solder joint of the ceramic oscillator