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How to Develop a Qualification Test Plan for RoHS Products

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Summary and Conclusions

The subject matter we address in this tutorial are the significant reliability uncertainties around Lead-Free Solder and how to best address these risks and mitigate them so as not to take a hit in the area of reliability during the lead-free transition.

Introduction

- ◆ Like the rest of the electronics industry, your products will transition to Restriction of Hazardous Substances (RoHS) compliance.
- ◆ At this time, there are significant reliability uncertainties around Lead-Free Solder.
- ◆ Even if your product does not need to be compliant, the materials and processes that make up your product are changing.

As one major consumer product team concluded, doing nothing would double the field failure rate of the electronics.

Introduction

- ◆ During this time of rapid transition, there is a significant new body of knowledge to understand to determine the areas of greatest risk to the reliability of your product.
- ◆ In this presentation, we will highlight a few of these significant risk areas and how to best mitigate these risks during the transition.
- ◆ Even though the deadline of July 1, 2006 came and went, many companies are still struggling with this issue and are either still trying to become compliant, or developed substandard methodologies to meet the deadline, only to find out that they created a ticking time bomb of reliability that is just waiting to go off.
- ◆ We will explore a few of these case studies.

Nomenclature

- ◆ RoHS: Restriction of Hazardous Substances
- ◆ Pb-Free or Lead-Free: Part of the RoHS directive is to restrict the use of lead on electronic systems.

Lead-Free Risks

- ◆ SnPb solder materials have been used in the electronics industry for over 60 years and therefore the processing conditions and their impact on materials and reliability are well understood.
- ◆ Converting to Pb-free materials and processes introduces many risks some of which are better understood than others.
- ◆ The following table describes some of the changes inherent with Pb-free, the failure mechanisms they may induce and the testing/inspection procedures used to screen for them.
- ◆ The test criteria called out in this Pb-free qualification document are intended to screen for many of these potential failure mechanisms.

Lead-Free Risks

	Area of Concern	Impacted Item	Failure Mechanism	Testing Method	Inspection Technique
	Moisture sensitivity	Plastic IC packages, optocouplers, other polymer based components	Popcorn delamination at higher reflow temperatures. Heat damage of IC packages	Moisture sensitivity testing. J-STD-020C	Visual inspection C-SAM
	Heat damage	All passive components, circuit boards	Cracking, dielectric breakdown (capacitors), PCB delamination, warping, or via cracking	Heat resistance MIL-STD 202G #210F Decomposition temp. Time to delamination Package planarity JESD22-B108A	Visual inspection, functional verification
	Poor wetting	All solder joints	Cold joints or weak joints fracture in use environment	Solderability J-STD-002B J-STD-003A	Wetting balance, visual inspection, x-sectioning, lead pull
	Solder fatigue	Solder joints, particularly on high CTE components	Cracked solder joints	Thermal cycle JESD22-A104-B , HALT Vibration	Electrical continuity Visual inspection
	Mechanical shock	Solder joints particularly on higher mass components	Solder joint failure during shipping or dropping	Shock test	Electrical continuity Visual inspection
	Sn whiskers	Sn and SnCu plated components	Shorting	NEMI / JEITA recommended procedures	SEM
	Surface mount process control	Insufficient process window creates poor solder joints	Occasional solder joint failures in use environment	Precondition and assembly JEDEC Standard 22-A113D	X-ray, X-section, Inspection, reliability test
	Rework process	Poor solder joints, damaged components,	Joint failures or cracked vias in use environment	Rework components followed by reliability testing	X-ray, X-section, Inspection, reliability test
	Wave solder process	Incomplete hole fill, fillet lifting, damage to board	Failed through hole, cracked vias, weak joints	Thermal cycle HALT Vibration	Electrical continuity, visual inspection
	Electrochemical migration	Board surface with no-clean paste residue	Shorting between biased traces in a moist environment	Bellcore GR-78-CORE J-STD-004 SIR	Visual and resistance after 35C/85%RH exposure at 50V

Note: For the board in this study, solder fatigue and mechanical shock do not seem to a significant risk and are not recommended for evaluation. This is based on the assumption of adequate packaging during transport and the stable operating temperature (very little if any thermal cycling during use).

The Approach

- ◆ The basic approach is to verify adequate qualification of the individual components has occurred.
- ◆ By requesting and reviewing detailed vendor data most of the risk for your product is either identified or reduced.

For example, if a vendor is unable to produce or has inadequate MSL rating test results, then the risk for popcorning defects is present. With engineering judgment, considering the processing parameters, we can decide to conduct proper MSL evaluation to determine true risk of using the component.

Qualification Requirements – 1st Level

- ◆ This level is reserved for products with lower perceived risk of failure due to introduction of lead-free materials and processing.
- ◆ Products determined to be in this level are relatively simple and constructed exclusively with components such as passives, through-hole and/or coarse pitch (>0.5 mm) surface mount leaded packages.
- ◆ Some exceptions may apply based on specific product application or use environment.
- ◆ To ensure that all materials can survive the elevated temperatures expected with lead free assembly, all components must be evaluated individually prior to assembly.
- ◆ Types of failure mechanisms being screened for include heat damage, moisture induced cracking/delamination, poor solderability, and weak joints.

Materials Used

The following information permits the identification of specific risks and creates a baseline of information on Pb-free assemblies and processes.

- ◆ PCB type
- ◆ PCB Manufacturer
- ◆ PCBA Assembler (list if sub contracted, In House, sub supplier)
- ◆ PCB glass transition temperature
- ◆ PCB decomposition temperature
- ◆ PCB manufacturer certified heat resistance
- ◆ PCB Thickness
- ◆ PCB # Layers
- ◆ 1 or 2 side populated
- ◆ Pad finish type (i.e.ImAg, OSP, etc.)
- ◆ List the surface mount lead-free alloy (i.e. Sn-3.5Ag-0.9Cu)
- ◆ Solder paste manufacturer and product # (list all suppliers)
- ◆ SIR test results from solder paste supplier.
- ◆ Flux type (no clean, water soluble, etc.)
- ◆ Wave solder Pb-free alloy
- ◆ Hand Solder / Rework (Wire) Pb free alloy

Process Information Questions

The following questions are meant to establish a baseline for these items relative to initial lead free process management.

1. Is the product built with a single or dual reflow process?
2. List the peak temperature distribution across the PCBA/Panel.
3. Time within 5C of peak.
4. List the time above liquidus temperature.
5. Provide time / temperature reflow profile. Provide location on PCB / Panel for thermocouple probes (attach picture / diagram) and temperatures for those locations during the reflow process.
6. List the minimum peak solder joint temp measured on board (under highest thermal mass component).

Process Information Questions, cont.

7. Wave solder process flow and maximum solder pot temperature / duration (if applicable).
8. Soldering iron temperature (Temp +/-) for rework and hand solder. Maximum allowable hand-solder duration.
9. Provide general overview of part storage and factory floor management for components according to MSL level (for moisture sensitive components). Detailed part management is subject to on site audit.
10. Is nitrogen used in reflow?
11. Procedures for rework to include inspection criteria and soldering iron temperature.
12. Inspection criteria used for lead-free solder joints. This will include criteria for sub contracted assemblies.
13. Provide general overview regarding isolation and tracking of leaded components / materials from Pb-free components / materials. Detailed part management is subject to on site audit.

Component Information – Heat Resistance

- ◆ All components used to build a Pb-free product must be rated for temperatures at least 10°C higher than peak assembly process temperature.
- ◆ Heat resistance testing should be performed following MIL-STD 202G #210F with 90-120sec above Pb-free solder liquidus with ≥ 10 seconds at or above peak (+10C).
- ◆ Deviation for time above liquidus may be allowed based on process TAL (must be a minimum of 20% greater than process TAL).
- ◆ MIL-STD-202G #210F should be followed for wave solder and soldering iron heat resistance.
- ◆ Components that are hand soldered, reworked, or touched up should be rated for a soldering iron temperature at least 10°C higher than process conditions.
- ◆ Recommended min sample size is 10/lot for 3 lots.

Component Information - Moisture Sensitivity

- ◆ Determining the moisture level for surface mount components should be done following J-STD-020C for Pb-free or JEITA ED 4701 (Test Method 301A for Pb-Free).
- ◆ Components qualified to J-STD-020B may be acceptable if temperature rating is deemed sufficient.
- ◆ Sample sizes are defined in the specifications as well as inspection and pass/fail criteria.
- ◆ A minimum of 3 reflows is required. A minimum of 60 seconds above liquidus or duration 20% higher than actual reflow process time above liquidus (whichever is longer) is required.
- ◆ SMT type components that are wave soldered will follow procedures detailed in JEITA ED 4701 (Test Method 301A for Pb-Free).
- ◆ A minimum of Level 3 (JEDEC) or Level E (JEITA) is required for all components. Level 4 components (JEDEC) or Level F/G (JEITA) may be approved if factory management is considered acceptable. Components that do meet minimum of Level 4 or above are not acceptable.

Lead Plating

- ◆ The Pb-free lead plating material is important in evaluating the risk for tin whiskers. Table 1 outlines requirements for Tin Whisker testing for plating materials determined to be a risk.
- ◆ Finer pitch components plated with Sn based lead finish are most susceptible to shorting due to whisker growth.
- ◆ A 1.3 μm nickel underplate is preferred for Sn finishes as this prevents copper diffusion into the Sn which contributes to compressive stress in the Sn layer (the primary driving force for Sn whiskers for Cu base material).
- ◆ SnCu plating is known to be a high risk for Sn whisker growth and should be avoided when possible (bright Sn is the highest risk and not acceptable).
- ◆ Lead plating situations as outlined in table 1 will require testing according to NEMI/JEITA recommended procedures: 1) Storing at 60°C/95%RH for 1000 hours followed by SEM analysis; 2) Thermal cycling 1000 times from -55°C/85°C followed by SEM analysis; and 3) Store at room atmosphere conditions for 1000 hours followed by SEM analysis.
- ◆ Criteria: Maximum allowable whisker length is 50 microns (separate criteria for FFC/FPC/Connector Mating).

Tin Whisker Test Matrix

All Components <i>EXCEPT</i> : FFC/FPC/Connector Mating End			
Finish	Lead Pitch > 0.5mm	Lead Pitch ? 0.5mm	Comments
Sn/Ni (>1.3 µm Ni)	Acceptable	Acceptable	
SnBi (1-4%Bi)	Acceptable	Acceptable	
SnAgCu & SnAg	Acceptable	Acceptable	
Sn (matte)	Acceptable	Testing Required	Reflow or annealing may help reduce Sn whisker density (conflicting industry data).
SnCu	Acceptable	Testing Required	For high reliability applications, testing may be required for >0.5mm pitch
Sn (bright)	Unacceptable	Unacceptable	Semi-bright Sn should be treated similar to SnCu
FFC/FPC/Connector Mating End ONLY			
	Min Conductor Spacing >270um	Min Conductor Spacing ?270um	Comments
Sn/Ni (>1.3 µm Ni)	Acceptable	Testing Required	Best tin based solution
SnBi (1-4%Bi)	Acceptable	Testing Required	Nickel Underplate preferred
SnAgCu & SnAg	Acceptable	Testing Required	Nickel Underplate preferred
Sn (matte)	Acceptable	Testing Required	Nickel Underplate preferred
SnCu	Unacceptable ^{Note g}	Unacceptable	Nickel underplate required ^{note g}
Sn (bright)	Unacceptable	Unacceptable	Semi-bright Sn will not be acceptable
Whisker length Criteria			
Criteria	Min Conductor Spacing ?140um		Max Whisker Length 20um
	Min Conductor Spacing >140um		Max Whisker Length 50um
NOTES:			
(a) Whisker testing includes both mating and PCB mounting end for connector			
(b) Conductor spacing is the minimum tolerance, not nominal value. Supplier specification must be provided that shows key dimensions including conductor spacing (nominal +/- tolerance).			
(c) Testing will be performed mated to the connector used in application. Both FPC/FFC and connector (if applicable) will be evaluated for tin whisker. A matrix shall be provided showing connector / FFC (FPC) combination tested.			
(d) Gold / Nickel Underplate is preferred for high reliability applications			
(e) Where possible, minimum spacing should be increased to mitigate whisker risk.			
(f) High Reliability applications may require testing for spacing above 270um for any Sn based plating type.			
(g) Will be allowed on exception basis only. Exception will be based on product application and risk. In addition these factors, minimum conductor spacing must be >270um.			

Sample Distribution

1. Full sample size must be provided from each manufacturing location and solder supplier used. This includes sub supplier qualification.
2. Full or partial sample for each bare PCB supplier will be required. Agreement regarding sample size and distribution will be made prior to qualification start.
3. If different manufacturing lines are used (at time of evaluation), then sampling must be from each line. Sampling rate will be determined prior to evaluation.
4. Distribution of key components from each manufacturer used. Key component(s) and build mix will be determined prior to evaluation.
5. A control group will be required for comparison purposes. This control group may consist of the same product assembled with SnPb solder or previous generation of SnPb product of same complexity.

Qualification Requirements – 2nd Level

- ◆ This level is reserved for products with moderate perceived risk of failure due to introduction of lead-free materials and processing.
- ◆ Products determined to be in this level are more complex and will likely have one or more of the following surface mounted components: plastic leadless packages, fine pitch QFPs (≤ 0.5 mm lead pitch), plastic ball grid arrays (≤ 27 mm body size) or chip scale packages with ball pitches ≥ 1 mm (ball pitch of less than 1 mm is generally require solder fatigue evaluation).
- ◆ In addition to the Level 1 requirements of proving process capability and functionality after assembly, this level of qualification requires testing for mechanical and thermally induced fatigue failure.
- ◆ This Level requires that the product also pass qualification Level 1.

Precondition / Assembly

- ◆ Assembly of product/test boards should be done at optimum process conditions (including wave or hand solder when applicable) followed by reworking of predetermined components on some boards.
- ◆ In some cases exploring additional assembly conditions may be required.
- ◆ For example, preconditioning components and boards prior to assembly is an effective way to prove that worst-case assembly conditions still produce reliable products (i.e. a sufficiently wide process window exists).
- ◆ A test plan specific to each product will be developed and sample sizes for each assembly condition agreed to prior to testing.

Vibration and Shock

- ◆ Concurrent testing for both vibration and shock shall be performed when determined to be necessary.
- ◆ Testing details will be prescribed according to the product type and expected use environment.
- ◆ Typical tests may include non-operational vibration followed by shipping shock (pack drop).
- ◆ In some instances mechanical shock and vibration testing may be preceded by thermal shock.
- ◆ Operational testing in a system level may also be performed.
- ◆ Sample sizes and pass/fail criteria will be determined during creation of the detailed test plan (sample size will typically be 5 or greater for each test type).

Thermal Cycling

- ◆ This testing is required primarily for level 2 components.
- ◆ Follow procedures described in JESD22-A104-B, condition J.
- ◆ The specific requirements described on the following page fit many product types, however, alternative thermal cycling test protocols and evaluation plans are potentially acceptable.

Thermal Cycling

1. Sample size: ≥ 20 . A separate group of an additional 10 reworked components will also undergo thermal cycle (if applicable).
2. The complete functional PCBA must be thermal cycle tested.
3. Cycle 1000 times from 0 to 100°C with a ramp rate of 10-20°C/min and a 10 min dwell time (measure temperature on the largest thermal mass component on the PCB).
4. Visually inspect joints and confirm functionality of complete PCBAs after 500 and 1000 cycles.
5. In cases where proving electrical functionality is not feasible, solder joints on BGA components can be evaluated after 1000 cycles using dye and pry.
6. Criteria: Zero solder joint failures accepted unless product life requirements allow for a failure.
 - A failure is defined by a functional test error or a joint that is cracked 50% through (as revealed by dye and pry).
 - Visual inspection and functional test specifics to be agreed upon prior to commencement of test. Additional evaluation may include cross sectioning, lead pull, and component shear. Issues found during additional evaluation, including visual inspection, will be reviewed prior to determination of product acceptability.
7. Test and failure analysis results will be provided. Solder joint failures will be assessed and corrective actions taken.

Highly Accelerated Life Testing (HALT)

- ◆ HALT is primarily a board level test that must be performed within a multi-stress (temperature and vibration) chamber. During the HALT process, thermal cycling and vibration are to be simultaneously applied.
- ◆ The temperature responses on critical components must be monitored with thermocouples to insure adequacy of the dwell periods selected
- ◆ The temperature range (between highest and lowest dwell temperatures) is to be a minimum of 80-degrees C unless otherwise technology limited.
- ◆ The product is to be functionally operational and monitored during "HALT" stressing.
- ◆ Sample size preferred is 2 units.
- ◆ Where a previously established baseline is available, the product must meet or exceed prior limits. Where no prior baseline is established, comparative results to leaded control sample must be met.
- ◆ Supplier conducted HALT must include reporting test results according to agreed upon format, including full failure analysis and corrective action on anomalies observed
- ◆ Criteria: Component delamination must meet criteria according to J-STD-020C. Zero functional failures, or fully cracked solder joints.

CONCLUSION

- ◆ SnPb solder materials have been used in the electronics industry for over 60 years and therefore the processing conditions and their impact on materials and reliability are well understood.
- ◆ Converting to Pb-free materials and processes introduces many risks some of which are better understood than others.
- ◆ Following the guidelines in this presentation can help mitigate these risks, resulting in reliability as good or better than SnPb.

Case Study 2: Military Application

- ◆ Understand your risk points with Pb-free
- ◆ Understand your primary drivers for product degradation
- ◆ Do not default to industry or military specifications
 - Review and modify as necessary