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2019 DESIGN FOR RELIABILITY CONFERENCE

Accelerated Radiation Susceptibility Analysis and Prediction (RadSAP) Tool

Your Partner Throughout the Product Life Cycle

March 25, 2019 | Greg Caswell & Ashok Alagappan

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Introduction

- Evaluating the effects of radiation on an integrated circuit design is a complex task, both in terms of the range of inputs and the number of computations necessary to consider the entire device. Most approaches to date require gate level analysis and do not scale easily to device level calculations, leading to methods that are not practical under most program timelines and budgets. The increasing complexity of devices, reduced budgets and accelerated program timelines require a new approach to predicting radiation of integrated circuit (IC) designs.

- Existing sensitivity and mitigation models can be adapted to more advanced nodes and IC designs using a physics-of-failure approach. IC designs can then be assessed without a costly and time-consuming build and test cycle, providing the opportunity for trade-off analyses and informed decision making that includes a quantitative radiation risk assessment during specification and design.

Approach

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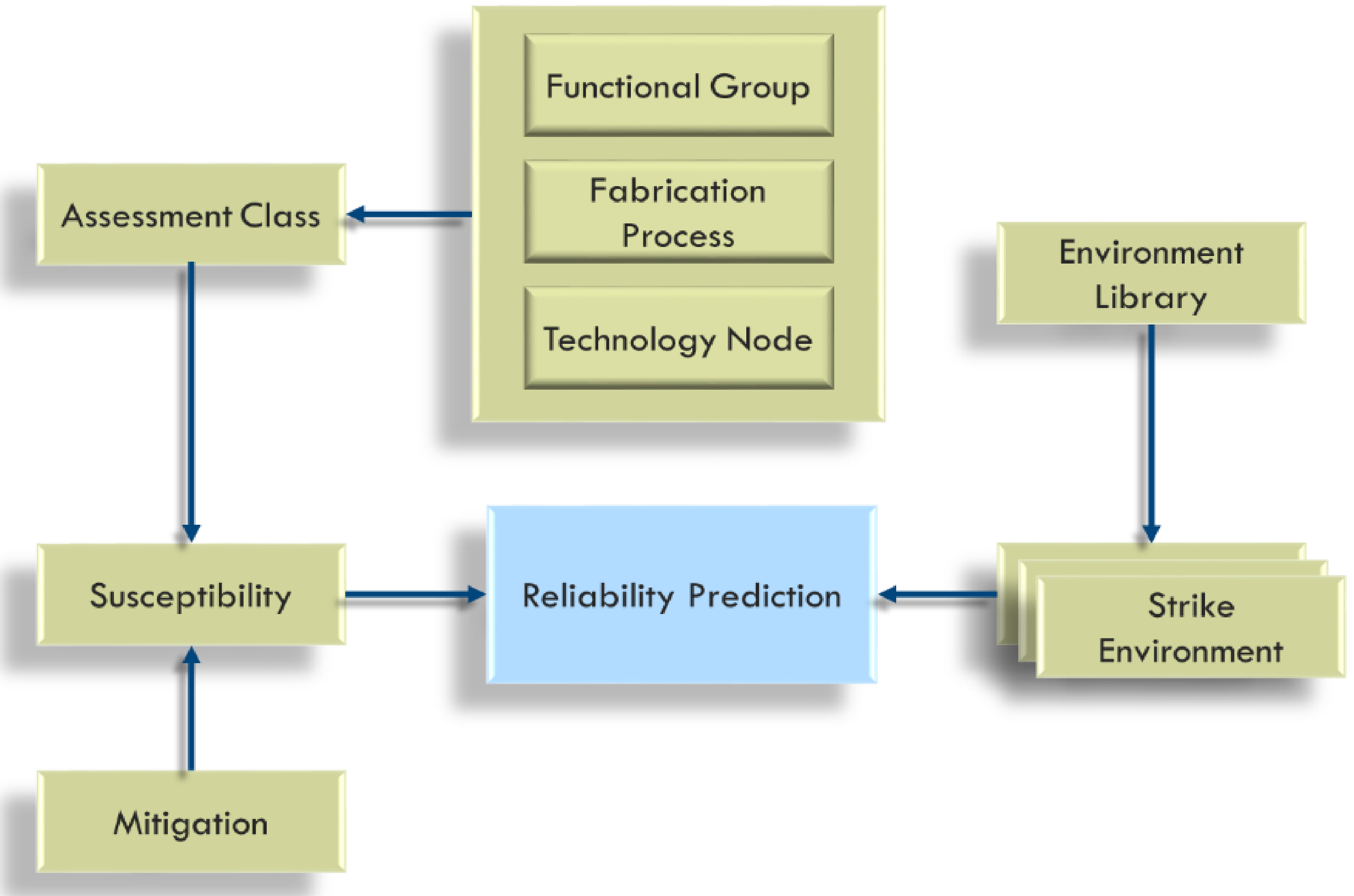
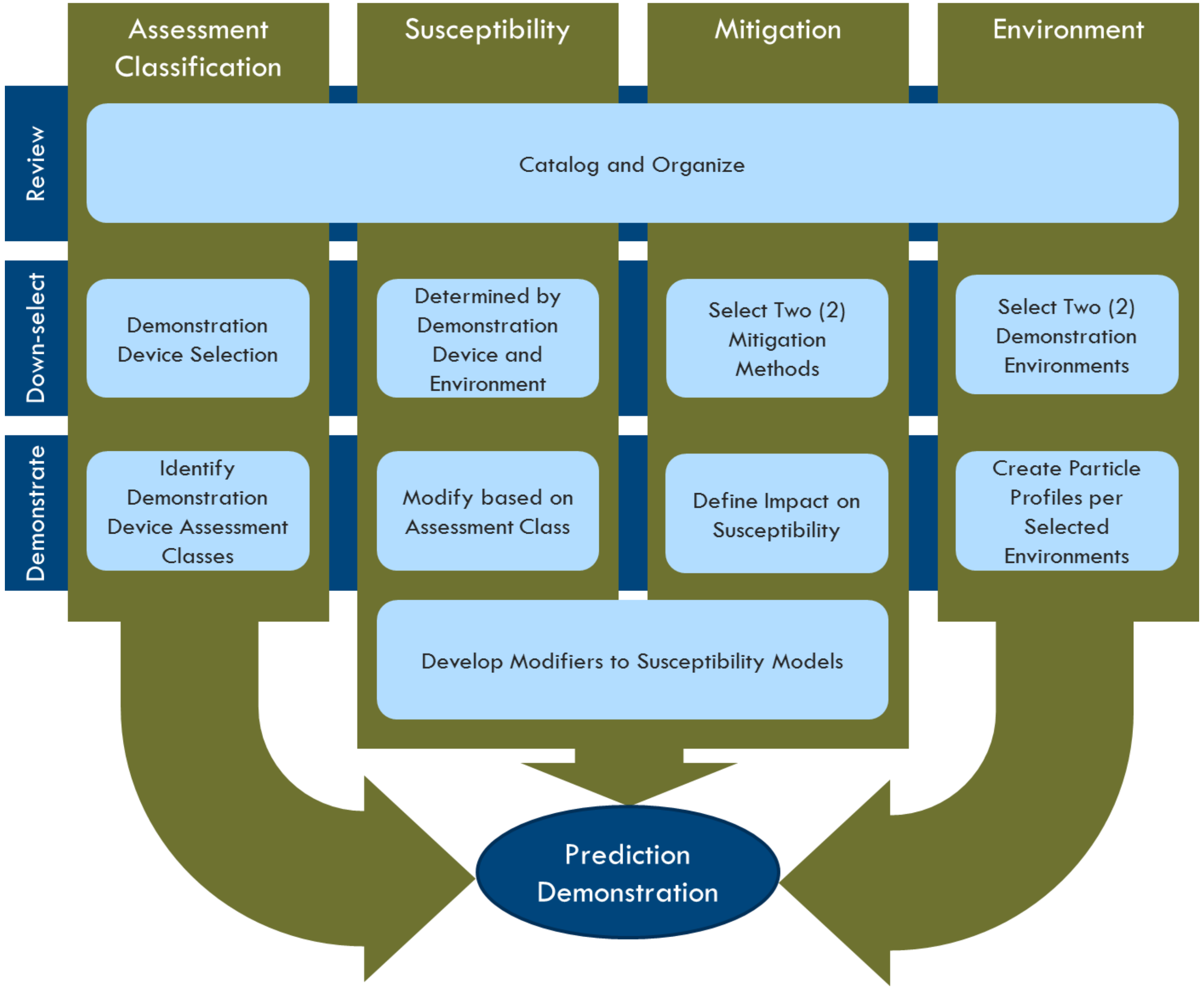
- Determine Functional Groups
- Define Fabrication and Packaging Processes
- Identify Technology Nodes
- Create Environment and Strike Libraries
- Identify Mitigation Techniques
- Perform Reliability Prediction



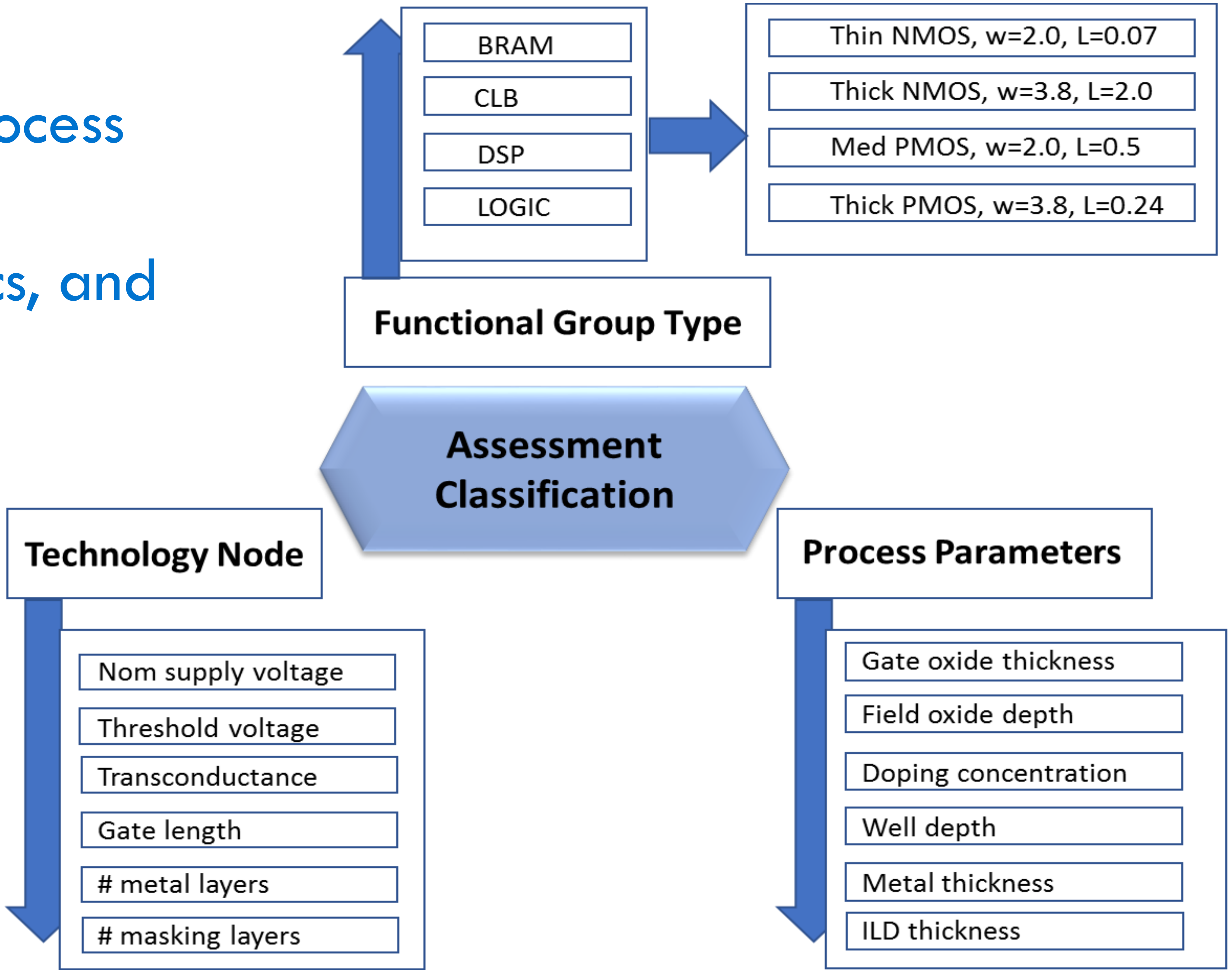
Actions

- Identified a Xilinx VirTex 5 processor as the baseline device
- Analyzed data on radiation susceptibility
- Identified technology nodes and functional blocks
- Selected 2 mitigation techniques
- Selected 2 environments – LEO and GEO



Classification Strategy for Xilinx part

Assembled into the tool the process parameters for the device, the technology node characteristics, and the baseline structures for the functional groups.

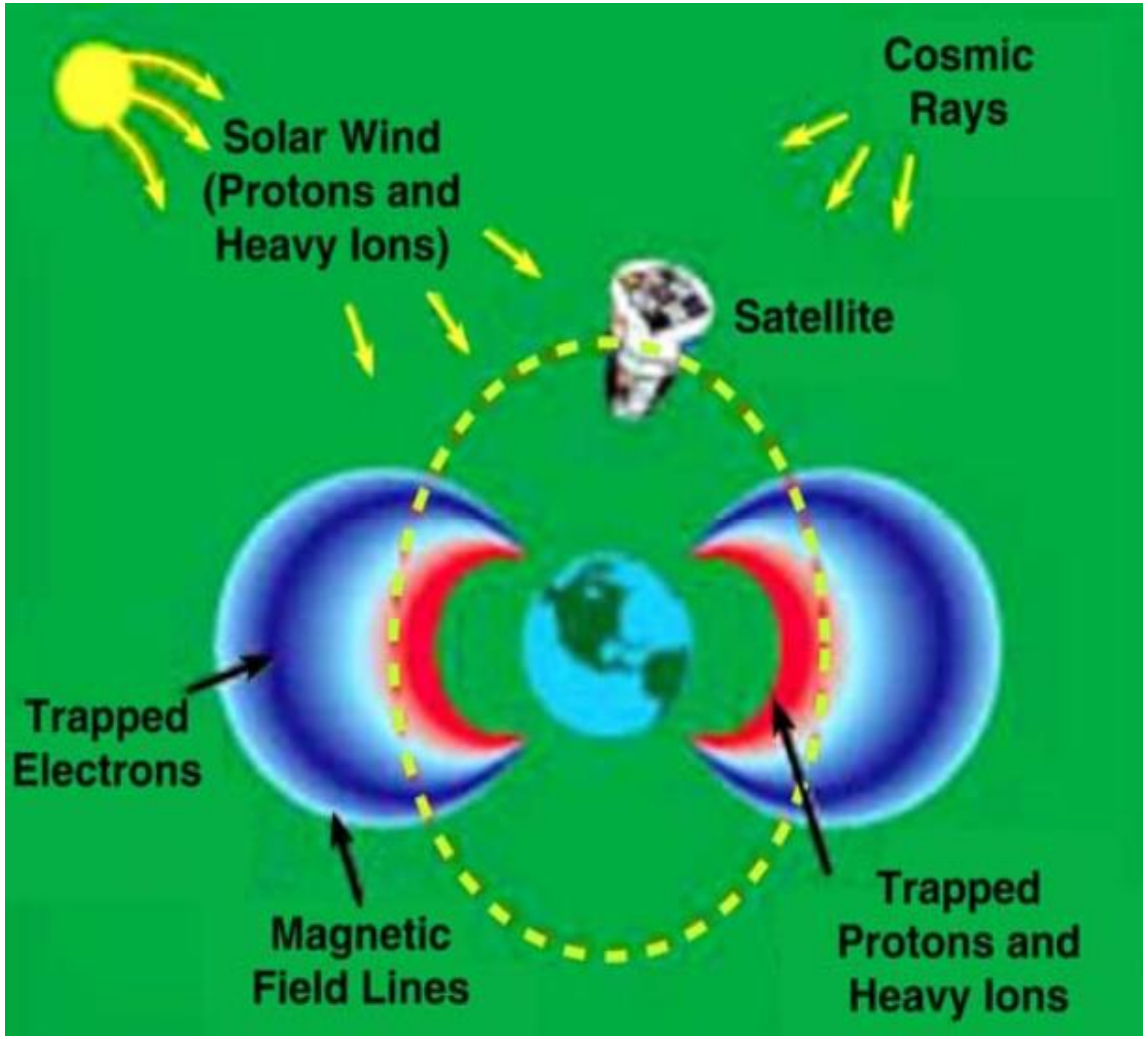


Strike Environments

For simplicity, the Inner Belt LEO and GEO radiation environments were selected for analysis, allowing the trapped proton and cosmic radiation strike models to be considered independently

The basic unit of the radiation environment risk assessed was the particle strike model. For each, critical metrics were necessary for evaluation and were characterized to include:

- Type (electrons, protons, heavy ions, etc.)
- Energy (Linear Energy Transfer (LET), MeV·cm^2/mg)
- Fluence (ions/cm^2)



Approach for Demonstration

Selected Environments

Environment	Particle	Charge	Energy Range	Effects
Inner Trapped Radiation Belt	Proton	+	1 KeV to 300 MeV	TID, SEE (sensitive devices)
Galactic Cosmic Rays	Heavy Ions	+/-	> 10, 000 MeV	SEE

Identified Shielding Materials

Particle	Good shielding material
Charged particle (p, e^-, heavy nuclei)	High Z material (such as aluminum)
X-ray / Gamma-ray	Heavy elements
Neutron	Boron
Alpha	Most materials
Bremsstrahlung	Low Z material (prevents Bremsstrahlung)

Model Flow Chart and Tool

1 Determine type of Microcircuit- *FPGA, memory, logic, analog*

2 Determine assessment classifier – *Device Parameters (gate length, width # metal, gate/field oxide thickness)*

3 Determine strike environment & Particle characteristics – *LEO, MEO, GEO Particle type, energy, flux, etc*

4 Determine radiation effects on the Component – *TID, SEE (SEU, SEL, SET, SEB, SEGR SEFI)*

5 Determine device susceptibility to Ionizing Particles using models – *Shift in Threshold voltage, leakage, subthreshold swing*

6 Determine effect of parameter degradation to overall circuit (parametric, timing, functionality) *- Predict reliability (Failure rate due to TID + SEE)*

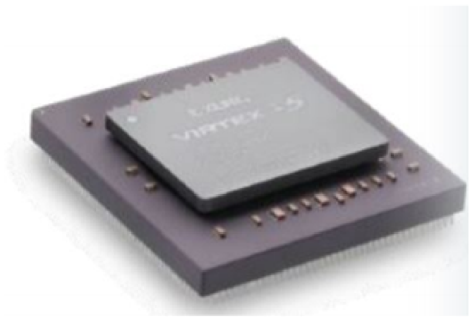
Acceptable

Yes → No risk in using the Component for the application

No → 7 Determine mitigation techniques- *Design (layout, redundancy, etc), Process (SOI, edgeless gate, epi, etc) System (shielding, etc)* → Repeat steps 5 and 6

RSAP Tool

Device	Virtex-2 (150nm	
Expected Lifetime	15	years
TID Mission Tolerance	1	Mrad
SEE Mission Tolerance	1.00E+00	upsets/device/day
Space Environment	LEO	



Effect	Include?	Mitigation Used?	Failure Rate Contribution (upsets/day/device)	
SEE	YES	YES	5.700000E-01	Within Tolerance
TID	YES	YES	8.196067E-08	
IC Wearout	YES	N/A	1.840683E-09	

Device Failure Rate	5.700001E-01	failures/device/day
	2.375000E-02	failures/hour/device

Phase II Approach

- Optimization of the analytical assessment classifier built in Phase I to increase and optimize processing throughput
- Development of abstraction modeling coupons to provide the necessary parameterization
- Development of the technology abstraction library and strike model library
- Optimization of the strike model library developed in Phase I by leveraging the feedback data provided with testing the abstraction modeling coupons.
- Development of a susceptibility classifier and integration of a radiation susceptibility analysis and predictor accelerator into a prototype level and fully integrated tool
- The radiation susceptibility results and a full chip design will be compared to the results obtained by the susceptibility analysis and prediction platform.
- Industry and government partners for Phase III must be identified along with demonstration of their support