DfR Solutions
RELIABILITY DESIGNED & DELIVERED

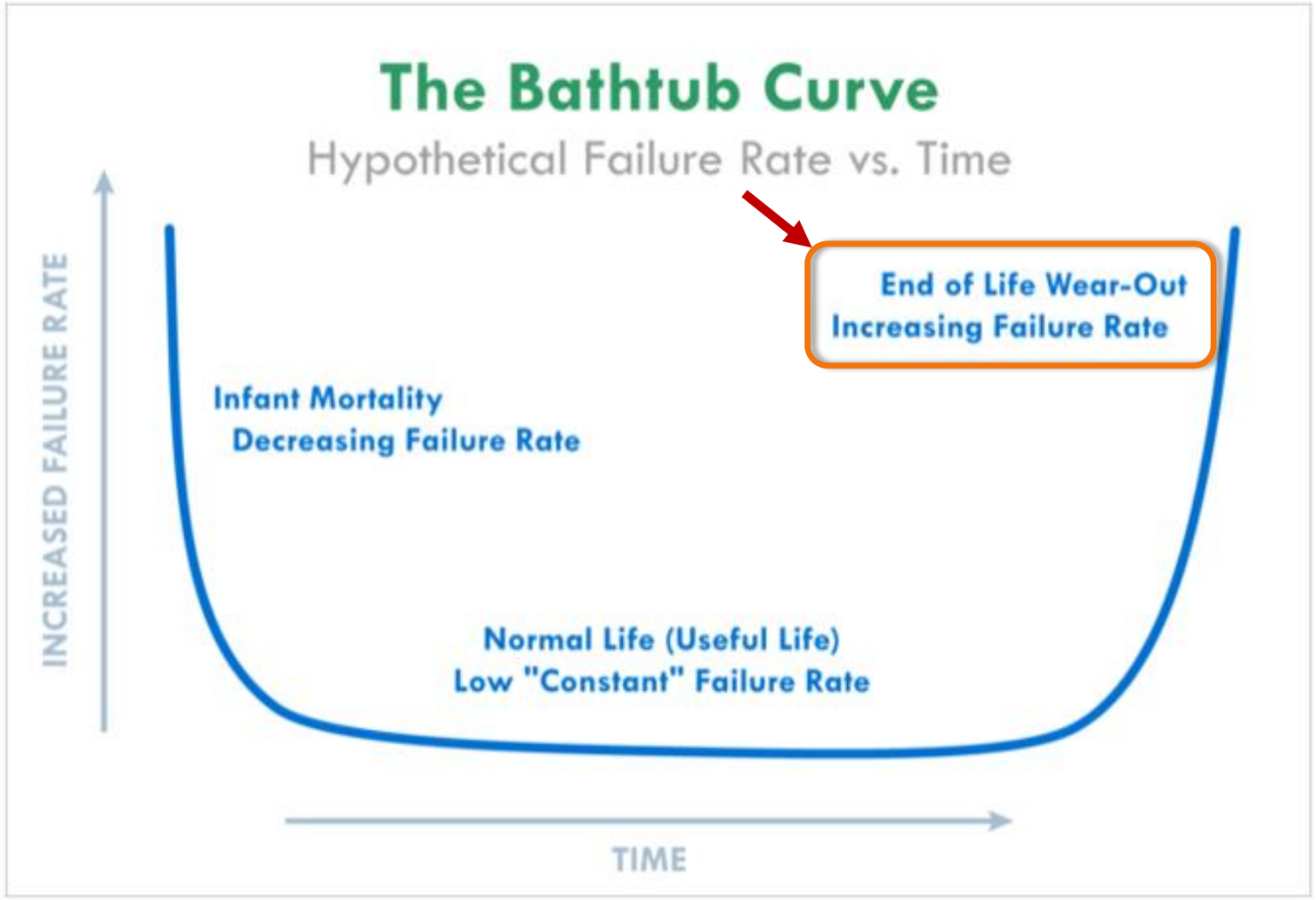
sherlock
AUTOMATED DESIGN ANALYSIS™

2019 DESIGN FOR RELIABILITY CONFERENCE

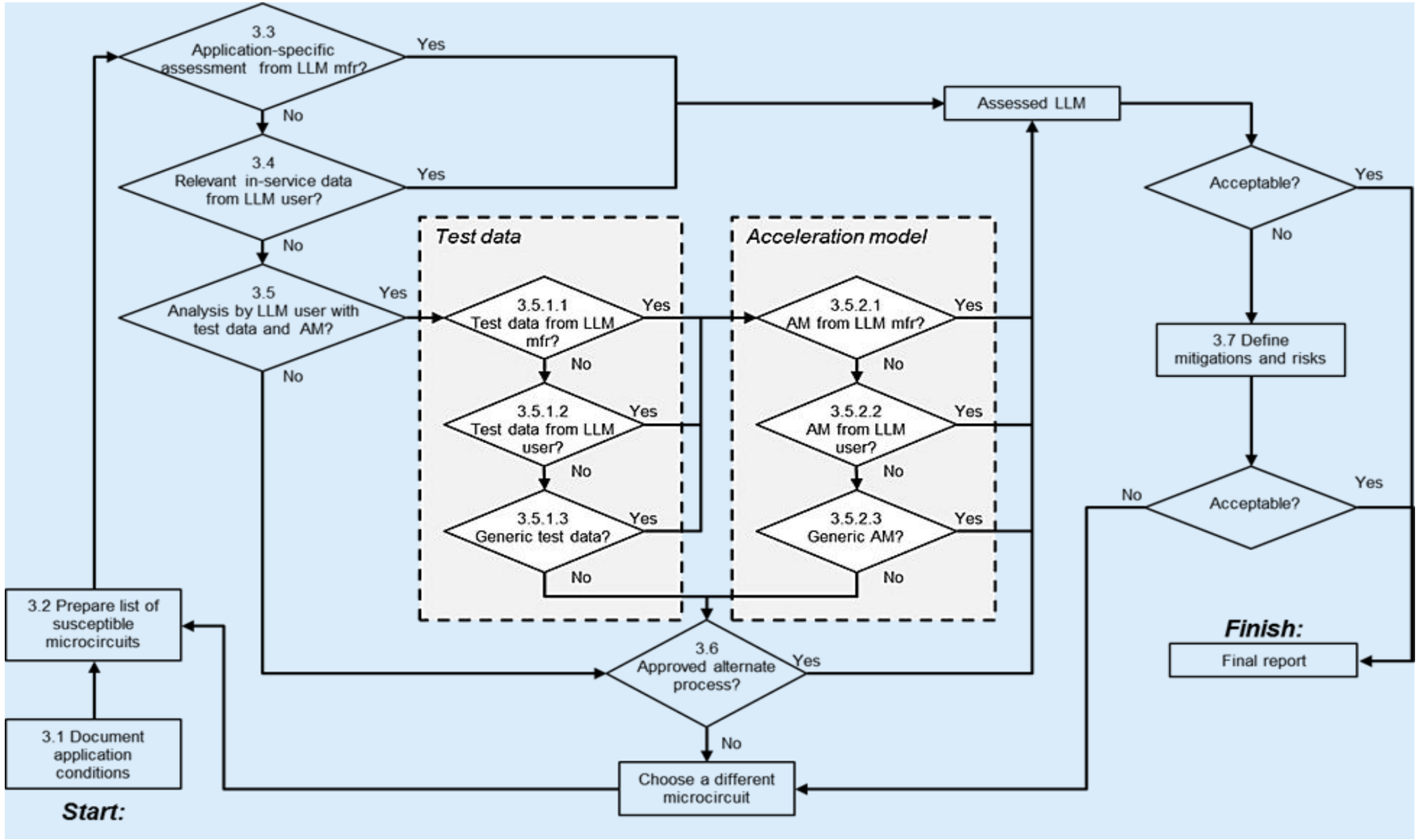
Predicting the Failure Rate of Next Generation Integrated Circuits using Reliability Physics

March 25, 2019 | Ashok Alagappan

BATHTUB CURVE



APPROACH - SAE ARP 6338



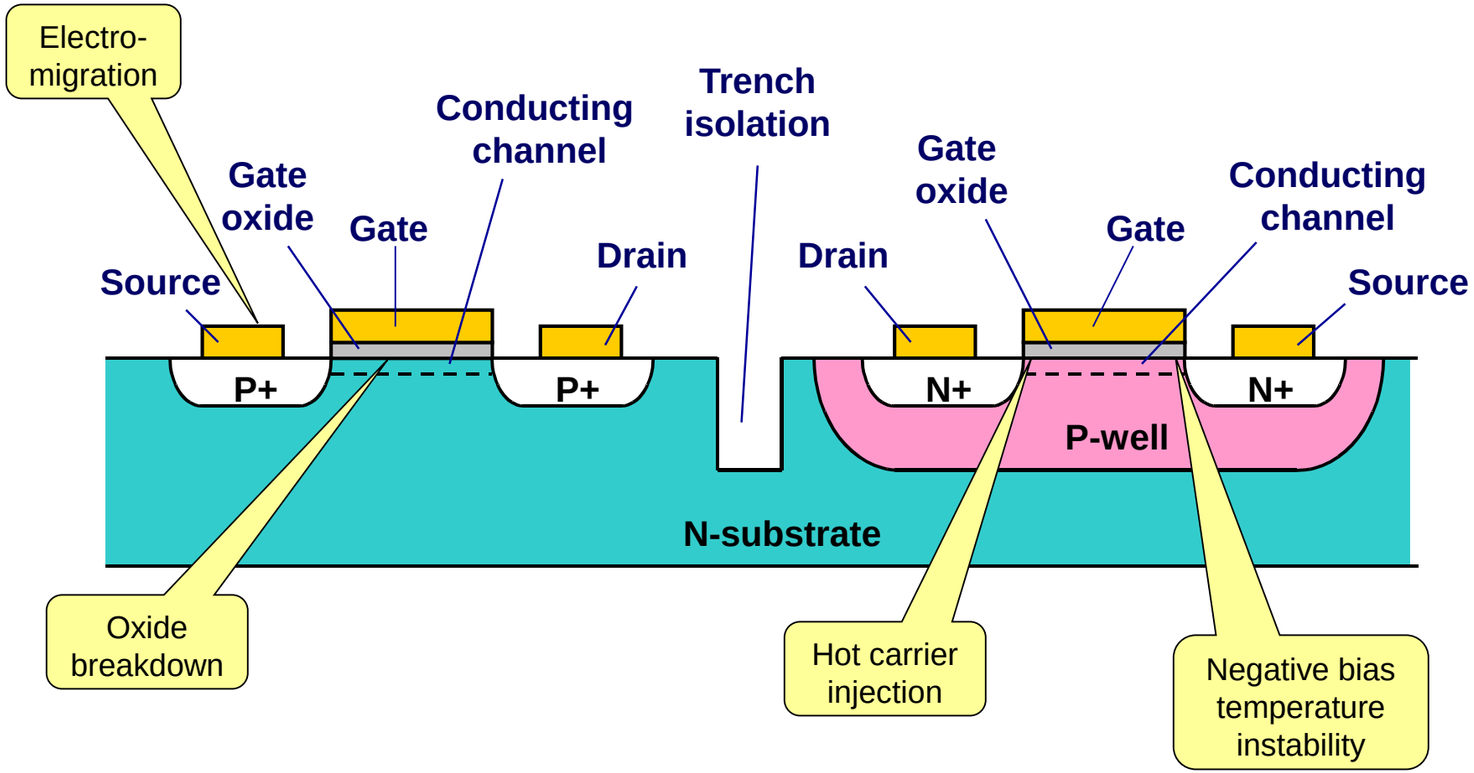
SHERLOCK: FIVE APPROACHES TO PREDICTION

		Data from Supplier	
		Temperature Specific Prediction	General Test Results
Acceleration Factor	Provided	2	3
	Calculated	4	5

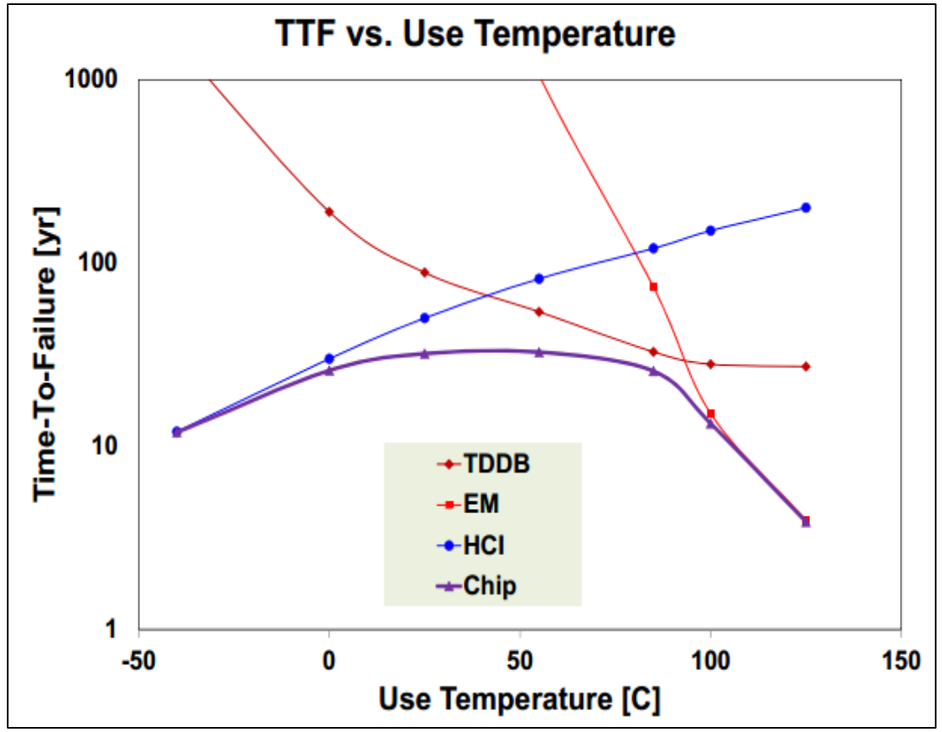
Option 1: The manufacturer provides a prediction based on the life cycle or the user has actual field data at the same or similar life cycle

FAILURE MECHANISMS and BEHAVIOR

- INTRINSIC FAILURE MECHANIMS



- FAILURE BEHAVIOR



TYPES OF FAILURE MECHANISMS

WEAROUT

- Stress induced break down of materials driven by time, voltage, current and temperature
- Random and sudden failure of active or passive components and structures
  - Time Dependent Dielectric Breakdown (TDDB)
    - Gate dielectric failure caused by high electric field across gate
    - Results in increased leakage across gate oxide eventually leading to breakdown
  - Electromigration (EM)
    - metal interconnect failure caused by high current density and/or high temperature
    - Results in void (open) or hillock (short) in metal lines

AGING

- Gradual parametric shift of all devices as a function of time, voltage, current and temperature
- Well behaved time dependency
  - Bias Instability (BTI)
    - PMOS FET's with negative bias experience this degradation mechanism.
    - Results in threshold voltage increase, drive current reduction
  - Hot Carrier Injection (HCI)
    - carriers gain sufficient energy to be injected into the gate oxide causing damage
    - Results in shifts in threshold voltage shifts, leakage current.

TRACEABILITY OF MODEL PARAMETERS

- Device parameters such as gate oxide thickness, gate length and width, nominal supply voltage, and drive current are obtained from ITRS roadmap

- Activation energy for different failure mechanisms are obtained from JEDEC JEP122F Failure Mechanisms and Models for Semiconductor Devices

- Voltage exponent, frequency exponent (gamma), and Weibull betas for each failure mechanism are obtained from published literature and industry sources

SHERLOCK RESULTS

- Lifetime prediction based on four intrinsic failure mechanisms

The following chart shows the Semiconductor Wearout Life Prediction curve for U3(NASA).