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2019
DESIGN FOR RELIABILITY
CONFERENCE

Risks of Wide Band Gap (WBG) Semiconductors in Power Supply Applications

Your Partner Throughout
the Product Life Cycle

March 25, 2019 | Dr. Craig Hillman

9000 Virginia Manor Rd Ste 290, Beltsville MD 20705 | 301-474-0607 | www.dfrsolutions.com

WHY WIDE-BAND GAP (WBG) SEMICONDUCTORS?

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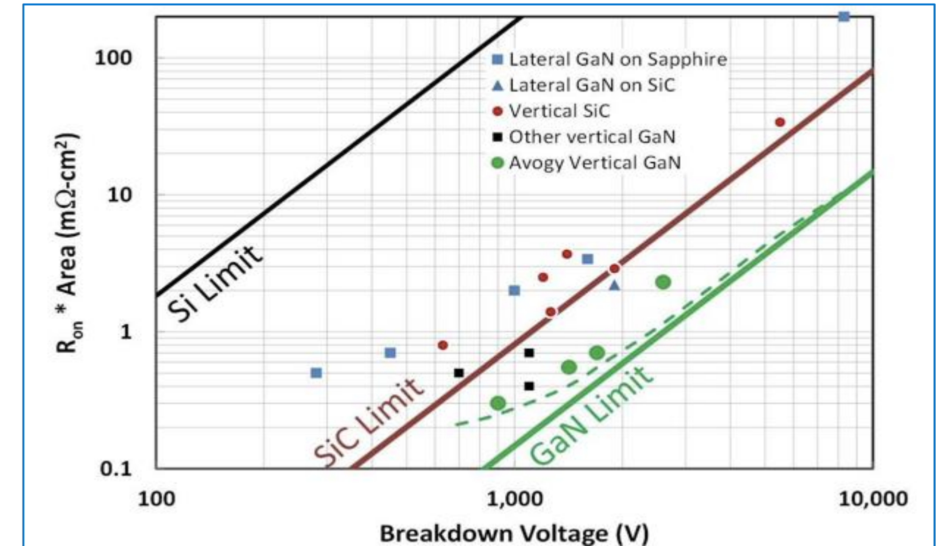
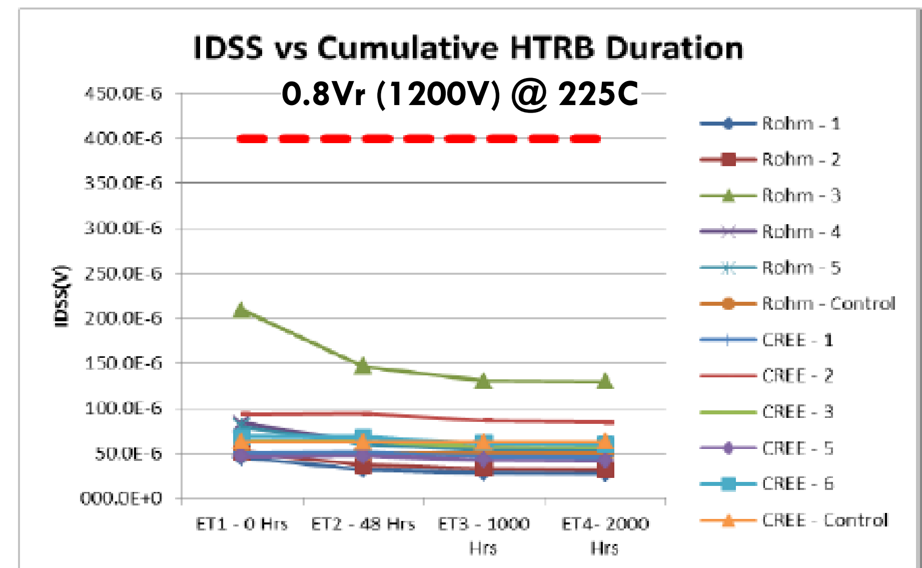
- The perfect switch has zero on-state resistance
  - Drain-to-source resistance in the on-state (R_{DSon})
- Intrinsic tradeoff with drain-to-source breakdown voltage
  - Thinner N^- layer and lower doping = lower R_{DSon}
  - Thicker N^- layer and higher doping = higher breakdown voltage
- Many applications prefer higher operating voltages
  - For a given power level, lower current, lower ohmic losses, lower temperature, etc.
- Because of a wider band gap, SiC and GaN have a 1000X lower R_{DSon} than Si for same breakdown voltage
  - Lower losses, higher currents, or smaller die size for same breakdown voltage
- Impressive long-term, high temperature performance





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WHY NOT WBG SEMICONDUCTORS?

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- Initial rollout of WBG power devices was not optimal (>10 years ago)
  - SiC diodes failing after 2 years in service
  - Failure rate of 4%/year and issues in with ThinQ SiC (dendritic growth and lack of guard ring)
  - Acharaya et. al. (2002) reported SiC Schottky diode failures at dV/dt > 50 V/ns

- WBG Quality and Reliability has three (3) Drivers
  - Die-Level Extrinsic (Presence of Defects)
  - Die-Level Intrinsic (Degradation Mechanisms)
  - Packaging-Level Intrinsic (Degradation Mechanisms)

- Reliability Physics of WBG can be challenging because die-level extrinsic has dominated most reliability studies to-date

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DIE-LEVEL EXTRINSIC - DEFECTS

- Semiconductor performance extremely sensitive to defect density
  - Si industry reduced defect density from 6/cm^2 (mid-1970's) to < 0.1/cm^2
- WBG devices initially on market had defect densities similar to early Si devices
  - One defect of concern is micropipes, which are a crystallographic defect
  - Shows up as faceted holes and can run the entire thickness
  - Results in breakdown at high electric fields
- Micropipe defect density is critical and can vary
  - Initially 25/cm^2 = no defects in 1x1 (2004)
  - Dropped to 2-5/cm^2 = no defects in 4x4/7x7 die (Si in '80s)
  - Now can be 0.2/cm^2 = no defects in 20x20 die
  - Some provide choices: Microsemi offers 15, 5, 1, or 0/cm^2
- Defect density likely had effect on change in SiC robustness
  - Action: Ask vendor for defect density of SiC die

Norstel Develops Low Defect 150mm SiC Substrates

Thursday 14th September 2017

Norstel AB, Sweden, has announces the successful development of low defect density 150mm SiC n-type substrates. "With a micropipe density (MPD) below 0,2 cm^{-2}

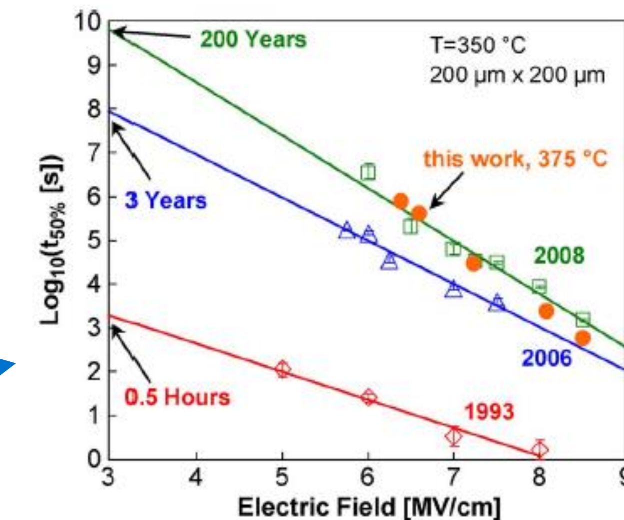

Fig. 13. Improvements of oxide reliability on SiC over the past 15 years. These data are measured on 200 $\mu m \times 200$ μm MOS capacitors at 350 °C.

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DIE-LEVEL INTRINSIC – dV/dt

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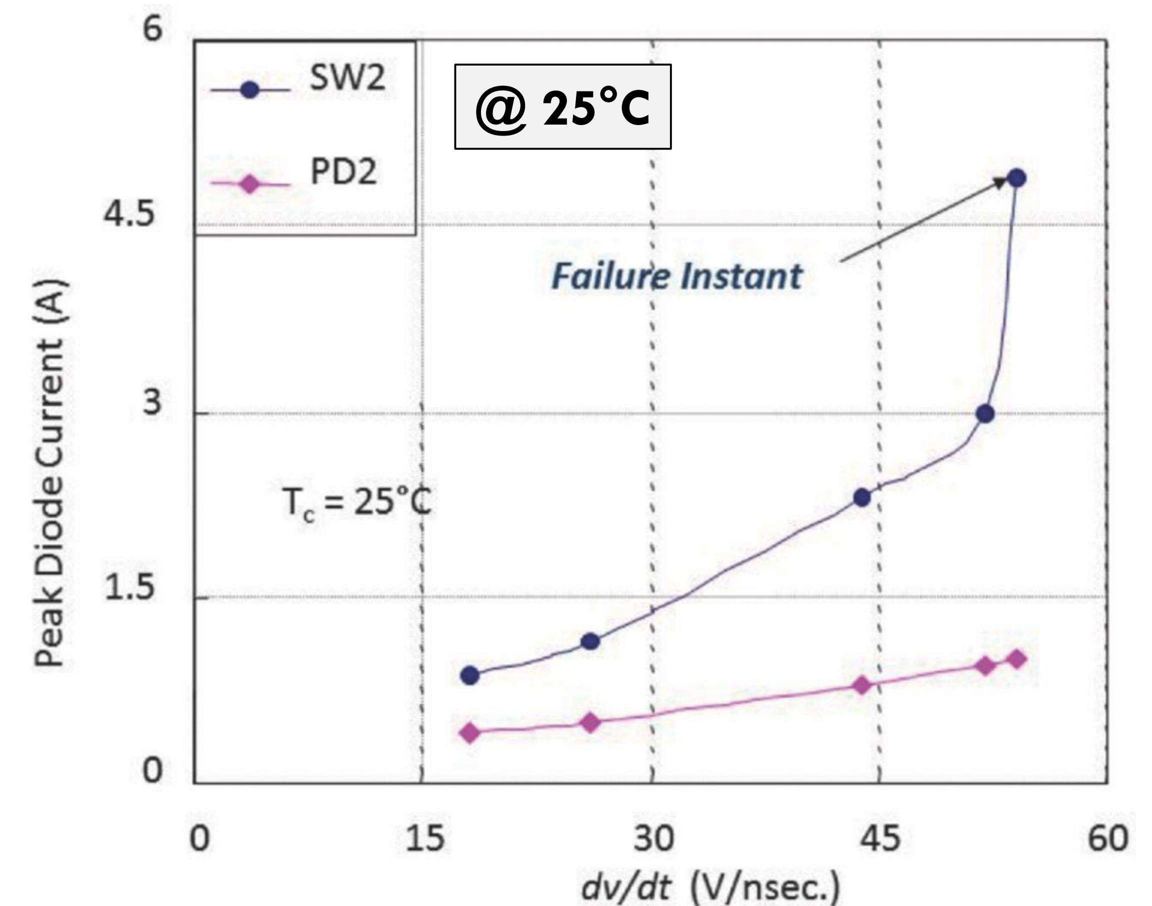
- Key limitation is inability to handle high dV/dt
  - Acharaya (2002) reported SiC Schottky diode failures at dV/dt > 50 V/ns
  - Microsemi believes dV/dt issues were due to surface defects at junction
- Recent experiment (right graph)
  - No failure of Si up to 100V/ns
  - At higher temps (~100C), SiC failed at 7V/ns, while still no failure of Si up to 100V/ns
- Action: Keep dV/dt < 10V/ns on the diode?

600V/6A **4H-SiC** Schottky barrier diode (SW2)
600V/8A **Silicon** merged pin – Schottky barrier diode (PD2)



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DIE-LEVEL INTRINSIC – THRESHOLD VOLTAGE DEGRADATION

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- SiC MOSFETs have thinner gate oxides compared to Si
  - Electric field in SiC gate oxide is ~2x silicon under on-condition and ~7x silicon under off-condition
- Drives degradation in threshold voltage (Vth)
  - Accelerated at elevated temperatures
- Trends are driven by polarity of gate voltage (Vgs)
  - Negative Vgs decreases Vth
  - Positive Vgs increases Vth
- Some vendors have solved the problem; others have not
  - Action: Ask for test data from vendors

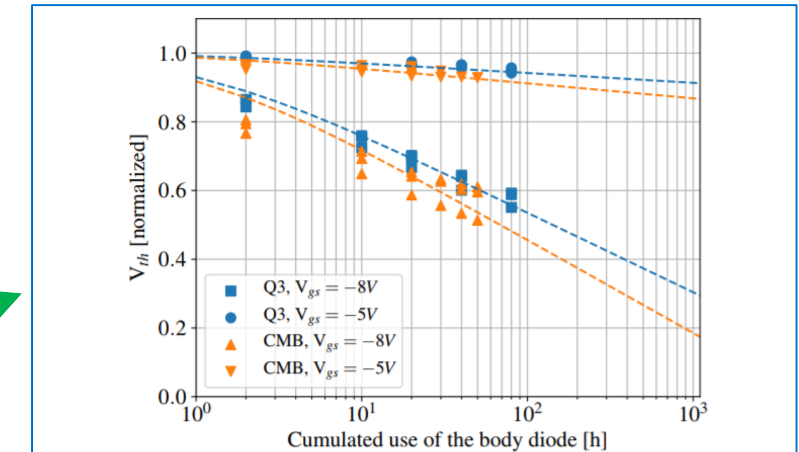

Figure 9: Evolution of the V_{th} as a function of time for the Static (3rd quadrant) and CMB tests (3 samples per test), data normalized for t=0, measured at I_d=100 µA, V_{dd}= 1 V, T_J= 25 °C. All tests were run at T_J=150 °C.

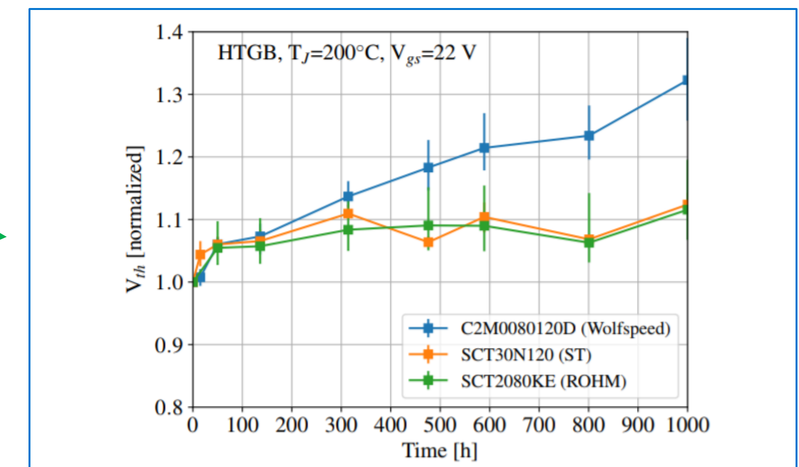

Figure 10: Evolution of the V_{th} for MOSFETs from three different manufacturers, in HTGB conditions (V_{gs}=22 V), for an ambient temperature of 200 °C.

Salvadó, Oriol Aviñó, et al. "Threshold voltage instability in SiC MOSFETs as a consequence of current conduction in their body diode." *Microelectronics Reliability* 88 (2018): 636-640.

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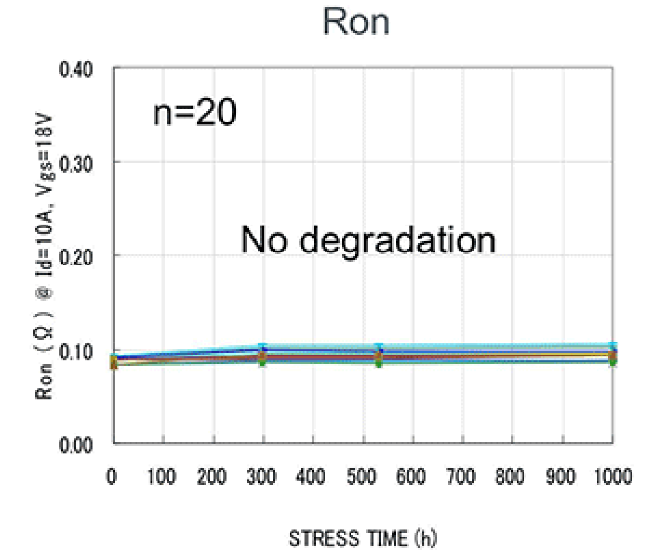
DIE-LEVEL INTRINSIC – BODY DIODE DEGRADATION

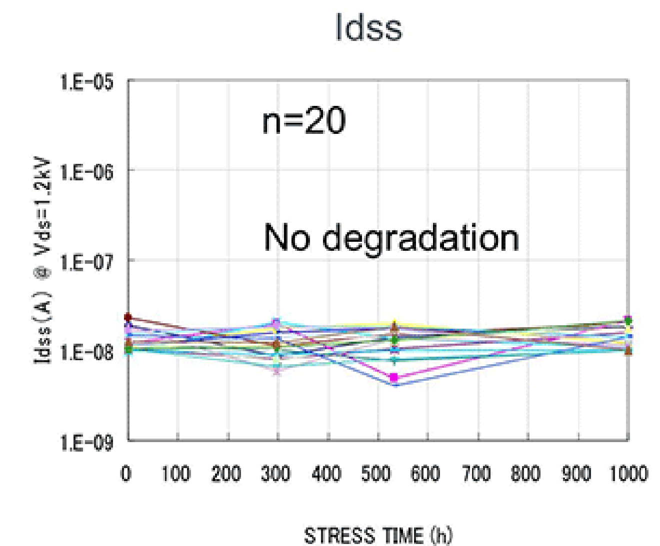
- SiC-MOSFETs have a fault mode called body diode conduction degradation
  - Occurs when forward current continues to flow in the body diode of a MOSFET
  - Driven by stacking faults (basal plane dislocation, BPD) that expand due to the recombination energy of electron-hole pairs
  - Affects current path; increases on-resistance (Ron), body diode forward voltage drop (Vf) and leakage currents

- Effect is less at low voltages (900-1200 V) and more at high voltages (>1700 V)
  - Use of free-wheeling external or built-in Schottky diode may not sufficiently prevent the damage.
  - <u>Action</u>: Degradation due to body diode varies among manufacturers and should be bench-marked

http://micro.rohm.com/en/techweb/knowledge/sic/s-sic/04-s-sic/6888

Body-diode conduction test (If=8A DC, Ta=25ºC, 1000h)
DUT: SCT2080KE (TO247 w/o SiC SBD).





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DIE-LEVEL INTRINSIC – SIC AND RADIATION

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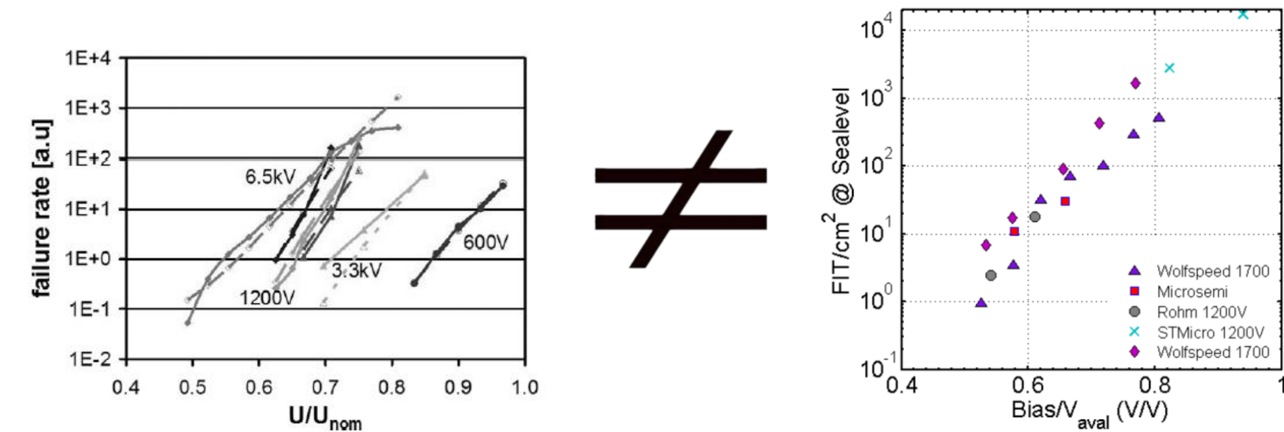
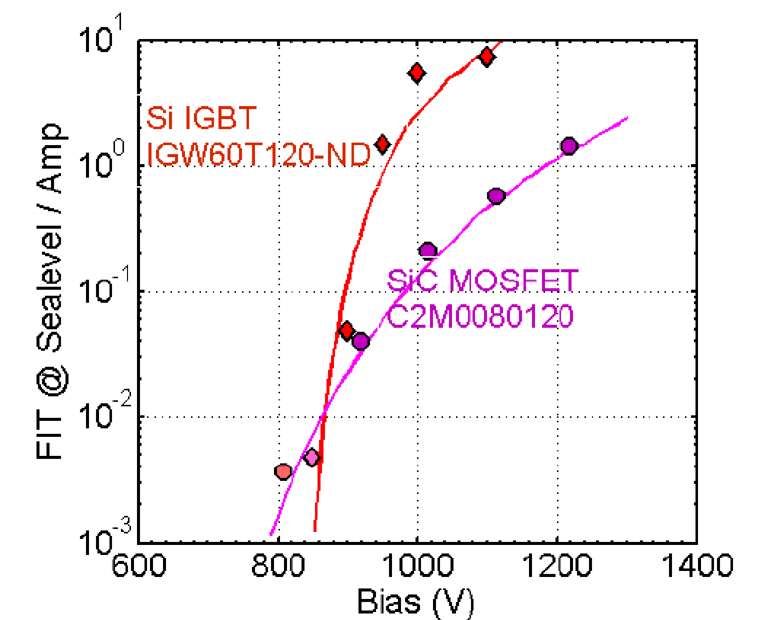
- In power devices (Si and SiC), cosmic radiation an issue above 300V
  - For terrestrial applications, neutrons are the concern
  - Failure mode is single event effect (SEU)
  - SiC struggles under heavy ion, but irrelevant for applications on Earth (gamma ray and TID also irrelevant)



- Challenge is differences in predicting performance
  - One study found different failure rates for different ratings
  - Another study claims failure rate is normalized by area, independent of voltage rating

- FIT rate can be higher than silicon at lower voltages



- Action: Calculate failure rate, compare to existing solution
  - Multiply the terrestrial failure rate by 4X to get Denver, CO
  - Note that failure rate drops with increasing temperature

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DIE-LEVEL INTRINSIC – OTHER

- Studies of SiC MOSFET have raised concerns on long term performance at elevated temperatures
  - Lelis measured unstable threshold voltage due to electron tunneling into and out of the oxide traps
  - Gurfinkel showed that conventional DC measurement technique underestimated threshold-voltage instability as fast transient trapping / detrapping events could not be captured with slow sweep rate
  - Yu reported hot carrier effects in SiC MOSFET operated at moderate drain bias

- SiC MOSFET will experience avalanche conditions due to high surge current and unintentional stray inductance in the current path.
  - Due to many defects in SiC material, adverse effects can happen such as increase in leakage current and RDSon.
  - Short circuit time may be 2-3 micro-seconds which may not be adequate for de-sat protection.

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