Understanding and Mitigating EOS and ESD in Electronics

DfR Webinar

April 28, 2016
Electro-Static-Discharge (ESD) or Electrical Overstress (EOS) related failures can have a significant impact on your product’s life expectancy and reliability. ESD is the sudden flow of electricity between conductive and non-conductive surfaces that builds an electric charge and then discharges it to ground, impacting any susceptible electronics in the path. For example, a person walking across a carpet and then touching a door knob can discharge as much as 15000V (65-90% humidity) which is usually above the threshold for most electronic components, yet does not hurt the human involved. Conversely, EOS failures are due to an overstress in a system either from a surge or overload on the circuitry. These failures exhibit much more damage due to the level of current or voltage incurred. This webinar will distinguish between the two failure modes and provide insight into what you need to do to protect your circuitry and deliver a reliable product.
There are three (3) predominant ESD models for IC's:

1) the Human Body Model (HBM);
2) the Charged Device Model (CDM); and
3) the Machine Model (MM).

There are many other ESD models for Systems:

IEC61000-4-2 / Human Metal Model (HMM)
ISO-10605, etc.

Not to be Confused!
ESD Models

- The HBM simulates the ESD event when a person charged either to a positive or negative potential touches an IC that is at another potential.
- The CDM simulates the ESD event wherein a device charges to a certain potential, and then gets into contact with a conductive surface at a different potential.
- The MM simulates the ESD event that occurs when a part of an equipment or tool comes into contact with a device at a different potential.
- HBM and CDM are considered to be repeatable 'real world' models, but MM is deprecated!
The Industry’s Challenge

ESD Susceptibility is only getting worse! As feature size continues to shrink, device robustness diminishes. Typical System Level stresses:

- 8KV
- 30 Amps
- 200 + ESD Events
- Testing while powered, can increase ESD damage susceptibility, over 50% in some applications
The Industry’s Challenge

A System ESD standard (IEC 61000-4-2) significantly increases amps (2 to 30) and response speed (nanoseconds to picoseconds) over IC ESD qualification standards.

Portable electronics increase environmental ESD threats

ESD damage is a lifetime product liability

Additional protection-specific transient Protection required

The chart above compares the IC 2000V Human Body Model for an ESD event (gold line at bottom) with a system IEC 61000-4-2 HMM 8000V Level 4 ESD event.
Impact of Scaling on ESD

Mobile computing is wide open to ESD damage. Each IC shrink reduces the oxide thickness and requires more ESD protection for which there is no room on the shrunk IC.

- Smaller IC geometries
- Reduced board space
- Higher frequencies
- Decreasing capacitance budgets for ESD protection
- Escalating #’s of signal lines
- Reduced budgets for ESD protection on chip & on PCB

Combined with
Impact of Scaling on ESD

• Every major IC technology advance has had mostly negative impact on ESD
• Today’s IC’s can no longer provide adequate ESD for portable electronics
• Compounding this, new circuit features and RF applications are increasing the complexity to both ESD and System Level IEC protection
What Do You Need to Do?

ESD Protection is necessary at the IC, component package and system level.

Different approaches are necessitated to achieve reliable protection.

Designing for ESD impacts both the product design but also the manufacturing process controls.

What are the technologies available to assure a reliable ESD protected Product?

At the IC level
At the component package level
At the system level

What are the testing methodologies available to ascertain protection levels?

Capacitive Discharge
Square Wave (Transmission Line) pulsers
Component Failure Mechanisms: ESD

- Objects moving with respect to each other transfer charge
  - Amount depends on materials, speed, proximity
  - Dissipation depends on conduction paths
- Extremely large voltages possible
  - Dry environment
  - Materials with easily stripped electrons
  - No discharge path
- Human perception > 5 kV
  - Circuits long since destroyed
Component Failure Mechanisms: ESD

- Two primary failure mechanisms:
  - Electric field-induced
    - Silicon dioxide breakdown $\sim 7 \times 10^8$ V/m
    - 60Å oxide destroyed at $\sim 4.2$V
    - Shorts gate permanently
  - Fields could push carriers into insulators
    - May just degrade performance
  - Thermal destruction
    - Any resistance in path subject to local intense heating
      - Contacts, vias, and junctions
      - Weakest link goes first
    - May also produce “walking wounded”
      - Increased leakage
      - Increased resistance
      - Softened junctions
  - Latent Damage may accumulate without any external failure signature
  - All protection techniques fail eventually
Component Failure Mechanisms: ESD

- Protection
  - Embedded circuits, shunts

- Design guidelines
  - Heat generated proportional to field x current density
    - Maximum at cylindrical junctions
  - Heat travels at Si/SiO2 interface
    - 10X difference in thermal conductivity
  - Al melts at much lower temp than Si
  - Uniform layout is crucial – avoid current crowding
    - Avoid “snaking” gates
    - As many contacts as feasible
    - Space contacts from junction edges
    - Wider metal better
    - Guard-ring any junctions
Component Failure Mechanisms: ESD Examples

- SEM of P/N junction
  Source: Frank, EDFAS, 2004

- SEM of metal line damage
  Source: Putnam et al., EDFAS, 2004

- Light emission of latchup in logic circuitry
  Source: Frank, EDFAS, 2004

- SEM & AFM of lateral ESD on line
  Source: Colvin et al., EDFAS, 2004

- SEM: HBM test on NFET
  Source: Putnam et al., EDFAS, 2004

- SEM of silicide shorts in SOI device
  Source: Prejean et al., EDFAS, 2004
ESD/EOS Injection Points

ESD/EOS Entry Vectors (Increasing Severity)

- Latent/Soft HBM/CDM Damage
- Hard HBM/CDM Strikes
- Failures detected in Device Test/Qual

- Latent/Soft HMM/Charged Board Damage
- Hard HMM/CBE Strikes
- Failures detected in System Test

- Latent/Soft Cable Discharge or System EOS
- Hard Cable/EOS Damage
- Failures detected in Functional Test

- Burn-in Elevated Temp/Voltage
- System Integration
- System Test

Turns Latent → Hardened Damage

Red Lines are Potential Latent Test Escape Paths

FIELD FAILURE
PROBLEM 1: Hard System Fails

When ESD **Hard** Failures Occur...

(System Qualification Fails / Field Returns)

**WHO IS AT FAULT?**

Hard Failures and EOS at the chip level are *usually* obvious, but the solutions at the system level are not!

Examples:
* Secondary Discharges
* Snapback Devices
  unloading bypass capacitors
* Induced Cable Discharge
  Events
**PROBLEM 2:** System ESD Design

When Non-Destructive *Soft* Failures occur, or *latent* ESD damage accrues...

...how to identify the right system nodes to begin analysis on?

Figure 9: cross section and close-up of CUT A
Design Practices for ESD

- Use ESD Industry Council SEED Method
- System Efficient ESD Design
  - Consider the potential “residual” ESD paths through the system
    - Identify all ESD Sensitive Parts on drawings
    - Mark Locations of ESD Sensitive parts on the Board with the ESD symbol
  - Consider the entire System (Design) as ESD Sensitive or Susceptible at some Level
  - Proper identification of Target Level Req'd
ESD Design Practices (cont.)

- Use ESD Protection on all susceptible parts (not just System I/Os)
  - Box or System I/O
    - ESD Rating > Class 2 IEC (4000V) MANDATORY
  - Internal Components (not exposed to outside connectors)
    - ESD Rating >= Class 1 ANSI (0-999V) MANDATORY
    - ESD Rating >= Class 2 ANSI (1000V)*** WHEREVER POSSIBLE
- High Speed, RF and GaAs parts will be particularly sensitive to ESD
  - GaAs Parts are typically rated as Class 0 (<250V) or Class 1A (<500V) – ONLY
    THE BEST PROTECTION DESIGN AND HANDLING PROCEDURES WILL PREVENT
    DAMAGE TO THESE PARTS!
- Place ESD sensitive components and traces to avoid locations where the
  board may be handled
- Consider ESD as well as RF shielding
- Where possible install protective devices before ESD sensitive parts
- Avoid Coupled ESD events – Do not route traces to ESD sensitive parts near
  lines connected to the outside world

*** 250V CDM and 1kV HBM Target Levels for components recommended by ESD Industry Council
for safe assembly with normal S20.20 ESD Protected Areas.
ESD Design Practices (cont.)

- Perform Circuit analysis to insure effectiveness of ESD protection (Class 2 ANSI [2000V] for internal, IEC level 2 [4000V] for I/O)
- Test Boards and Systems for Internal and I/O ESD tolerance
- ESD Protection devices must be connected to a good ground to accommodate up to 30A ESD spikes.
**ESD Scanning Analysis**

**I_{residual} ESD Analysis Concept**

KCL Current split between TVS and “Protected Device”/ASIC

Inductive Current Probe Measures "Secondary" shunt current on the node in question (i.e. USB D+)

This assumes, however, that the "problem current" is in the I/O node of interest. What about elsewhere?

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ESD Susceptibility Analysis

Susceptibility Scanning setup

Virtual Susceptibility Hotspot Diagram

STEP 1:
Inject an X*Y Array of
Increasing step-test ESD pulses
Into a moving loop probe (1kV, 2kV, 3kV etc at each point until failure)

STEP 2:
Log the ESD "fail level" in the step test where the system malfunctions, and
plot it with a color
enhanced 2D image to show ESD "hot spots"
ESD Current Reconstruction Analysis

- Extend the EMI scanning concept to “listen” to where the residual ESD pulse travels.
- Compare “with/without” for head-to-head protection decisions
- Finds unexpected secondary paths
  - This example was a USB port coupling into an Ethernet MAC. More TVS clamping made the problem worse!
Failure Criteria for Susceptibility?
(BER? Eye degradation? Catastrophic failure?)

LVDS port with TVS

LVDS w/ TVS after IEC testing; 500V steps thru 5kV; Then 12kV 3 times
"Relative Susceptibility" Example
(Different Chip Versions, same Function)

- JTAG PINS HERE (NOT AFFECTED BY EXTERNAL I/O)
- EXTERNAL PINS HERE, LIKELY TO SEE DIRECT ESD EVENTS!!!
ESD Sensitive Parts (Pin Sensitivity)

- Any pin of a discrete ESD sensitive part (FET, Transistor, etc) may need protection (if not connected to a supply)
  - Input pins
    - Can be sensitive since they have little or no built-in ESD protection
    - Especially on high speed devices like GaAs ICs or discretes,
  - Pins other than inputs (on an ESD sensitive part)
    - Can also be sensitive because an ESD pulse can affect internal voltage levels
    - Any improperly terminated or unprotected pin can be a conduit for ESD
  - Supply pins
    - Provide reference bias connections
    - Should not need additional protection (as long as they are connected to the power supply)
  - Outputs of logical or functional parts designed with active (usually buffered) output stages
    - May have clamping diode protection to the supplies and may not need additional protection – check the part ESD rating
Evaluate Potential ESD

- If ESD sensitive parts are used in design, the circuitry connected to device pins should be evaluated
  - Insure that it provides “attenuation” to prevent voltage in excess of the parts ESD rating from developing in case the pin or connected traces are contacted during board handling or system assembly.
- Often the recommended circuit components for operation of the part will provide adequate ESD protection.
  - This should be verified by analysis or simulation and extra protection added as required to limit the voltage seen at the part.
- Assumptions for analysis/simulation
  - 2000V, 1.5K, 100pf for Internal circuits
  - 4000V, 330 Ohms, 150pf for I/Os
Protection only divides the ESD current path, it does not strictly “divert” 100% of it. Analysis of the Current Sharing between TVS ($I_{SHUNT}$) and ASIC ($I_{RESIDUAL}$) is required.
ESD Protective Device Options

- Passive Networks
  - Capacitors – Simple, Low cost
  - Band-pass filters – Somewhat more complex, good ESD protection
- For lower speed devices
  - Schottky Diodes – Simple, but capacitance loads HF circuits
  - Diode Clamping Arrays – Good for LF circuits and outputs
- For higher speed devices (requiring low capacitance)
  - Low capacity protection diodes (<1 pf) – Robust, Good HF compromise
  - Polymer ESD (PESD) Protection devices (<0.25 pf)
    - Excellent HF characteristics, small size 0402, 0603
    - PESDs have limited Pulse life, good parts withstand 100 to 1000 strikes
    - Operating voltage typically 5V, available to 12V, Trigger Voltage 100, 150V
**Simple Capacitive Protection**

- Use to provide ESD protection on bypassed pins for ESD sensitive devices, or at Supply input connections
  - Make sure capacitance (C2) is significantly larger than the Human Body Model (>> 150pf) to minimize developed voltage (approx 28 times or 4000pf for protection of a Device with an ESD sensitivity of 150V)
  - May add a Resistor to bleed off charge (from C2)
  - Use 200V rated Cap (for C2)

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**Diagram**

- Human Body Model
- Protection Cap (C2)
Filters

- Band-pass filters can be used for higher frequency applications and can be effective for RF system inputs
- Very Robust circuit with good protection

Band-pass Filter 850-2GHz, 50 Ohm Impedance
C1, C2, C3 rated at 100V
Protection with Clamping Diodes

Protection Diode Array (CM1213-01)

ESD at output is clamped at approximately 14V with 4000V ESD hit through 330 Ohm resistance
PESD (Polymer ESD) plus Inductor

- The Inductor shunts lower frequency energy to ground, removing stress from the PESD.
- Provides better protection than the PESD alone and extends life of the PESD.
- The PESD can be used alone for wider bandwidth operation.

IEC HBM
PESD, Trigger
Voltage = 150V
Summary of ESD Design Guidelines

- Design ESD Protection for External (System) I/Os to IEC HBM Class 2 (4000V, 150pf, 330 Ohm) Including:
  - RF or signal inputs
  - Control and System I/Os that DO NOT have built in protection to the required limit
- Design ESD Protection for Internal ESD sensitive parts to meet ANSI 20.20 Class 2 (2000V)
- Know the ESD rating of every part used
- Select parts (where possible) to meet ANSI 20.20 ESD level Class 2 or better (2000V)
- Parts rated less than Class 2 should have additional protection circuitry added to protect the board during handling
ESD Design Guidelines (cont.)

- For External (System) Inputs use Robust protection:
  - Band pass filter
  - PESD plus Inductor (for Severe condition use PESD + Filter)
- For Internal ESD Sensitive pins use:
  - Single bypass Cap (where possible)
  - Filter if needed
  - PESD or PESD plus Inductor
- Any Pin of an ESD sensitive part may be at Risk If It is NOT:
  - Connected to a supply plane
  - Adequately decoupled to GND (~4000pf @200V)
  - Protected by a “filter” network (simulate for an ESD hit)
- External (System) Output or I/O
  - Use low capacitance Clamping diodes (1pf)
  - PESD if required for speed (.25pf)
Often difficult to distinguish between EOS/EOL (electrical overstress and electrical overload) and ESD. Some rules of thumb:

- **ESD damage**
  - Small failure sites
  - Not always visible without deprocessing
  - No visible evidence at the package level

- **EOS damage**
  - Large areas of damage
  - Burned silicon and metallization
  - Sometime visibly evident package damage
Trying to distinguish between EOS & ESD

- **EOS: Thermal overstress to a component’s circuitry**
  - Short Pulse Width Failure – Junction Spiking
  - Long Pulse Width Failures – Melted metallization and open bond wires
  - Junction spiking occurs when the amount of Al migration into the silicon substrate has reached the point wherein the Al has penetrated deep enough so as to short a p-n junction in its path. By that time an Al spike is said to have shorted the junction, damaging the device permanently.
## Relationship of EOS and ESD

<table>
<thead>
<tr>
<th>EOS</th>
<th>Amount of stress (spec was exceeded)</th>
<th>quantity of stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>Kind of stress (discharging of C)</td>
<td>quality of stress</td>
</tr>
</tbody>
</table>

EOS and ESD are **not alternatives** to each other; ESD can be a **cause** of EOS damage.

Understanding EOS

- Damage signatures from Electrical Overstress (EOS) are the leading reported cause of returns in integrated circuits and systems that have failed during operation. Solutions to this problem are hindered by a prevailing misconception in the electronics industry that insufficient robustness to electrostatic discharge (ESD) is a primary cause of EOS.

- Definition
  - An electrical device suffers an electrical overstress event when a maximum limit for either the voltage across, the current through, or power dissipated in the device is exceeded and causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.

Industry Council on ESD Target Levels -- White Paper 4: Understanding Electrical Overstress - EOS, April 2016"
Definitions

- **OVERLOAD** –
  - 1. A load greater than that which an amplifier, other component, or a whole transmission system is designed to carry. It is characterized by waveform distortion or overheating.
  - 2. In electronics, it is that quantity of power from an amplifier or other component or from a whole transmission system which is sufficient to produce unwanted waveform distortion.

**OVERLOAD CAPACITY** - The level of current, voltage, or power beyond which a device will be ruined. It is usually higher than the rated load capacity.

**OVERLOAD LEVEL** - The level at which a system, component, etc., ceases to operate satisfactorily and produces signal distortion, overheating, damage, etc.
How Should Absolute Maximum Ratings be Interpreted

The yellow line is the number of components suffering immediate, catastrophic EOS damage.

There are different methods a device manufacturer may use to determine AMR values. The manufacturer may pick very conservative AMR values not based on physical properties of the product. This results in a wide region C before the onset of immediate damage. Alternatively, the manufacturer may define the AMR values based on detailed circuit and technology understanding resulting in a more accurate prediction of the damage threshold. This can result in the near elimination of region C. Regardless of the method chosen, the manufacturer is solely responsible for defining the AMR.
Sources of EOS

- EOS is usually assigned to any visible damage signature that appears to have been the result of excessive voltage or current.
  - However, the damage could be a violation of an AMR caused by incorrect biasing in the application,
  - Over voltage, induced latch-up conditions,
  - Extreme uncontrolled ESD,
  - Misorientation, or something else entirely.
  - The damage may also have been due to a defect in an individual weak device, an improperly set AMR or an intrinsic weakness in the technology.
Definitions

- Electrically Induced Physical Damage (EIPD)
  - Damage to an integrated circuit due to electrical/thermal stress beyond the level which the materials could sustain. This would include melting of silicon, fusing of metal interconnects, thermal damage to package material, fusing of bond wires and other damage caused by excess current or voltage.

- Electrical Overstress (EOS)
  - An electrical device suffers electrical overstress when a maximum limit for either the voltage across, the current through, or the power dissipated in the device is exceeded and causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.
The three main categories where EOS damage can occur are:
- powered handling
- unpowered handling
- switching / alternating current (AC) applications
EOS Root Causes

Unpowered Handling
- Field induced events
- Charged people
- Charged devices / boards / systems
- Unsuitable processes

Manufacturing Process
- Inappropriate welding
- Unsuitable packaging
- Environmental factors

Handling & Storage
- Lack of / poor grounding
- Charged cables

Discharges
- Saturation of inductors
- Impedance mismatch

System Design
- Floating inputs
- System ESD
- Heat dissipation

EOS

Power Handling
- Lightning
- Unstable / incomplete tests
- Misinterpretation of standards
- Misorientation

Testing
- Hot switching / triggering
- Open / shorted supply lines
- Power supply sequencing
- Accidental power failures

Assembly
- Spurious violations
- Other components
- Overheating
- Intermittent contacts

Powerup / down
- PCB design
- Inductive switching
- Switching of capacitors

Power Transients
- Power up / down
- Fault voltage transients
- Inductive switching

EOS Root Causes

Industry Council on ESD Target Levels -- White Paper 4: Understanding Electrical Overstress - EOS, April 2016"
Points to consider include:

1) Proper understanding of AMR
2) Realistic specifications of AMR and customer realization of its limits
3) Accurate determination of the location and possible causes of the damage and finding the true root cause event which created the damage
4) Understanding the use application and impacts to the IC’s ESD protection design
5) Lessons learned from product returns from both manufacturing and the field
Tools to Help

System Transient Event Analysis Tools

• Several new tools are now available to the EMC engineer to help resolve EMC issues, insure better reliability and future EMC compliance. These include:

  – ESD/EMC Immunity scanning
  – RF Immunity Scanning
  – EMI Emissions scanning with Phase Measurements
  – Resonance Scanning
  – Current Spreading scanning
Customer Returns Exhibiting EOS Damage

- Root cause diagnosis of EOS damage requires knowledge of the application at the time of the damage. This involves the following:
  - where in the application or system the damage occurred
  - environmental conditions at the time of the damage or during the test which revealed the damage, in terms of automotive, this would include the environment within the particular location of the car
  - schematic / layout of board devices in the application
  - details of the supply, ground and input/output (IO) connections and voltages at the time of damage
  - details on the interconnection of devices on the board which could provide paths for the electrical stress
  - Any possible “precursors” to damage (on the supplier side, determination of IC process, IC assembly yield, test issues, or results of device analysis indicating a weakness; on the system manufacturer side, tester programming / hardware, or connection related issues in the application)
Transients

- There are many ways a transient can enter into a system. Some may be from a directly applied source including, but not limited to:
  - overvoltage spikes on supplies
  - charging / discharging of large value capacitors directly into system pins
  - long charged cables connecting directly into system pins
  - a system being supplied with power before its connection to ground (connection of a board into a system plug contacts supply pins before ground pins)
  - Inductive kicks or loads
Other Sources

- Process induced – Such as those in assembly or IC misprocessing resulting in low breakdown, direct shorting, or unintended high current density path from device die to IC pin.

- Charged board – Sudden discharging of a charged board to a ground potential can result in discharge paths through the board’s supply and ground tracks which directly route to or through components causing excessive current densities and component damage.

- Test induced – Excessive voltage transients resulting from incorrect power supply switching or incompatible switch control voltages, glitches on supplies, program induced misbiasing of supplies, incoming testing using charged multimeters.

- Coupling of external radiated energy into unprotected devices of a system – This can occur in those applications which generate or are in the range of this type of energy and which can also cause high voltages / currents that cause damage in systems and components.

Industry Council on ESD Target Levels -- White Paper 4:
Understanding Electrical Overstress - EOS, April 2016
Additional Causes of EOS

- Oscillation
- Linear mode
- Shoot through
- Vendor quality
- Welding (soldering)
- Electrostatic coating
- Outsourced processes
- Fails at card lamination (customer)
- Connection to neighboring device
- Weakness in PCB design
Often the analysis of a potential EOS event starts with the identification of a damaged part. To determine the reason for a non-working system or component, the technical expert needs to identify the broken part in the system and perform a detailed inspection of the system, component, board and IC.

For example, one typical EIPD signature, which suggests an EOS event as root cause, is an extended melt area of metal routing on the IC (often on the order of >100 µm). This is an indication of a very powerful energy pulse, excluding pulses such as a low energy ESD pulse during IC handling as root cause. Knowing that dissipated energy is a function of the current through a resistance, and the time (Energy (J) = Current\(^2\) (A) * Resistance (ohm) * Duration(s)), examples of various amounts of dissipated energy through a 1 ohm resistance as a function of the surge or stress are shown on the next slide.
# Analysis of EIPD and EOS

<table>
<thead>
<tr>
<th>Surge/Stress</th>
<th>Application</th>
<th>$I_{\text{peak}}$ [A]</th>
<th>Duration</th>
<th>Typical range of energy*</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDM</td>
<td>component</td>
<td>3-6</td>
<td>0.8 ns</td>
<td>1 - 10 nJ</td>
</tr>
<tr>
<td>HBM</td>
<td>component</td>
<td>0.7</td>
<td>150 ns</td>
<td>100 nJ</td>
</tr>
<tr>
<td>IEC61000-4-2</td>
<td>system</td>
<td>16</td>
<td>120 ns</td>
<td>10 $\mu$J</td>
</tr>
<tr>
<td>ISO7537:1</td>
<td>system</td>
<td>10</td>
<td>2 ms</td>
<td>100 mJ</td>
</tr>
<tr>
<td>ISO7637:5 (load dump)</td>
<td>system</td>
<td>43</td>
<td>40-400 ms</td>
<td>10 - 100 J</td>
</tr>
</tbody>
</table>

* in 1 ohm resistance

Another example is the ignition of heavy vehicle engines by large supply sources through insufficient contacts or MOV/Capacitor combinations that don’t limit the voltage levels sufficiently.

The three analysis steps can be summarized as:

- **What has happened?**
  - Describe the situation at which the fail occurred and which part has failed.
  - Complete failure analysis (Chapter 6) to identify the EIPD and determine possible causes.

- **How has it happened?**
  - Analyze the path of the stress pulse and its electrical parameters like pulse length, polarity, etc.
  - Look to replicate the EOS event at either the supplier or customer site to better understand the EIPD.

- **Why has it happened?**
  - Get an understanding of how the stress aggressor, victim and protection have interacted during the stress.
EOS Images

Two locations on same signal line
EOS Images

- Melted Coupling Diode
**EOS Due to Board Layout Spacings**

<table>
<thead>
<tr>
<th>Voltage Between Conductors (DC or AC Peaks)</th>
<th>Minimum Spacing</th>
<th>Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bare Printed Board</td>
<td>B1(^1)</td>
<td>B2</td>
</tr>
<tr>
<td>0-15</td>
<td>0.05 mm [0.002 in]</td>
<td>0.1 mm [0.004 in]</td>
</tr>
<tr>
<td>16-30</td>
<td>0.05 mm [0.002 in]</td>
<td>0.1 mm [0.004 in]</td>
</tr>
<tr>
<td>31-50</td>
<td>0.1 mm [0.004 in]</td>
<td>0.64 mm [0.025 in]</td>
</tr>
<tr>
<td>51-100</td>
<td>0.1 mm [0.004 in]</td>
<td>0.64 mm [0.025 in]</td>
</tr>
<tr>
<td>101-150</td>
<td>0.2 mm [0.0079 in]</td>
<td>0.64 mm [0.025 in]</td>
</tr>
<tr>
<td>151-170</td>
<td>0.2 mm [0.0079 in]</td>
<td>1.25 mm [0.0492 in]</td>
</tr>
<tr>
<td>171-250</td>
<td>0.2 mm [0.0079 in]</td>
<td>1.25 mm [0.0492 in]</td>
</tr>
<tr>
<td>251-300</td>
<td>0.2 mm [0.0079 in]</td>
<td>1.25 mm [0.0492 in]</td>
</tr>
<tr>
<td>301-500</td>
<td>0.25 mm [0.00984 in]</td>
<td>2.5 mm [0.0984 in]</td>
</tr>
<tr>
<td>&gt;500</td>
<td>0.0025 mm/volt</td>
<td>0.005 mm/volt</td>
</tr>
</tbody>
</table>

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**Note 1:** These values presume woven fiberglass coated with epoxy-based resin systems; other systems may have different values.

B1 = internal conductors, B2 = External uncoated conductors to 10,007 feet, B3 = external conductors uncoated conductors above 10,007 feet, B4 = coated external conductors
A5 = External conductors with Conformal Coating, A6 = uncoated traces to 10,007 feet, A7 = component leads conformally coated.
Thanks

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Reference Links

- Industry Council on ESD Target Levels
  - http://www.esdindustrycouncil.org
  - WP3 P1&2: System vs Component ESD/SEED
  - WP4 Understanding EOS

- EOS/ESD Association
  - http://www.esda.org
  - Six Part Series on ESD Fundamentals

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