Predicting the Reliability of Zero-Level TSVs

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Through Silicon Vias (TSV) are the next generation technology for system in package devices and are similar to plated through holes in a PCB from a reliability behavior perspective. The promised advantages include thinner packages and a greater level of integration between active die. The process is still being optimized and costs must be reduced for widespread adoption.

TSV is rarely justified by just miniaturization alone as it is more cost-effective to thin, stack and wire bond. Cost can be 2X-4X price of flip chip ($200/wafer is the goal) and 5X-10X the price of wire bonding. TSV will be justified by performance; specifically an increase in inter-die I/O, increase in bandwidth, and a corresponding decrease in interconnect length as shown in Figure 1.

	On-Die	On-Package			Off-Pkg
		2D Planar MCP	Substrate Embedded Die MCP	3D Stacked Di MCP	
	CPU Memory		CPU Memory	Memory CPU	CPU Memory
I/O Speed		4–7Gb/s	4-10Gb/s	10+Gb/s	4Gb/s
# of Connections		200-400	400-10,000	10,000+	~4–6 channels DDR
Bandwidth		100-200 GB/s	200 GB/s – 1 TB/s	> 1 TB/s	< 100 GB/s
Capacity	< 50 MB	512+ MB	< 512 MB	< 512 MB	> 1 GB
Interconnect Length	< 1 mm	~7 mm	1-3 mm	1 mm	> 100 mm

Figure 1 – Performance Versus Technology [(1)]

This paper will present two different approaches to the generation of TSVs as the vias can be created at various stages of the process: By the wafer provider, IC manufacturer, or packaging house.

The paper will also address the techniques for creating the TSVs e.g. etching and lasering with respect to their differences and results as well as provide insight into the various approaches for filling the vias. A comparison between solid fill, polymer fill and no fill concepts will be made.

Finally, the paper will address the three primary failure mechanisms for TSVs, that of, cracking of the copper plating, cracking of the silicon /change in resistance of silicon and interfacial delamination of the via wall from the silicon. The paper will conclude with a focus on the challenges for this technology as the exact process and architecture (materials, design) for TSV has yet to be finalized which in turn can lead to large changes in stress states.

Introduction

Semiconductor integration has continued for several years in the electronics industry, essentially in a two-dimensional approach. This continuing reduction in gate geometries and packaging has resulted in a drive toward interconnection of dies in a 3D approach without increasing power, by utilizing connections through the silicon itself. This process of interconnection, called through-silicon-vias (TSVs), provides a means of connecting signal paths from the top of a die to the bottom for easier, faster die to die signal propagation by utilizing the area under the bond pads. Vertical chip stacking in a single package increases the amount of silicon that can be put into a given package footprint. Stacking die also provides a faster signal path as a result of the shorter die to die routing and reduces the number of placements for board assembly by reducing the number of components. Connecting devices in a 3D approach promises higher clock rates, lower power dissipation, and higher integration density.[2] However, many of these new technologies are implemented before the reliability of the technology is full understood.

This paper will address some of the failure modes that occur with TSV's and the resultant impact on reliability.

Approach

Before getting into the failure modes, it is useful to understand the different methodologies used for the creation of TSVs, as this variability has a significant impact on predicting the reliability of the products using TSV technology.

There are different approaches used in the generation of TSVs, the Via First (FEOL) Front End of Line and Via First or Last (BEOL) Back End of Line. The reason for these different approaches is that vias can be created at various stages of the process: by the wafer provider, IC manufacturer, or packaging house.

At the foundry TSVs can be inserted just before device fabrication which is before the front end of line
(FEOL); or just after the devices have been fabricated. This still occurs before the fabrication of the on-chip interconnect and before the back end of line (BEOL). If the TSVs are generated FEOL ,then the
conductive material selected for the vias is typically doped polysilicon. This polysilicon deep trench TSV technology has been described in detail in many publications.[2] Although the polysilicon connections are not as conductive as copper connections, they provide sufficient conductivity for many applications. If the TSVs are fabricated after the devices are formed, tungsten or copper can be used. Engineers at IMEC in Belgium have developed a FEOL copper-based process called "copper nails."

Figure 2 compares the FEOL and BEOL manufacturing flows.

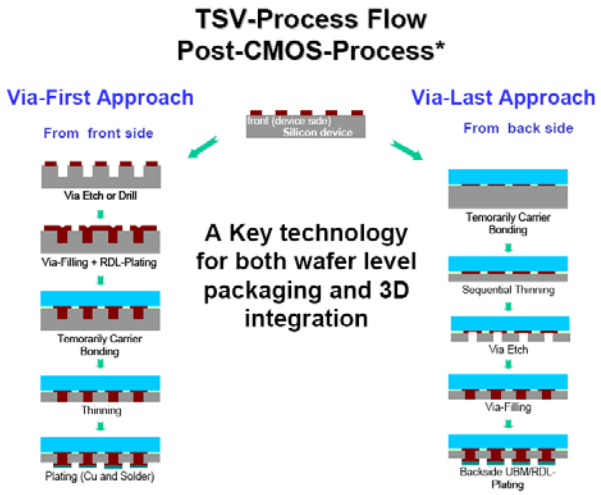


Figure 2 – Via First versus Via last Manufacturing Flows

The creation of TSVs have essentially 3 steps to the process; silicon via etching, via insulation and via metallization. The next paragraphs will briefly describe these process operations.

DRIE Via Etching

Dry Etching or Bosch Etching was developed more than a decade ago for the MEMS industry. The Bosch process alternates between short isotropic SF6 plasma etches for the removal of silicon and short C4F8 plasma deposition steps for sidewall passivation. Current etch rates are approximately 50 um/min. For next generation thinned die, this could allow via formation in less than one minute. DRIE is capable of creating very high aspect ratio vias with no limit on minimum diameter.

Laser Etching/Drilling

Being maskless, the laser etching process eliminates PR coat, expose, develop and strip processing.
The laser process produces sloped sidewalls which are more conducive to barrier and seed layer deposition and can "drill" through oxide and nitride layers as well as Al, Cu, Ni and Ti metallizations.

In DfR's opinion, laser drilling will likely dominate at this time. Initial adoption of the technology will be for memory stacks and interposers. Neither approach requires large numbers (10K+) of small diameter connections. Under this configuration, laser drilling is more cost effective and easier to implement. CPUs will likely not utilize TSV until 10K+ connections can be made between die, at which point reactive etching may become the technology of choice. Figure 3 illustrates this cost transition point.

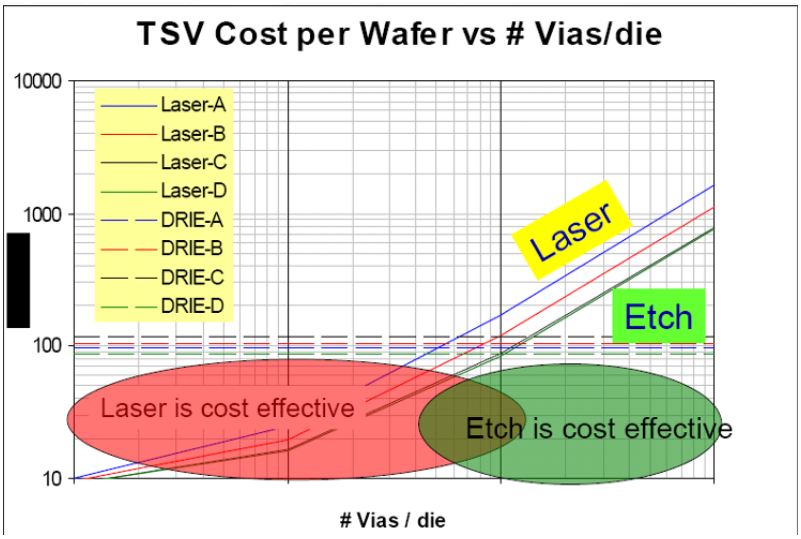


Figure 3 – Laser versus DRIE Etching Transition

Via Insulating
After via formation, oxide (SiO2) insulation layers are typically deposited by CVD using silane (SiH4) or TEOS. If the TSVs are being insulated and filled after chip fabrication, care has to be taken with the deposition temperature. Typical TEOS deposition processes are in the 275-350°C range. To reduce the deposition temp, one option is the use of Parylene precursor, which can be deposited at room temperature, as a conformal organic insulator for TSVs.

Via Filling
The final step in the generation of TSVs is the filling of the via. It is important to know what aspect ratios will be required for various via diameters both in terms of creating the vias and filling them. Most cost of ownership (CoO) models show that via formation and via filling are the major cost barriers for 3-D, but this depends on size, pitch and aspect ratio.

Via Fill Tradeoffs

Solid Fill using copper, nickel, tungsten, aluminum, etc. is the most robust with respect to fatigue, although there can be a high stress in silicon. It is the longest process yet provides greater density (similar to filled microvias) and provides enhanced thermal performance.

Polymer Filling of TSVs is still robust, induces a reduced stress in silicon, is a shorter process but utilizes more expensive material.

No Fill (annular) is the least robust, yet provides the lowest stress on the silicon, is the fastest process and as such results in the lowest cost. Figure 4 illustrates this concept.

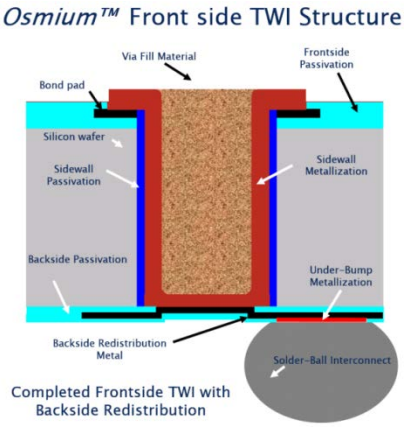


Figure 4 – Typical Filled TSV

How Can Through Silicon Vias (TSV) Fail?

Through Silicon Vias have three primary failure mechanisms; Cracking of the Copper Plating, Cracking of the Silicon /Change in Resistance of Silicon, and Interfacial Delamination of Via Wall from Silicon. There are several challenges in ascertaining all of the relevant failure mechanism involved as the exact process and architecture (materials, design) for TSV has yet to be finalized and can lead to large changes in stress state.

For example, is the copper deposited through electroplating or chemical vapor deposition (CVD)? CVD is used primarily for small holes (<3um dia.) having high aspect ratio, while EP is used for larger holes (>5um dia.). Will there be an anneal after plating? Stress free temperatures can also be completely different. For example, electroplated copper is stress free near room temperature (25 – 50C) but CVD can occur at 400C and annealing can occur around 200C. Figure 5 shows these variations in stress levels.

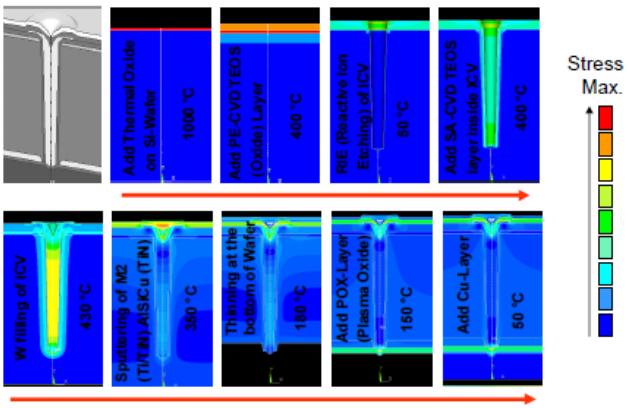


Figure 5 - Stress States Through TSV Processing [3]

Another failure mechanism is the cracking of the copper TSV. Issues at this operation include whether the copper in TSV will experience fatigue cracking. Classic circumferential fatigue cracking of copper plating is currently unlikely for two reasons:

Reason #1: Hole Fill - Most TSV concepts seem to be moving to a solid plug design (fully filled) (Figure 6a). Whereas a partial fill or plated barrel may likely produce a process defect (pinch off due to non-optimized leveler) as shown in Figure 6b.

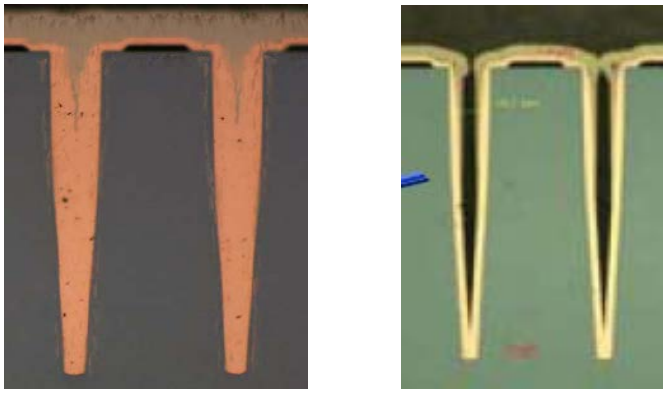


Figure 6 – (a) Solid Fill Via on left and (b) partial fill on right

In comparison, filled PCB vias (copper, solder, or conductive fill) do not fail when subjected to temperature cycling. Except for one key point where partially filled PCB vias fail faster due to the presence of a stress concentration.

Reason #2 involves the unfilled via and compressive stress. Unlike in PCB, the 'matrix' (i.e., silicon) has a lower coefficient of thermal expansion (CTE) than the barrel. In addition, there is also a lower CTE mismatch (PCB: 50ppm vs. 17ppm (33) / TSV: 2ppm vs. 17ppm (-15). If electroplated, the stress free state should be at room temperature. Any increase in temperature, due to hot spots or change in ambient conditions, will place the copper plating under an axial compressive stress. The tensile stress then arises circumferentially and could induce cracking along the length of the via, but will not cause electrical failure, as shown in Figure 7.

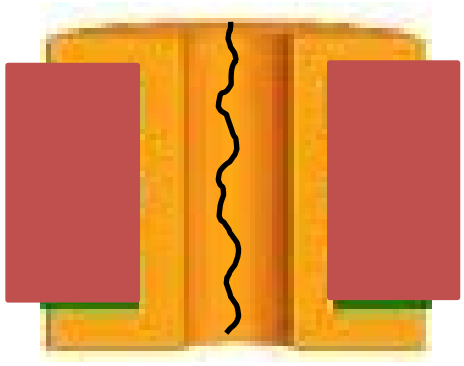


Figure 7 – Crack Along Length of Via

DfR observed one publication which seems to show stress-driven cracking of a TSV, but little additional information is provided. This is shown in Figure 8

Shear stress for plated Cu is dangerously close to yield for ~250°C TSV processing temperatures and CTE differences. What happens if we place an additional time or spatial gradient driven stress from power up and power down cycles or hot spots of 30-60°C?

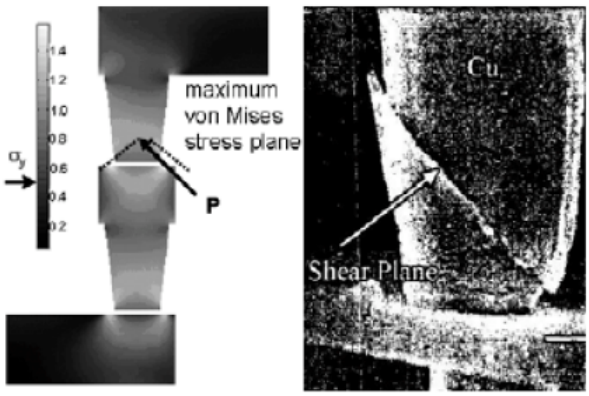


Figure 8 – Stress Crack[4]

Cracking of Silicon – Single TSV

Stresses within the silicon can be computed using the plane-strain analytical solution known as the Lamé stress solution.

Cylindrical [5]

$$\sigma_r^{Si} = -\sigma_\theta^{Si} = \frac{-E\ \varepsilon_T}{2(1-\nu)}\left(\frac{D_f}{2r}\right)^2$$

σ_r and σ_q are radial and circumferential stresses
E is modulus, $\varepsilon_T = (\alpha f - \alpha m)\Delta T$ (thermal mismatch strain), D_f is TSV diameter, υ is Poisson's ratio

Cartesian [6]

$$\sigma_{xx}^m = -\sigma_{yy}^m = -\frac{r^2 B \Delta\alpha \Delta T (x^2 - y^2)}{2(x^2+y^2)^2}$$

σ_{xx} and σ_{yy} are in plane stresses
B is modulus, $\Delta\alpha\Delta T$ is thermal mismatch strain, r is TSV radius

Figure 9 illustrates the effects of TSV height and diameter with respect to the stress level, with the stress being reduced with increased height and increased with increased TSV diameter.

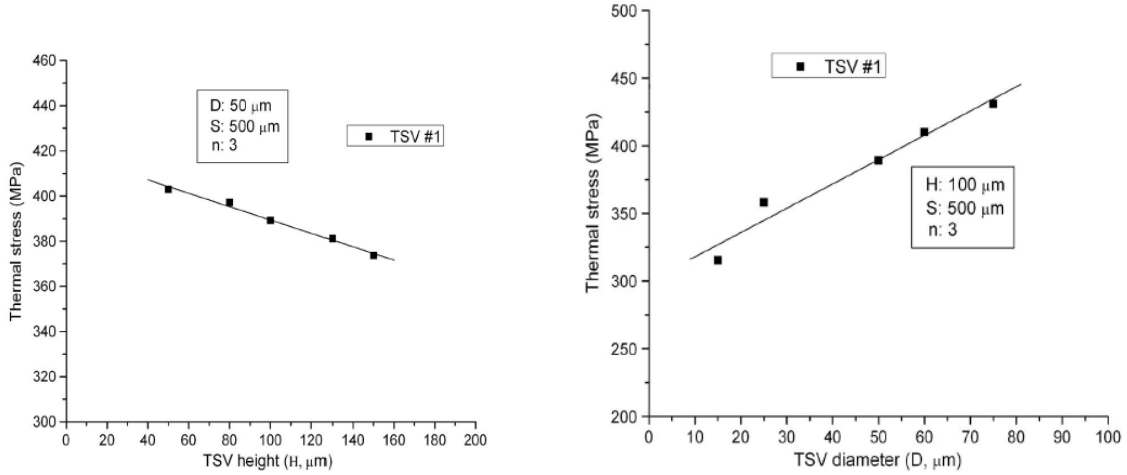
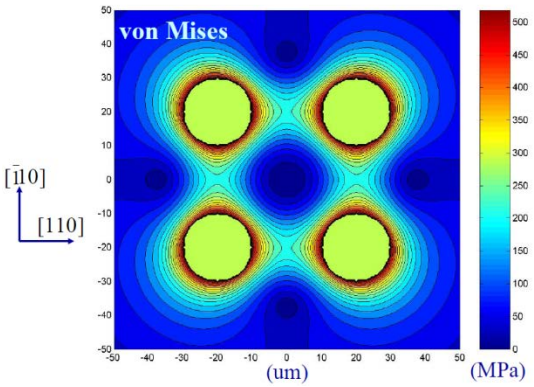


Figure 9 – Change in Stress as a Function of TSV Height and Diameter [6]

These results beg the question - Are these stresses high enough to cracking semiconductor-grade silicon? DfR's opinion is that this is unlikely as fracture strengths of silicon wafers have been reported between 1 – 20 GPa [7] there has been some debate about silicon and fatigue with Dauskardt reporting no fatigue behavior while Ritchie reports fatigue behavior up to 0.5 fracture strength.

These stresses can be adjusted for a TSV array, where D is the TSV, diameter, H is the TSV height, and S is the spacing of the TSV array as shown in Figure 10.



$$\theta_2^* = \theta_1^* \cdot \frac{1}{1 - R_{VS}^*} = \frac{D^{*2}}{H^*} \cdot \frac{1}{1 - \frac{\pi}{4} \cdot \frac{1}{(S^*+1)^2}}.$$

Figure 10 – von Mises Stresses on TSV Array [9]

The array does not create a substantial rise in stress. The maximum stress is theoretically 4.66 times that of a single TSV, but requires very close spacing.

Interfacial Failure of TSV

In DfR's opinion, this failure mechanism is the most likely failure mode of TSVs. There are very high and complex stresses involved and it is very difficult to measure the material properties. Key material properties are not controlled (i.e., fracture strength) and analysis by Dudek identified the risk of micro cracking and delamination problems at the upper via pad in a local model. [8] In his research, Liu found that Cu/SiO2 interfacial cracks and SiO2 cohesive cracks are likely to initiate and propagate at the

corners of electroplated Cu pads, where large stress gradients and plastic deformation exist [10]

The interfacial delamination of TSVs was found to be mainly driven by a shear stress concentration at the TSV/Si interface which can result in TSV extrusion, fracturing the overlaying dielectric material. [10] This is illustrated in Figure 11.

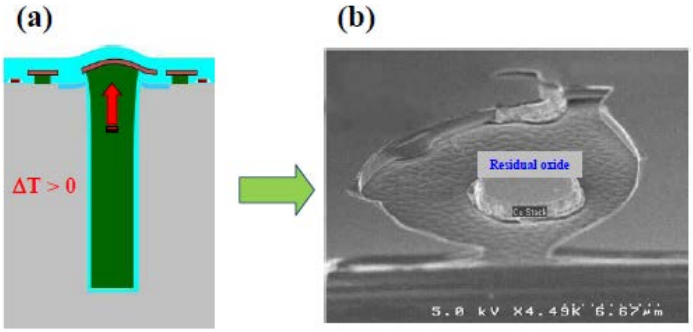


Figure 11 – TSV Interfacial Delamination

Summary

The ability to predict TSV reliability still in its infancy and is hampered by little published test data (primarily simulation). Any prediction must take into account changes in interfacial material. DfR recommends an approach of: don't simulate/test nominal; investigate realistic worst-case.

However, there is no need to reinvent the wheel. A significant amount of relevant material, especially in regards to interfacial reliability can be found in studies on fiber-reinforced ceramic composites

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