

White Paper
**0.3mm Pitch Chip Scale Packages:
Changes and Challenges**

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Industry Trend

The movement to 0.3mm pitch in chip scale packages (CSPs) can be considered inevitable. The electronics industry is rarely willing to make a leap to a unproven technology will gradual improvements in existing processes are sufficient (Moore's law being a classic example).

To successfully move to 0.3mm requires buy-in from the entire manufacturing industry, from the printed board manufacturer, to the solder paste supplier, to the stencil manufacturer, and a comprehensive understanding of the potential reliability risks the change in interconnect design may entail.

Printed Board Challenges

As a first step in adapting to 0.3 mm (12 mil) pitch, printed board manufacturers are developing processes to allow for 2 mil (50 micron) spacing and 2 mil trace width. Why 2 mil? The expected board bond pad diameter for a 0.3mm pitch device will be 0.15 mm. With only 150 microns (6 mil) spacing, 2 mil is the largest trace that can be routed under these new component packages (though, most designs will likely use a filled via-in-pad to route internally instead).

One of the processes PCB manufacturers are introducing is a reduction in copper foil thickness. While this would typically be the provenance of the laminate industry, PCB suppliers are finding costs can sometimes be lower by purchasing laminate with 0.5 ounce copper (17 microns) and reducing the thickness to 0.25 ounce copper (8 microns) through an additional etching process.

While the thinner copper does provide several advantages, including reduced lateral etching, more uniform trace width and tighter width control (approximately ± 0.25 mil), there are some potential reliability issues with this change in board architecture. The most critical is trace cracking. This is driven by thinner copper, which can potentially introduce bamboo-type structures that are more brittle, in combination with newer printed board formulations (phenolic, halogen-free, filled) that can introduce sub-surface cracks that initiate trace fracture.

Solder Paste

Continued reduction in stencil apertures and bond pad dimensions are forcing solder paste suppliers to continue modifying formulations and reducing particle size. As seen by the table below, type 5 or type 6 solder paste, with particle sizes potentially down to 10 microns, will likely be the preferred material set for 0.3 mm pitch (12 mils) attachment. This is especially true if one follows the general rule of maintaining a minimum of 4 or 5 solder particles across the stencil opening (assume 0.15 mm).

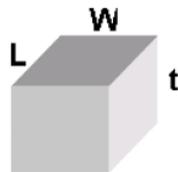
Taking into consideration particle distributions, we can see that we are rapidly approaching sub-micron particles (or nanosolder, if one wants to throw in a little marketing). While changes in solder paste chemistry and performance can be expected, the increasing ratio of surface area to volume in these small particle systems may start to influence coalescence behavior and storage times as well.

Powder for Solder Paste

Powder Type	Type in IPC-SPEC.	Particle size	Remarks
50	Type 2	53 - 10 um	25mils pitch
42	Type 3	45 - 25 um	20mils pitch
32	Type 4	36 - 25 um	16mils pitch
21	Type 5	25 - 15 um	12mils pitch
10	Type 6	15 - 5 um	Wafer bumping

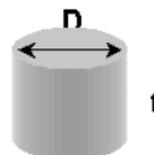
Stencil Printing

Stencil design and printing process will be critical to the successful implementation of 0.3 mm pitch CSPs. One of the quantifiable success factors in stencil printing is maintaining a minimum area ratio. The area ratio is the area of the aperture over the area of the aperture wall.



$$A_{\text{opening}} = L \times W$$

$$A_{\text{walls}} = 2(L \times t) + 2(W \times t)$$



$$A_{\text{opening}} = \pi D^2/4$$

$$A_{\text{wall}} = \pi D t$$

The actual minimum area ratio tends to change for different solder paste types. For standard Type 3, the number tends to be 0.66, while pastes with even smaller powder have minimum area ratios closer to 0.5. Regardless, for a 0.15 mm (6 mil) bond pad, maintaining either of these ratios would require stencil thicknesses of less than 4 mil.

These stencil requirements can be problematic for larger or non-fine pitch components, which can potentially experience solder starvation or solder bridging or solder balls (if the stencil aperture is widened to introduce more paste on pad). All of these challenges are, of course, before attempting to select the type of stencil technology (electroformed or laser cut) or the process parameters (pressure, speed, etc.).

Reliability

As usual, reliability is often the last issue to be considered. While minimum modeling or testing has been performed, the relatively small volume of solder and the non-uniformity of the interconnect geometry (0.15 mm bond pads on board and 0.075 mm bond pads on package) could create unique scenarios in regards to solder joint response to the application of stresses. This is in addition to the increasing introduction of mixed mode (shear and tensile stresses) that are greatly accelerating creep and fatigue damage accumulation.

Conclusion

While the move to 0.3 mm pitch CSPs will be challenging, there is significant opportunity for leveraging the experiences of other portions of the supply chain. Examples include wafer-level bumping, which has been stencil printing 0.15mm pitch solder bumps for some time period, BGA substrates, which has been using 2 mil width and spacing on advanced packages, and 01005s, which have bond pads only 7 mil wide. Success will be ensured through adopting the information gained from these other processes, being aware of the potential gaps in this knowledge, and implementing industry best practices and physics of failure to understand margins and interconnect robustness.

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