

White Paper
Quality and Reliability Challenges for
Package-on-Package

By Craig Hillman and Randy Kong

Background

Semiconductor technology advances have been fulfilling Moore's law for many decades. However, with feature sizes approaching atomic dimensions, alternative technologies will be needed to meet the evolving performance, size and cost demands driven by applications from mobile to cloud computing. One example of such technologies is heterogeneous semiconductor packaging technology such as 3D packaging.

3D packaging technology, i.e., integration of devices in the vertical dimension, has been driven by the need for high die counts and mixed device integration within a given component footprint. Examples of 3D packaging in high volume applications include stacked die package, stacked package such as package-on-package (POP) and package in package (PIP). When it comes to integrating memory and logic devices, stacked die system-in-package (SiP) technology provides excellent performance and meets the size requirements. However, it does not provide the same cost, design and time-to-market flexibilities as package-on-package, i.e., POP technology.

The concept of POP occurred around the 1980's and was more recently introduced in ECTC 2003 by Nokia and Amkor. POP enables surface mount stacking of thin, fine pitch ball-grid array (BGA) packages that can connect logic and memory devices in a flexible manner. As a "killer" application for POP, almost all major smart phone manufacturers have adopted POP and the volume is projected to go from less than 200 million in 2007 to over 600 million units by 2011. POP has become the 3D package of choice for smart phone designs in meeting the feature, cost, size, weight, and time-to-market requirements.



POP typically consists of two laminate substrates corresponding to the top and bottom POP, which are interconnected together and to the printed circuit board (PCB). The top POP, which may contain multiple or stacked die, usually supports a BGA with larger ball size and thinner mold body. The bottom POP usually supports thin die and mold cap to accommodate top package. Special mold technology is required for the bottom POP to leave its perimeter free for interconnecting the top POP. Standard POP package sizes can range from 12 mm x12 mm to 15 mm x15 mm. Ball pitch dimensions can range from 0.4mm to 0.65mm with ball sizes varying from 0.35 to 0.45mm.

There are a number of driving factors for the popularity of POP. They include:

Market: With the exploding market for mobile phone, digital camera, MP3 player and other mobile computing applications, more functions and features are increasingly packaged into same or smaller form factors, which in turn drives the necessities of integrating, e.g., logic and memory devices in 3D packages

Process Flow: Logic and memory devices can be separately assembled and tested before the board level integration. The OEM has more flexibility in configuring logic and memory for desirable business flow/ownership. For example, the memory amount can be varied based on market conditions and product differentiation needs. Apple's iPhone has memory configurations between 8GB to 32GB, which can be changed at assembly point as a build option. This flexibility is enabled by POP stacking.

Total cost: In many cases, POP has the lowest TOTAL cost. Such cost can be related to test and test access, known-good die (KGD), business flow and ownership/liability concerns. For example, POP enables easy upgrade and multiple sourcing of memory components. The cost ownership is clearly defined. The bottom package belongs to the logic manufacturer, while the top package goes to the memory manufacturer, and board level connection is owned by the OEM.

Infrastructures and Standards: POP is supported by key logic and memory vendors, assembly equipment vendors, and package vendors as well as EMS/CM assembly houses. The bottom POP is designed to JEDEC standards, delivered by the logic supplier, and tested and guaranteed to the same performance and reliability levels as a standard component. The top POP is delivered by the memory supplier as a standard component. OEMs acquire the two components, stack them with a modified SMT flow maintaining a single reflow process, achieving the integration. Additionally, POP-specific JEDEC standards have been developed for the mechanical outline and integrity of the stack, electrical pin-outs, etc.

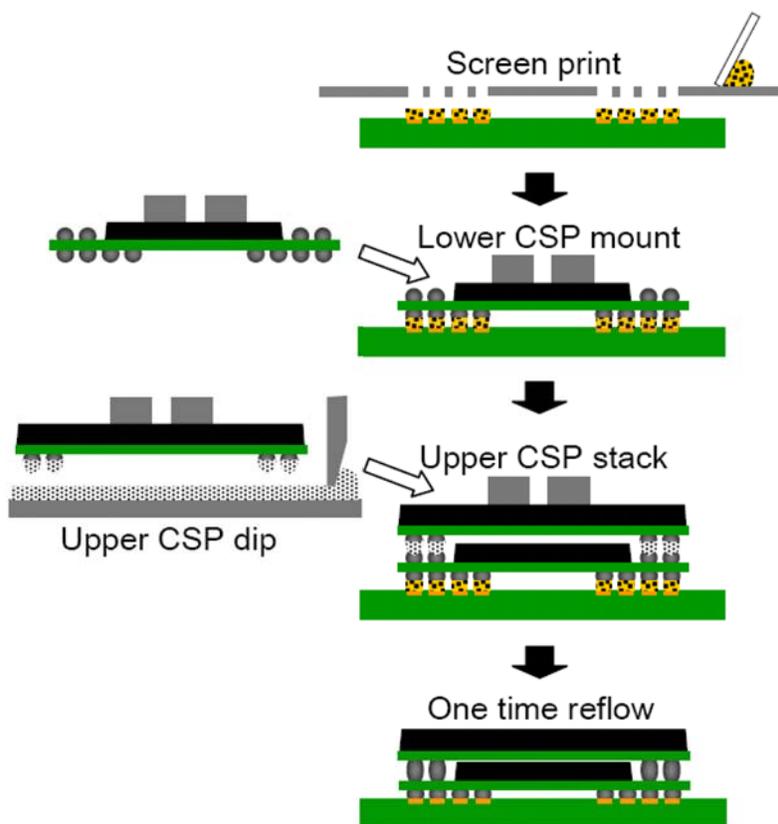
Future POP will likely see tiers in addition to memory and logic as more functionality, such as RF, analog, passive devices, are integrated. New generations of POP technology will also provide increased miniaturization, reliability and performance with optimum total cost structures.

Quality and Reliability Challenges

Despite the many advantages of POP, there are also inherent challenges with respect to board-level and system level quality and reliability. The quality/reliability related cost implications can be high as, e.g., a poor quality process would result in two or more BGA rework or scrap. In the following, we discuss manufacture related quality, and drop/thermal cycling related reliability challenges.

Manufacture Quality

In terms of manufacture quality, the bottom and the top packages are very thin. They must be capable of being placed on the printed circuit board (PCB) and reflowed to each other and to the board with acceptable yield. The assembly of POP is primarily carried out through one-pass reflow process. POP placement requirements and process technology are close to individual BGAs. Once screen print is done, the bottom component is placed before the top component is flux dipped and placed. In a typical assembly line, the only significant modification is adding a flux dip module for placement machines.



However, the stacked packages require greater attentions when it comes to quality than a single BGA package. For example, distortion in the bottom package will be reflected in the one above it as well, and there can be improper reflow profiles that lead to solder balls dislodging or migrating off the pad.

Of all defect types, the most dominant issue affecting POP assembly yield is the nature and extent of warpage that can occur during reflow of the logic and the memory POP. One study has found that more than 90% of the defects in POP assembly are due to package warpage, and the extent and degree of warpage is increasing as substrates become thinner. For conventional packages, the warpage direction is not critical as long as the co-planarity requirements are satisfied. For POP, the magnitude as well as the relative direction of the warpage can greatly impact the assembly yield. There can be warpage profile differences between the bottom and

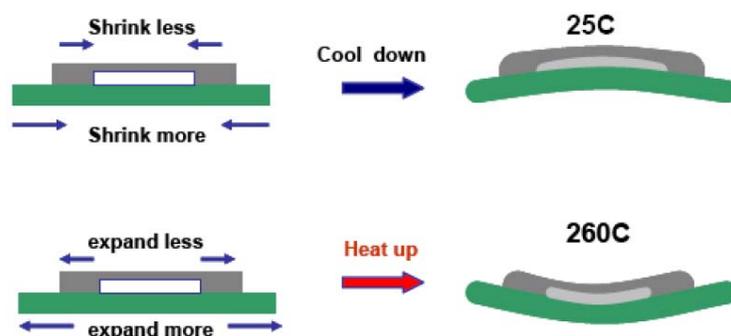
the top packages, especially when one is concave (smiling) and the other one is convex (crying). Large differences will result in opens or cold solder joints in the stacked interface, thus whole substrate warpage above solder liquidus temperature should be reduced for high yields. In addition to open joints, excessive component warpage also leads to solder ball bridging, solder slumping, head and pillow defects.

In terms of locations of potential open solder joints, it's more critical for POP at the top solder joints (memory to logic POP) than the solder joints between the logic POP and the PCB. This is true especially since in most cases, there is only flux applied to the memory package before it is reflowed. There may not be additional solder paste to fill the void if the two packages move apart during reflow due to warpage. The general warpage trend at room temperature is inconclusive. Some claim bottom is smiling (positive, concave) when the top is crying (negative, convex), while others claim the reverse is true. This trend should be partially dependent on if the CTE of mold compound is more or less than that of the substrate, thus materials selection is critical.

Controlling and matching warpage of top and bottom packages will be necessary to improve the quality in POP assembly. Warpage is always present and can vary from batch to batch, but top and bottom package warpage can be modulated to a different extent by choosing the right material set and construction. The factors contributing to warpage include:

- Materials: die attach, mold compound, substrate materials, solder ball alloy,
- Construction: laminate thickness, silicon-mold ratio, solder ball-size/pads
- Process: reflow profiles, time control, substrate pad finish

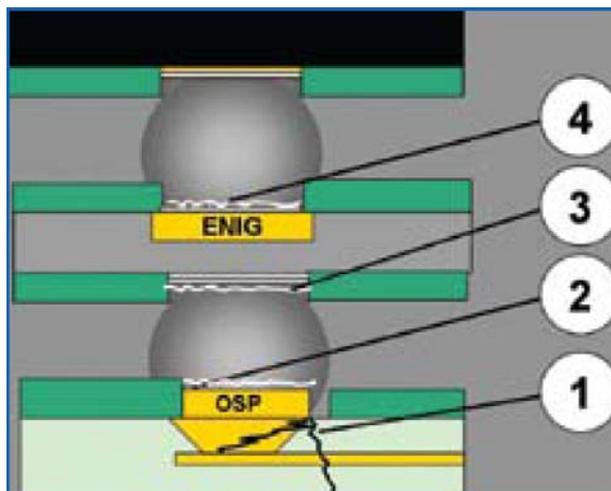
There are extensive interactions among material selection, package design and process parameters. The most critical materials properties are the mismatches in CTE between the substrate, mold compound, die and die attach. High Tg mold compounds are used to balance CTE mismatch between die and substrate, but the effect of mold compound becomes negligible at reflow temperatures. For die geometry, thinner die and smaller die tend to minimize warpage while larger/thicker die tend to drive "crying" warpage at room temperature. There have also been reflow profile studies that correlate preheat ramp rate, soak time, peak temperature and belt speed to the consequent sliding, bridging, tombstones and open joints.



Reliability and Durability

In addition to manufacture quality, POP package and board-level reliability are also more challenging than single package level. Full environmental, assembly and operational stresses should be carefully evaluated for potential risk exposures. Most focuses on POP have been on robustness against drop impact and thermal cycling fatigue stresses, though the usual full JEDEC qualification is a necessity, e.g., moisture/reflow sensitivity, thermal cycling, temperature-humidity bias, and shock and vibration. There is a POP-specific test such as modification to ambient thermal cycling. It is suggested that device generated heat may account for a “worst-case” scenario in real world operations. For this propose, JESD22-A105C has been proposed to couple thermal cycling with power cycling.

Mechanical shock or drop robustness is a critical requirement for mobile applications such as smart phones. According to JEDEC JESD11-B22, each board should be dropped 200 times at 1500G for 0.5ms. In most cases, the bottom POP package will be the first to fail. Different failure modes have been observed during drop testing such as cracking in the dielectric layer with the non-solder mask defined pads; cracks in the intermetallic layer between the solder bump and the PCB copper pad on the soldermask defined pads; cracks in the intermetallic layer between the solder bump and the component copper pad; and cracks at the IMC–nickel layer interface in example shown below.



In mobile applications, in addition to proper PCB layout which influences drop failure sites, underfill is often required to compensate for the shock impact. Underfill material provides stress relief in solder joints, it also protects the package from environmental hazards as a barrier for gases or vapor diffusion. Drop robustness can be dependent on materials and process parameters such as ball alloy type and underfill dispensing type, e.g., underfilling both the top and bottom packages is preferred over underfilling only the bottom package. Drop performance can be improved with a high modulus underfill with CTE values between 16ppm – 30ppm, as it reduces stress on interconnect due to substrate bending.

Since the introduction of copper as interconnection material in the late 1990's, low dielectric constant interlayer dielectric (i.e., low-k ILD) materials have been deployed in semiconductor chip process. Low-k ILD (and future ELK and ULK dielectrics) has inherently weak mechanical strength. Its incompatibility with a package can introduce delamination and/or die cracks. There needs to be both package-level (e.g., delamination) and board level (e.g., solder fatigue life) reliability evaluations against thermal cycling stresses. As mentioned earlier, there are concerns regarding the inadequacy of stand-alone ambient temperature cycling for POP, as defects can be sensitive to local temperature gradients. To overcome this limitation, JESD22-A105C has been proposed, which applies temperature excursions together with power cycling.

While underfill improves drop performance, POP thermal cycling fatigue reliability may not necessarily be improved with underfill. In principle, underfill can reduce shear stress on solder, as well as thermal expansion mismatch between die and substrate. However, actual test data indicates that improper selection and use of underfill may greatly reduce reliability under temperature cycling. In one case study where temperature is cycled between -40 and 125C, failure occurred just around 300 cycles with the underfill, whereas the package survived to 1000 cycles without the underfill. In thermal cycling, the PCB layout had little correlation to reliability test results, but the underfill selection can make a significant impact. Underfill with high Tg, low CTE and high filler provides much improved temperature cycling and drop performance.

Reliability of POP is highly dependent on the initial quality such as warpage issues discussed earlier. From the perspective of minimizing package warpage, one study found that the preferred POP configuration to be

- Thin die (50 micron vs. 100 micron)
- Thick mold on top package (0.45 vs. 0.35 or 0.25 mm)
- Thick substrate
- Top package (0.21 vs. 0.16 or 0.12 mm)
- Bottom package (0.36 vs. 0.26 or 0.21 mm)
- Large standoff on top package (0.45 vs. 0.40 or 0.35 mm)
- Medium standoff on bottom package (0.23 vs. 0.28 or 0.18 mm)

The problem is that except for the thin die, POP design is moving in the opposite directions of the above findings. Additionally, thick die, thin substrate, mold compound with low CTE can reduce stress in a low-k ILD under thermal cycling conditions. Thus, there is a trade-off between mold compound CTE, substrate and die thickness for low-k ILD stress and warpage.

Conclusion

In conclusion, POP is an exciting packaging technology that is finding wide spread applications in popular electronic devices. It maximizes design and logistics flexibility, reduces total lifecycle cost, and establishes clear business/engineering ownership. However, complex materials, design and process interactions need to be well understood in order to minimize quality and reliability risks discussed above. While assuring package and board-level reliability establish a good baseline, it is equally critical to examine system-level design, process and operation specifics. For example, JESD-22-A104C and JESD22-B111 provide an excellent reliability/durability evaluation against drop and thermal cycling stresses, it does not necessarily account for materials/process margins with respect to possible application-specific thermal exposures, environmental or operational.

As POP and other 3D packaging technology continues to progress, e.g., improvements in substrate size, ball pitch/size, package height reduction, the quality/reliability challenges will demand increased understanding and appropriate risk assessment/mitigations by all parties of interest, which would in turn require close collaborations among the device, packaging, and OEM companies.

Disclaimer

DfR represents that a reasonable effort has been made to ensure the accuracy and reliability of the information within this report. However, DfR Solutions makes no warranty, both express and implied, concerning the content of this report, including, but not limited to the existence of any latent or patent defects, merchantability, and/or fitness for a particular use. DfR will not be liable for loss of use, revenue, profit, or any special, incidental, or consequential damages arising out of, connected with, or resulting from, the information presented within this report.