Temperature Cycling of Coreless Ball Grid Arrays

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Abstract

There are countless challenges in making mobile electronics more reliable, including the thin form factor of cellphones and tablets that is forcing mobile computing packages to get thinner. Using coreless ball grid array (BGA) substrates decreases the overall height of the component, but it presents manufacturing challenges and potential reliability concerns when subjected to thermal cycling. This study presents results from tests performed on a coreless 25 mm by 27 mm BGA package with a relatively large die and stiffener ring that survived over 8,000 temperature cycles without failure. In order to investigate the reason behind this robust performance the coefficient of thermal expansion (CTE) of the part was measured using digital image correlation (DIC). The DIC results indicated that this combination of die size, package size, and stiffener ring reduces the CTE mismatch between the BGA package and printed circuit board (PCB).

I. INTRODUCTION

Standard flip chip substrates are constructed with a 200-800 micron thick core laminate layer with build-up layers on either side. A coreless substrate does not have the core laminate and is only comprised of the build-up layers. A comparison of a standard and coreless substrate is shown in Figure 1, where the coreless substrate lacks the thick glass laminate layer present in the standard substrate.

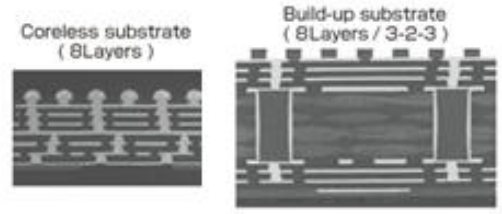

Figure 1: Coreless substrate (left) and standard substrate[1]

The use of coreless substrates for BGA packages involves overcoming manufacturing and reliability challenges. They are typically more prone to warpage during assembly than a standard substrate and coreless BGAs have a higher CTE, which may lead to decreased reliability during temperature cycling.

In this study, a large BGA package with a large die was subjected to 8,000 temperature cycles without any failures. The robust performance of this part during temperature cycling was unexpected because of the large die dimensions. Therefore, additional experiments were conducted to better understand the fatigue behavior of the package.

II. EXPERIMENTAL PROCEDURE

The BGA package studied is shown in Figure 2. The die can be seen on the top, the substrate is below, and the stiffener ring is located along the perimeter of the substrate. The package is 25 mm by 27 mm by 1.54 mm (total thickness), and the die is 13.8 mm by 16.5 mm by 0.75 mm.

[1] http://www.toppan.co.jp/material/english/semicon/package/fc-bga/coreres/

Figure 2: Coreless BGA studied

Samples

11 samples of 2 different configurations of the device were studied.

1. 5 samples – no edge bonding
2. 6 samples – adhesive edge bonded

Monitoring

Each device featured multiple daisy chains to allow for monitoring and isolation of failed solder joints within the ball grid array, as shown in Figure 3. During testing the daisy chains for each device were connected in serial resulting in a single resistance value for combined chains. This was monitored using an Agilent 34970A data logger populated with 34908A singe ended multiplexer cards. Resistances were recorded in 1 minute intervals.

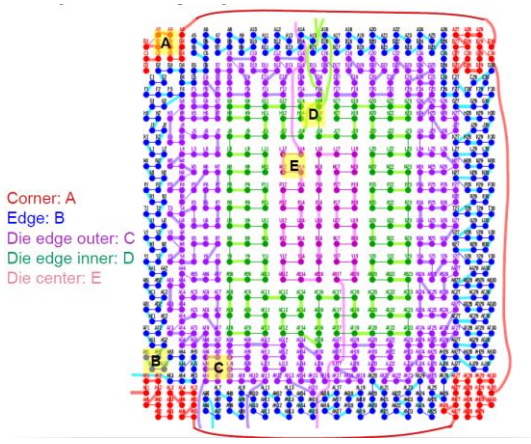

Figure 3: Daisy chain locations

An example of the printed circuit board assembly (PCBA) sample subjected to thermal cycling is shown in Figure 4.

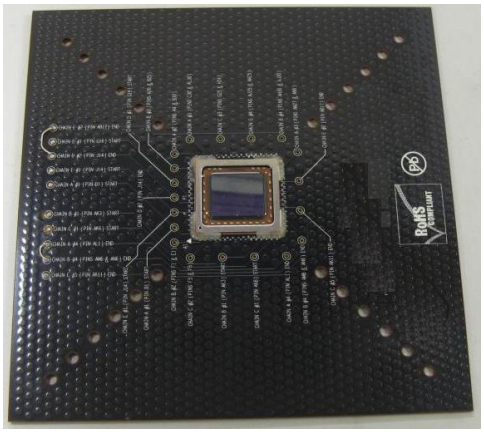

Figure 4: Test PCBA

Environment

The test boards were subjected to 8,027 temperature cycles in a SUN Electronics thermal chambers with liquid nitrogen cooling. The boards were thermal cycled from -40°C to 85°C. The dwell time at the minimum and maximum temperature was 23 minutes and the ramp rates were maintained at 17°C/min.

After the initial 8,027 thermal cycles the samples were subjected to an additional 3,840 cycles using an Espec TCC-150 thermal chamber under the same thermal profile as detailed previously.

Digital Image Correlation

After testing, a sample was subjected to (differential) digital image correlation and tracking (DIC/DDIT), an optical method that employs tracking and image registration techniques for accurate 2D and 3D measurements of changes in sample deformation. DIC was conducted at the Optomechanics and Physical Reliability Lab at the State University of New York at Binghamton.

First, the sample was coated with a stochastic pattern using white paint to

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allow for tracking of the sample movement as shown in Figure 5. Then the deformation over a range of temperatures was recorded and used to calculate the effective CTE of the top (die side) and bottom (solder side) of the package.

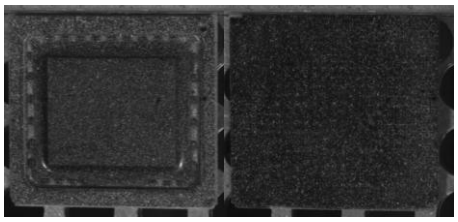

Figure 5: Front and back of BGA with white stochastic pattern

III. RESULTS and DISCUSSIONS

The 11 devices were subjected to a total of 11,867 thermal cycles in order to induce failure of all the devices.

Cycles to Failure

A 2 parameter Weibull plot of the failures for each sample type are shown in Figure 6. The Weibull parameters are:

Samples with adhesive edge bonding:
Shape parameter, β = 8.9575
Characteristic Life η = 10,924 cycles

Samples without edge bonding:
Shape parameter, β = 15.369
Characteristic Life η = 9,777 cycles

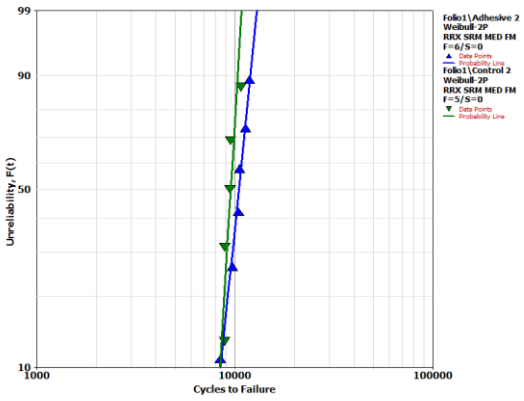

Figure 6: Cycles to failure for samples with (green) and without (blue) edge bonding

The results indicate that the presence or absence of edge bonding does not impact the failure behavior of the tested devices. This is evidenced by comparable β and η values and can be seen visually in Figure 6, where the slope and times to failure of the with adhesive edge bonding and without edge bonding samples are comparable.

Therefore, the data was combined into one population and plotted using a 2-parameter Weibull plot as shown in Figure 7.

The overall Weibull parameters are:

Shape parameter, β = 10.8304
Characteristic life η = 10,425 cycles

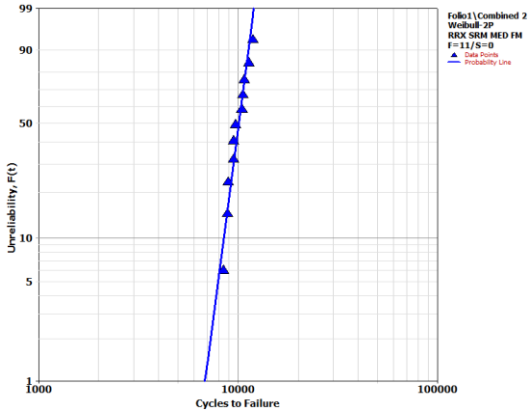

Figure 7: Cycles to failure for both samples combined into one Weibull

To better understand the demonstrated robustness of the coreless BGA under thermal cycling a part was removed from the printed circuit board (PCB) and subjected to DIC to determine its CTE behavior.

Images of the deformation in the X direction at 70˚C and 110˚C are shown in Figure 8 and Figure 9.

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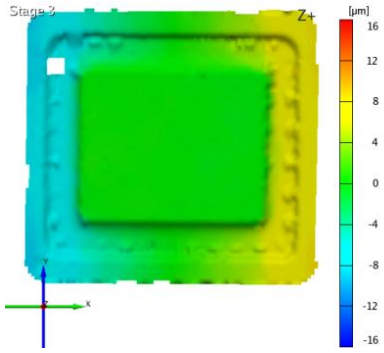

Figure 8: Top X deformation at 70˚C

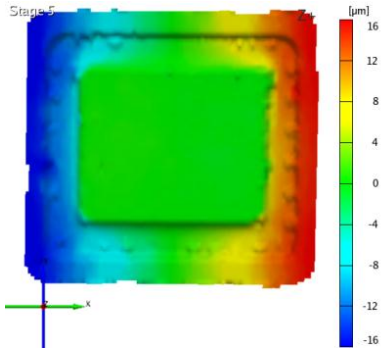

Figure 9: Top X deformation at 110˚C

Images of the deformation in the Y direction at 70 ˚C and 110˚C are shown in Figure 10 and Figure 11.

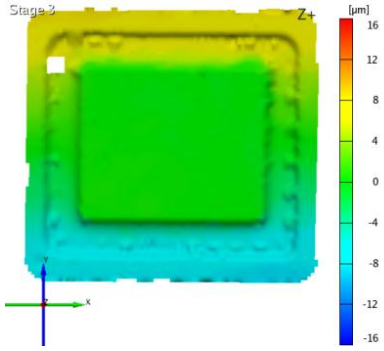

Figure 10: Top Y deformation at 70˚C

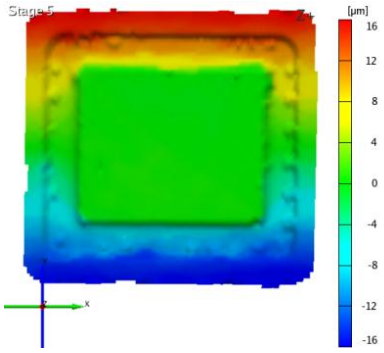

Figure 11: Top Y deformation at 110˚C

These images indicate the top of the deformation on the top of the package is driven by the presence of the die. The stiff die experiences little to no deformation as evidenced by the green color in all the images. The majority of the deformation occurs in the substrate between the die edge and the substrate edge. These results support the typical BGA device observations that solder balls at the edge of the die typically fail first.

Images of the deformation on the bottom of the package in the X direction at 70 and 110˚C are shown in Figure 12 and Figure 13.

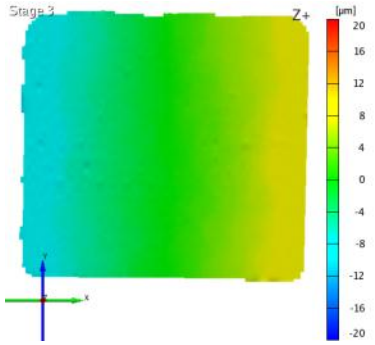

Figure 12: Bottom X deformation at 70˚C

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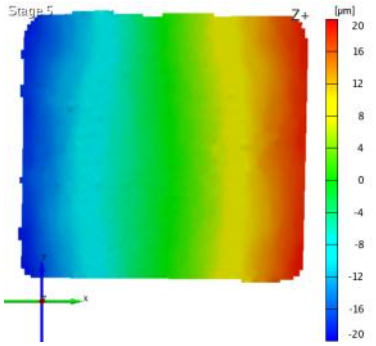

Figure 13: Bottom X deformation at 110˚C

Images of the deformation on the bottom of the package in the Y direction at 70 ˚C and 110˚C are shown in Figure 14 and Figure 15.

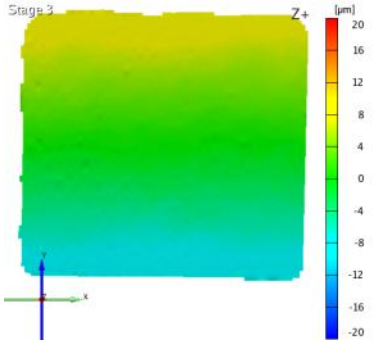

Figure 14: Bottom Y deformation at 70˚C

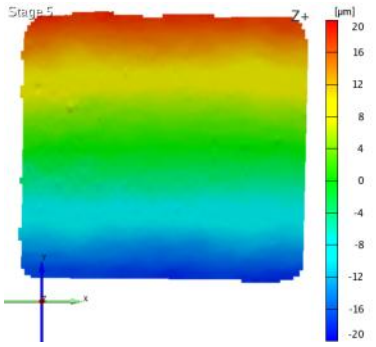

Figure 15: Bottom Y deformation at 110˚C

Unlike the top side, the results show that the deformation of the bottom of the package is not impacted by presence of the stiff die. Rather, the bottom side has a relatively uniform deformation across both the x and y axes.

The computed CTE values from the deformation plots are summarized in Table 1. The CTE values from the bottom side of the package match to that of PCBs, which are typically 15-17 ppm/ ˚C. Therefore, the stresses on the solder balls caused by CTE mismatch between the coreless BGA package and PCB are minimized. The CTE values from the top side of the package are slightly lower because they are driven by the stiffness of the die.

Table 1: Coefficient of thermal expansions

Side	X ppm/˚C	Y ppm/˚C
Top	13.5	15
Bottom	16	17.2

The CTE match between the bottom of the coreless BGA package and the PCB resulted in the samples surviving more than 8,000 thermal cycles without failure. A standard substrate BGA package does not last as long because the die stiffness has a greater impact on the bottom side CTE, creating larger mismatch and more thermally induced stresses within the solder joint.

While the coreless BGA was robust under thermal cycling, one of the main issues with using coreless substrates is their propensity for warping (z-axis deformation) during assembly. The package studied featured a stiffener ring to prevent warpage during reflow. The effectiveness of the stiffener ring was measured over a limited temperature range (up to 110˚C).

The warpage at 70˚C and 110˚C are shown in Figure 16 and Figure 17.

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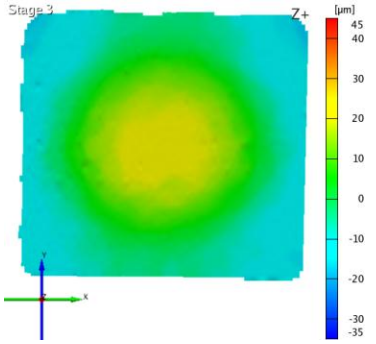

Figure 16: Warpage at 70˚C

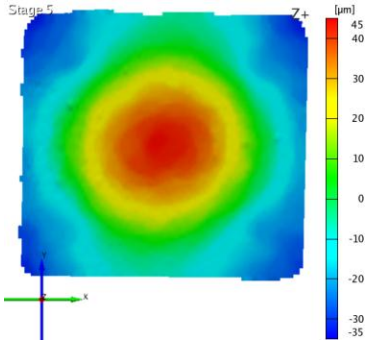

Figure 17: Warpage at 110˚C

Typically the warpage of the package shows an inflection point close to the glass transition temperature (T_g) of the 1st level underfill or overmolding. An example of this was shown in a study conducted by Garrett, as shown in Figure 18. A comparison of the warpages for the tested BGA samples with different molding materials indicated that around the T_g of each material, an inflection point in warpage behavior exists. The warpage behaviors seen in Figure 16 and Figure 17 are comparable, indicating that 110˚C is below the T_g of the molding compound used in the tested coreless BGA.

It is possible that the studied coreless BGA will experience a warpage inflection point during reflow, however, the DIC testing presented here focused on temperatures the package would see during operation and not during manufacturing. The warpage behavior can be predicted based on the study by Garrett.

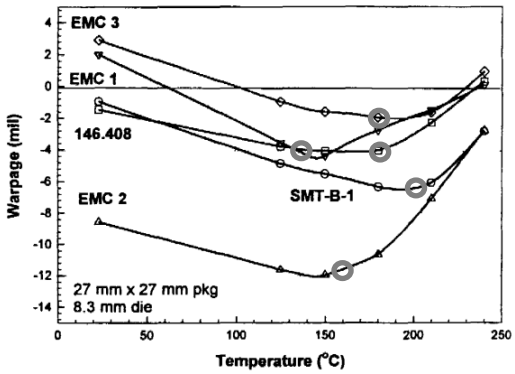

Figure 18: Warpage of molding compounds; grey circles indicate approximate T_g [1]

As shown in Figure 18 the amount of warpage measured by Garrett was between 2 and 4 mils (50 to 100 µm) from room temperature to 110˚C. As shown in Figure 17, the warpage measured for the part tested in this study was about 80 µm which is within this range. One would expect the warpage behavior to show the same behavior (decrease in warpage) as the temperatures increase beyond the T_g of the underfill of the part.

IV. CONCLUSIONS

The accelerated life cycle testing of a coreless BGA package has been reported. This particular coreless BGA package was very robust with regards to temperature cycling. The source of this robustness was investigated using digital image correlation and was shown to be due to the coefficient of thermal expansion of the package bottom being very well matched to that of the printed circuit board. An additional investigation also showed that the warpage of the package over the limited temperature range of standard overmolded BGA parts did not include an inflection point.

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References

1. “Elevated Temperature Measurements of Warpage of BGA Packages”, David W. Garrett, Amoco Electronic Materials, Plaskon Division, Alpharetta, Georgia

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