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White Paper

Temperature Dependence of Electrical Overstress

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1. What is Electrical Overstress (EOS)?

Electrical overstress is typically defined as an over voltage or over current event with a duration exceeding 100 to 1000 nanoseconds and nominal durations of 1 millisecond that occurs while the device is in operation. It is typically differentiated from electrostatic discharge (ESD), which has a shorter duration (1 nanosecond to 1 microsecond) and is primarily an issue during non-operational manufacturing and handling.[1, 2] Events that can lead to EOS damage include voltage spikes, lightning strikes and any temporary and unexpected connections to power or ground.

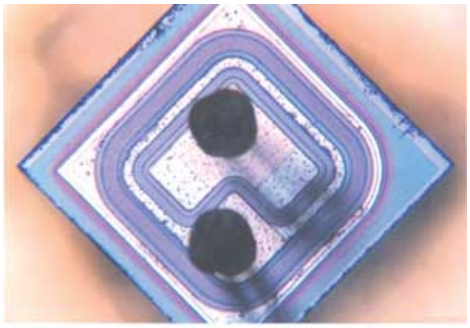
2. How does EOS cause failure?

EOS events typically induce failures either due to dielectric breakdown (excessive voltage) or thermal runaway from Joule heating (excessive current). Examples are shown in Figure 1. In addition, some research has indicated that current-induced and field-induced degradation mechanisms complement one another and both are required to fully explain breakdown behavior over a wide range temperature.[3,4,5]

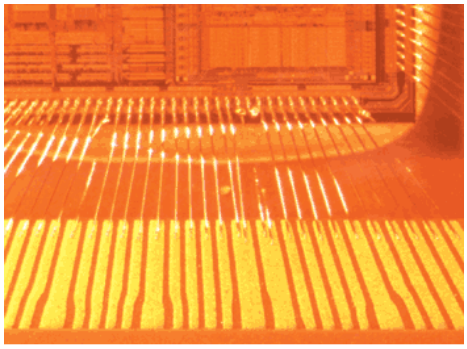
These failures can be further defined into primarily four different failure mechanisms

- Gate oxide breakdown
- Thermal runaway (junction damage or junction breakdown)
- Thermal runaway (conductor or metallization fusing)
- Latchup

To understand the influence of temperature on the probability of EOS, the temperature dependence of dielectric breakdown and joule heating must be reviewed and discussed.



1. This bipolar junction transistor was damaged by thermal overstress caused by EOS. Note the hot spots in the base and emitter regions.



2. EOS-induced thermal overstress can even melt the wirebonds between a chip and its package.

Figure 1: Photographic examples of field-effect (left) and current driven (right) damage due to EOS events (http://www.elecdesign.com/Articles/Index.cfm?AD=1&ArticleID=4127)

[1] Failure Mechanisms in Semiconductor Devices, 2nd edition, E. A. Amerasekera and F. N. Najm, 1997, John Wiley, London, England
[2] CHARACTERIZATION, MODELING, AND DESIGN OF ESD PROTECTION CIRCUITS By STEPHEN G. BEEBE, March 1998
[3] C. Hu and Q. Lu, "A unified gate oxide reliability model," in *Int. Reliabil. Phys. Proc.*. Piscataway, NJ: IEEE, 1999, pp. 47–51.
[4] K. Cheung, "A physics-based, unified gate-oxide breakdown model," *IEDM Tech. Dig.*, 1999, pp. 719–22
[5] J. McPherson, R. Khamankar, and A. Shanware, "Complementary model for intrinsic time-dependent dielectric breakdown in SiO dielectrics," *J. Appl. Phys.*, vol. 88, no. 9, pp. 5351–5359, 2000.

2.1 Dielectric Breakdown

Dielectric breakdown, also known as avalanche breakdown or punch-through, occurs when the applied electric field exceeds the dielectric strength of the gate oxide. In reviewing the literature, it can be difficult to differentiate between EOS and TDDB induced by pulses of short time duration. As seen in Figure 2, Smith believes that the mechanisms that initiate breakdown in the regime of nano or microseconds are intrinsic in nature, while longer duration exposure results in a thermally driven breakdown behavior.

Based on the previous definition of EOS, because Smith[6] confirms that breakdown events milliseconds and longer are fundamentally driven by the same mechanism, and because a number of publications on TDDB extrapolate behavior down to the millisecond and microsecond regime (see Figure 3), the effect of temperature on TDDB behavior will be assumed to invoke a similar behavior to EOS sensitivity.

The TDDB process takes place in two stages. In the first stage, the oxide is damaged by the localized hole and bulk electron trapping within it and at its interfaces. The second stage is reached when the increasing density of traps within the oxide form a percolation (conduction) path through the oxide. This short circuit between the substrate and gate electrode results in oxide failure.

When discussing TDDB, it is important to differentiate between thick oxides (older technology) and thin or ultrathin oxides (newer technology). For thick oxides, time to failure is electric field dependent (E). There has been much debate in the industry over the form of this dependency, with both an anode hole injection (1/E) and thermo-chemical (E) model proposed. Review of the literature seems to suggest a preference for the thermo-chemical model. This model proposes that defect generation is a field-driven process and the current flowing through the oxide plays a secondary role at most[7]. The interaction of the applied electric field with the dipole moments associated with oxygen vacancies leads to a conduction sub-band formation and to severe Joule heating at the stage of oxide breakdown.

The temperature dependence of the thermo-chemical model is described through classic Arrhenius behavior

$$\ln(TF) \propto \frac{\Delta H_o}{k_b T} - \gamma E_{ox}$$

where ΔH_0 is the activation energy, E_{ox} is the electric field in the oxide, k_b is Boltzmann's constant, and γ is the field acceleration parameter[8]. The activation energy is typically given as approximately 0.8 to 0.9 eV[9].

For thinner oxides, the absolute voltage is the greater driver than electric field. In addition, it has been demonstrated that temperature dependence can no longer be described as Arrhenius, as seen Figure 4. For newer technology devices with thinner oxides, Wu et. al. have provided an alternative temperature-dependence model

[6] General EOS/ESD Equation, Smith, J.S., Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1997, Date: 23-25 Sep 1997, Pages: 59 - 67

[7] McPherson JW, Mogul HC. Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO2 thin films. J Appl Phys 1998;84:1513–23.

[8] Comparison of E and 1/E TDDB Model for SiO2 under Long-Term/Low-Field Test Conditions
J. W. McPherson, V. Reddy, K. Banerjee, and H. Le, Technical Digest IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 6-9, 1998, pp. 171-174

[9] Sanyo and Semiconfareast

$$T_{BD} = T_{BD0}(V) \exp\left(\frac{a(V)}{T} + \frac{b(V)}{T^2}\right),$$ [10]

where T_{BD} is time to failure and T is temperature in Kelvin. This equation is plotted in Figure 3 out to microseconds, a time span equivalent to EOS events.

As a general role of thumb, the dielectric breakdown strength of oxide film is generally said to be 5 to 15 x 10^6 V/cm depending on thickness[11]. For this reason, devices with a thin oxide film, e.g. 1 nm, experience dielectric breakdown at approximately 1 V.

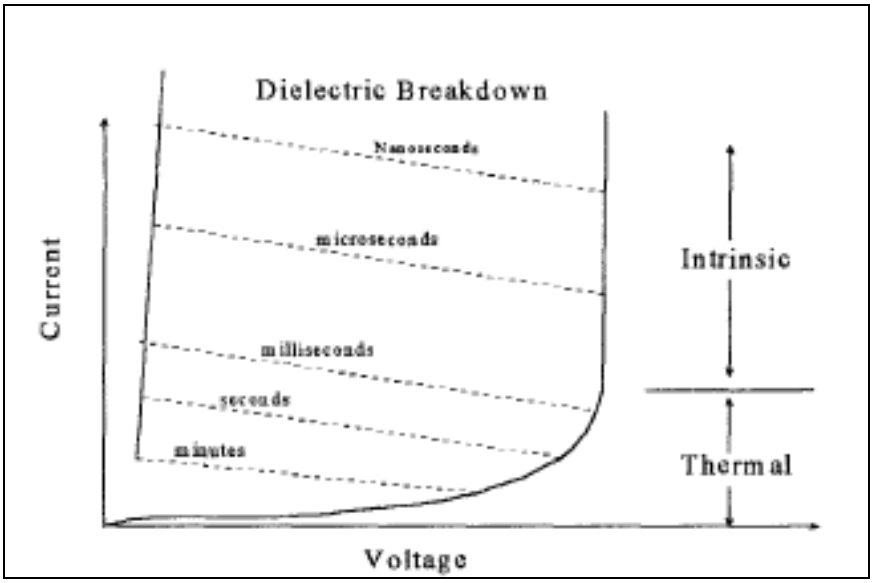


Figure 2: Transition between thermal and intrinsic breakdown in dielectrics[12]

[10] IBM Research Journal, Volume 46, Numbers 2/3, 2002, CMOS scaling beyond the 100-nm node with silicon-dioxide-based gate dielectrics, E. Y. Wu, E. J. Nowak, A. Vayshenker, W. L. Lai, and D. L. Harmon
[11] http://www.semiconductorglossary.com/default.asp?searchterm=silicon+dioxide%2C+SiO2
[12] General EOS/ESD Equation, Smith, J.S., Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1997, Date: 23-25 Sep 1997, Pages: 59 - 67

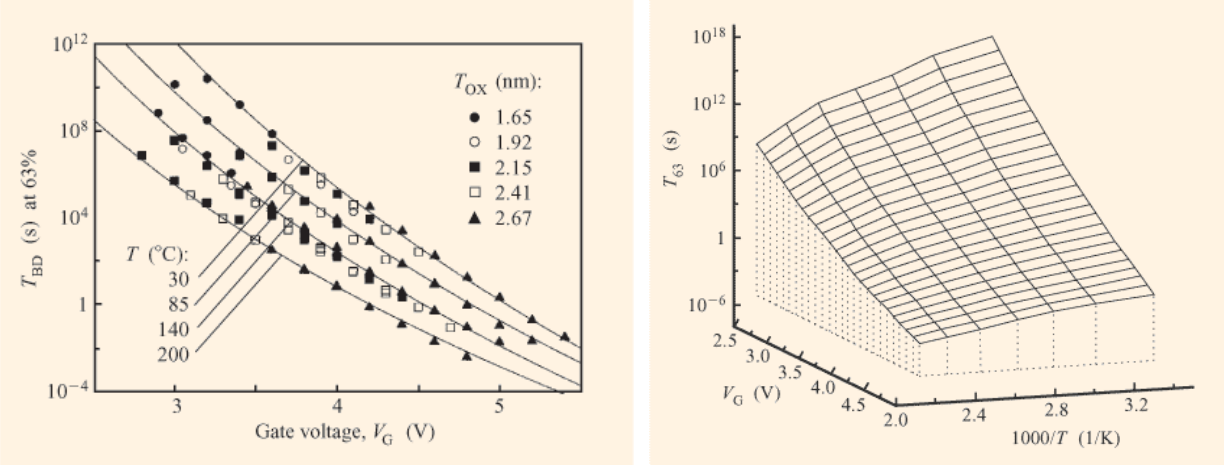


Figure 3: Time to breakdown as a function of voltage and temperature[13]

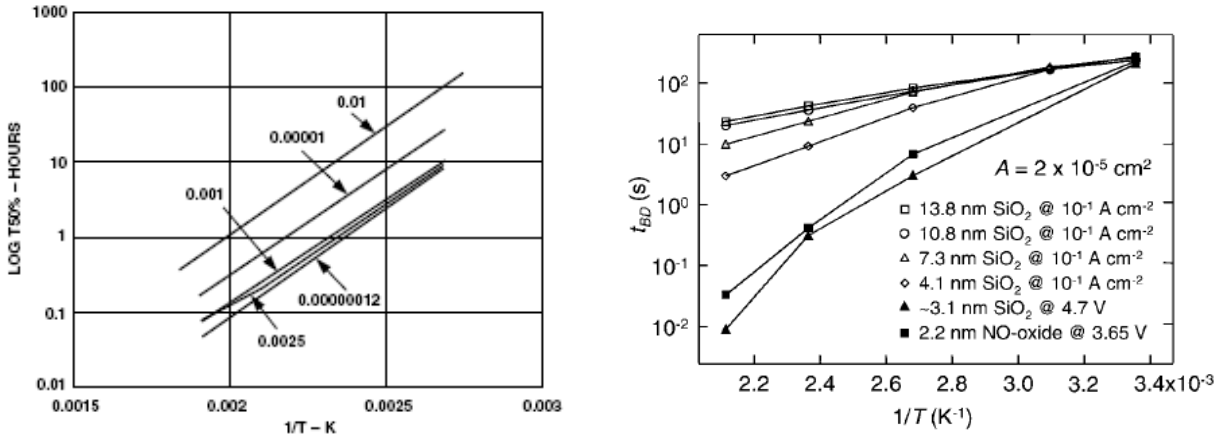


Figure 4: Thicker oxides displaying Arrhenius behavior (left), while thinner oxides display non-Arrhenius behavior (right)[14],[15]

[13] IBM Research Journal, Volume 46, Numbers 2/3, 2002, CMOS scaling beyond the 100-nm node with silicon-dioxide-based gate dielectrics, by E. Y. Wu, E. J. Nowak, A. Vayshenker, W. L. Lai, and D. L. Harmon

[14] Semicond. Sci. Technol. 15 (2000) 436–444. Reliability: a possible showstopper for oxide thickness scaling?, Robin Degraeve, Ben Kaczer and Guido Groeseneken

[15] ADI Reliability Handbook, www.analog.com/UploadedFiles/Associated_Docs/ 51998357609450215 3Fab_Reliability.pdf

3. Junction Breakdown (Thermal Runaway)

Junction breakdown occurs when excessive current flow raises the junction temperature enough to destroy it with heat. The specific behavior can be understood by examining the images in Figure 5. When energy is dumped into a silicon device during an EOS event, the heating of the silicon is uneven. This can cause a small area of the junction to heat up, causing its resistivity to drop sharply. Once heating occurs, the small area becomes thermally isolated from its surroundings because the thermal conductivity of the silicon decreases. This effect is a positive feedback mechanism resulting in damage to the device junction.

Since junction energy consumption differs for a forward or a reverse discharge, different breakdown voltages result. Electrical discharge in a forward direction does not concentrate energy in localized areas as a reverse discharge does. Consequently the breakdown voltage for a forward discharge is higher than that for a reverse discharge. In addition, this mechanism tends to be more prevalent in bipolar devices.

Junction breakdown can also occur due to tunneling or avalanche mechanisms. However, based upon review of the literature, thermal instability seems to be the primary failure mechanism at the junction during an EOS event. The Wunsch & Bell model, with its thermal diffusion formula, is commonly used to describe this failure mechanism. In the model, the junction breakdown phenomenon is determined from the pulse width and power density that are applied to the device[16].

$$\frac{P_f}{A} = \sqrt{\pi \kappa \rho C_p}\left[T_m - T_i\right] t^{-1/2}$$

where P_f is the power-to-failure in W, A is the area in cm^2, C_P is heat capacity in J/gcm-K and ρ is density in g/cm^3. κ is thermal conductivity in W/cm-K, t is the width of a square pulse, T_m is melting temperature of the junction, and T_i is the initial temperature.

Via this relationship, the direct effect of ambient temperature could be seen as minimal as Ti, between 335 and 400K, is much smaller that Tm at approximately 1700K. However, Mars[17] determined that the more appropriate peak temperature was not the melting temperature, but the intrinsic temperature[18] of the silicon, which is typically in the range of 180 “C to 300 “C. With this modification of the Wunsch and Bell model, it can be seen that an increase in ambient temperature from 60C to 85C could have a measurable effect on the frequency of EOS events.

Thermal conductivity, as seen in Figure 5, decreases with ambient temperature, which can result in a greater temperature rise for a given energy input. In addition, the power that is being introduced into the PN junction is influenced by the electrical resistivity. The relationship between resistivity and temperature for a pure semiconductor is

$$\rho \propto T^{-3/2} e^{E_G/kT}$$

[16] www.semicon.toshiba.co.jp/ eng/prd/common/data/pdf/relia_dis02.pdf
[17] P. Mars, “Thermal Analysis of P-N Junction Second Breakdown Initiation” Intemational Joumal of Electronics, 1972, Vol. 32, No. 1,pp. 39-47.
[18] Intrinsic temperature is when the concentration of thermally generated carriers exceeds the concentration of carriers generated by doping. When these thermally generated carriers swamp the number of doping atoms, free carriers will exist. If an electric field is present this will form a current.

where E_G is the band gap. As seen in Figure 5, resistivity of doped can be highly sensitive to temperature. Doped silicon initially exhibits a positive temperature coefficient, but reaches a peak value of resistivity and thereafter exhibit a large negative temperature coefficient. The rapid decrease in resistivity following the peak will result in increased current density in any region subjected to a constant potential difference.

The subsequent Joule heating of the material can cause the temperature to rise, further decreasing the resistivity. This cycle continues, resulting in a thermal runaway that eventually melts the silicon with the hot spot when its temperature exceeds the melting point of silicon.

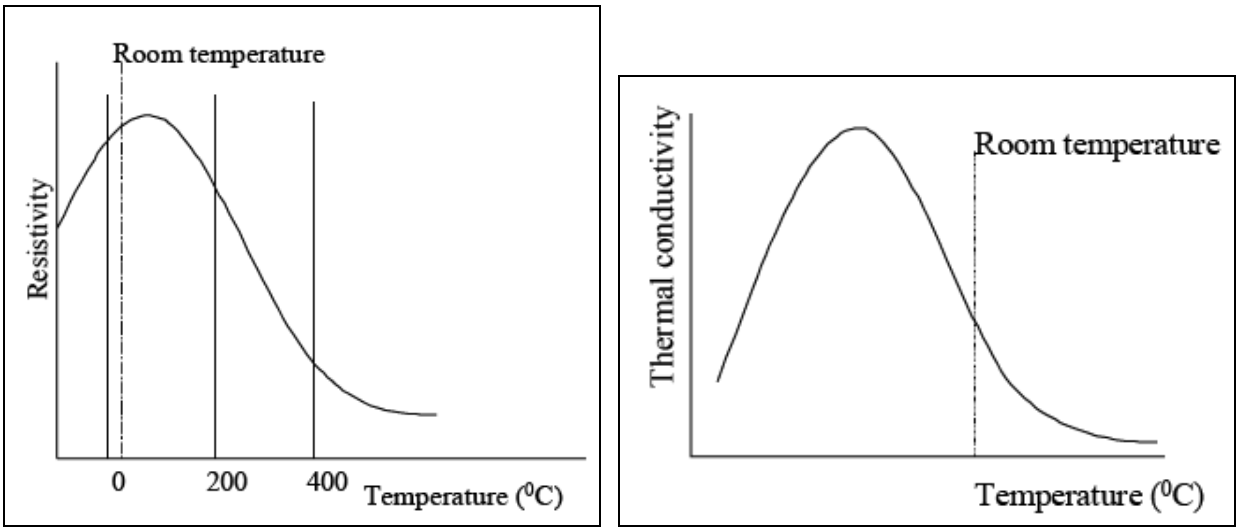


Figure 5: Change in resistivity and thermal conductivity of doped silicon as a function of temperature

4. Conductor / Metallization Fusing

This failure mechanism is driven by overheating of the conductor being used to carry current within the device, typically either bond wires of metallization. As conductors heat up, their electrical resistance increases as a function of

$$R = R_0 \left[1 + \alpha(T - T_0)\right]$$

with the temperature coefficient of resistance, α, ranging from 3.9 x 10^{-3} / °C for copper and aluminum to 3.4 x 10^{-3} / °C for gold. Typically, this increase in resistance tends to prevent thermal runaway, but the resistance of the conductor is minimal in comparison to the rest of the device, so this change in electrical resistance simply increases the Joule heating effect (I^2R) without resulting in a drop in current.

The actual current density necessary to induce metallization fusing is given as

$$J = \sqrt{\frac{c_v (T_m - T_0)}{\rho \tau}}$$

where heat capacity, □ is the bulk resistivity, □ is the duration of the EOS event, T_m is the melting temperature of the metal and T_0 is the initial temperature[19]. Given the nominal change in electrical resistance over the given temperature range and the relatively high melting temperatures for copper, aluminum, and gold, increases in ambient temperatures are not expected to play a significant role in this failure mechanism.

5. Conclusion

The influence of EOS sensitivity as a function of temperature for a given system is difficult to predict given the different failure mechanisms that can be induced and the different dependence on temperature for each one of these mechanisms. These dependencies range from minimal for metallization fusing to strong dependencies for junction and oxide breakdowns.

[19] General EOS/ESD Equation, Smith, J.S., Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1997, Date: 23-25 Sep 1997, Pages: 59 - 67

Additional Data and Information

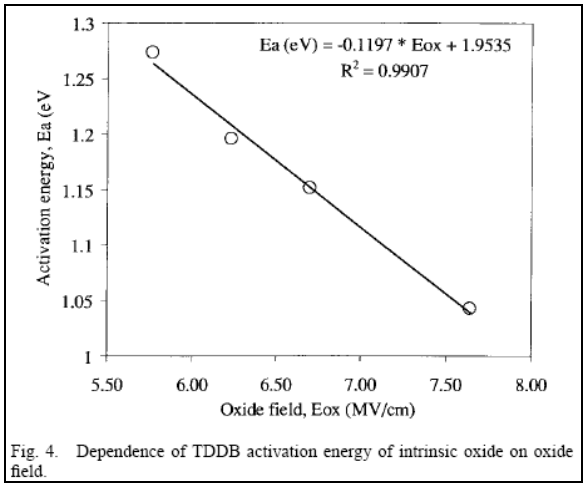


Fig. 4. Dependence of TDDB activation energy of intrinsic oxide on oxide field.

IEEE ELECTRON DEVICE LETTERS, VOL. 20, NO. 8, AUGUST 1999, Field and Temperature Dependence of TDDB of Ultrathin Gate Oxide, Abdullah Yassine, H. E. Nariman, and Kola Olasupo

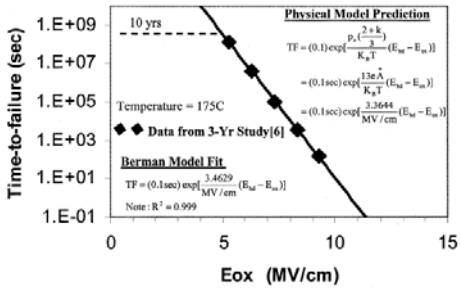


Fig. 10. Comparison of the Berman model and physical/thermochemical model when applied to longer-term/lower-field TDDB data. TDDB data collected for three years [6]. Data suggests that TF data can be extraplated successfully from E_{bd} data. Here, breakdown was defined as the field at which failure occurs in 100 ms.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 8, AUGUST 2003 1771, Trends in the Ultimate Breakdown Strength of High Dielectric-Constant Materials, Joe W. McPherson, Jinyoung Kim, Ajit Shanware, Homi Mogul, and John Rodriguez

Thin Gate-Oxide Reliability – the Current Status

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Another factor that makes the reliability of ultra thin oxide a serious problem is temperature. Due to the high power dissipation level of high performance IC, the finished products are expected to be operating at elevated temperature. thus the reliability specification is not for room temperature but for 125C.

It is well known that the gate-oxide breakdown lifetime is shorter at higher stress temperature [12-15]. For a long time, the temperature (T) dependence of oxide lifetime was well described by an activated process. In other words, log(t_{BD}) vs 1/T is a straight line. Recently, however, it is reported that the temperature dependence of log(t_{BD}) is non-Arrhenius [16-18]. The temperature acceleration factor (the slope of log(t_{BD}) vs 1/T) is observed to be larger at higher temperature. This is certainly not good news for running the IC at higher temperature.

A even more troublesome trend in temperature acceleration of t_{BD} is that the acceleration factor increases with decreasing oxide thickness and the trend is nonlinear. In other words, the increase in acceleration is itself accelerating with decreasing oxide thickness. Going from room temperature to 125C, while the lifetime of 100Å oxide decreases by a factor of ~3, the lifetime of 22Å oxide decreases by a factor of 100 [17]. Thus, for accurate projection of thin gate-oxide reliability, the temperature effect must be taken into account.