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Think twice about that low Tg underfill

Craig Hillman

Reaching way back, like several months ago, the first part of my column on underfill discussed the fascinating history of flip chip devices and underfill, its recent successes, and the transition to underfills with a lower glass transition temperature to resolve drop issues and brittle low-K dielectric.

Underfill with low glass transition temperature (Tg). Theoretically, it solved everything. Good enough to prevent white bump failures. Good enough to prevent failures under temperature cycling. Almost too good to be true.

Now, to start, we should probably define exactly what low Tg underfill is (the what). From my perspective, low Tg underfill is defined as a glass-filled epoxy with a glass transition temperature below the maximum use temperature of the device. Note (actually, a very important note): Not below the maximum storage temperature or the maximum test temperature or the maximum junction temperature. Only when it is below the maximum use temperature.

The introduction of low-Tg underfill into the marketplace was followed by rapid acceptance by most of the major manufacturers of flip chip ball grid arrays (FCBGAs). Central processing units (CPUs), graphic processing units (GPUs), and field programmable gate arrays (FPGAs) fabricated with low-K dielectric (the transition was between 45 nm and 90 nm process node depending on the technology) quickly integrated the new material set into their packaging construction. White bump issues faded to the background, and the new material passed all JESD22-A104 temperature cycling tests with flying colors. The low Tg underfill was so good it became literally impossible to get flip chip bumps to fail under temperature cycling. It was literally bullet-proof! And that should have been the first indication that something was very wrong.

The problems first became apparent in between 2005 and 2007. Numerous vendors started reporting extremely high failure rates on some products, with some indications of either a 60% failure rate or repair rates exceeding 100% (the average unit came back for repair more than once). Initially, the failures were difficult to diagnosis, and some organizations struggled with identifying root-cause for several months. The reason for this dilemma was a combination of the nature of the failure mode, the architecture of flip chip packaging, and the random location of the failure site.

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What was happening, as we now know, was the solder bumps under the flip chip device were failing due to thermomechanical fatigue. However, due to the array nature of flip chips (this is a problem with ball grid array packaging as well), the nearest neighbors will force the crack closed. This results in a failure mode that is intermittent (sometimes there, sometimes not). This intermittency was so well known that some users of a particular gaming system that was experiencing flip chip cracking would wrap the unit in towels and force it to overheat. This would increase the intermittency duration long enough for them to resell the gaming system back to retailers.

The other major challenge for identifying the root-cause of low Tg underfill failures was the random location of the failure site. Typically, in most electronic applications, thermo-mechanical fatigue of solder joints is due to shear stresses, which peak at the maximum distance from the neutral point (i.e., the corner). However, low Tg underfill failures, for reasons I will explain in the next paragraph, are driven by tensile stresses. And failures due to tensile stresses can literally occur in any flip chip solder bump. When the flip chip device has 1000 bumps, it can be like trying to find a needle in a haystack.

So, you might be thinking at this point, why tensile stresses? What tensile stresses? Tensile stresses arise in the solder bump when the operating temperature of the flip chip device goes through the glass transition temperature (Tg). An explanation of why can be seen in Figures 1 and 2.

As a quick refresher, the glass transition temperature marks the midpoint between a thermoset polymer being hard and brittle to soft and squishy. As underfill approaches the Tg, the CTE starts to increase dramatically (from 30 ppm/°C to 80 ppm/°C) with no corresponding decrease in modulus. This delay occurs because changes in the coefficient of thermal expansion (CTE) in polymers tend to be driven by changes in the free volume, while changes in modulus tend to be driven by increases in translational and rotational movement of the polymer chains. Increases in CTE tend

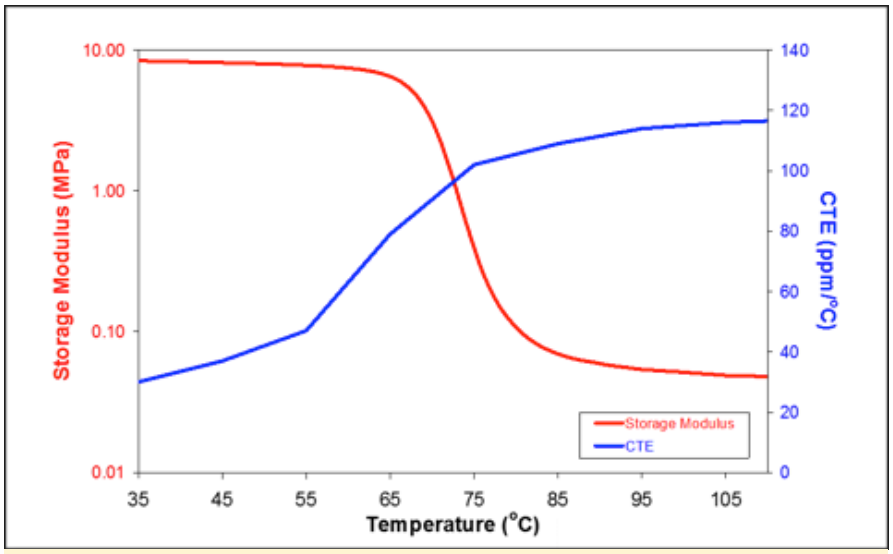

Figure 1. As underfill approaches the Tg, the CTE starts to increase dramatically.

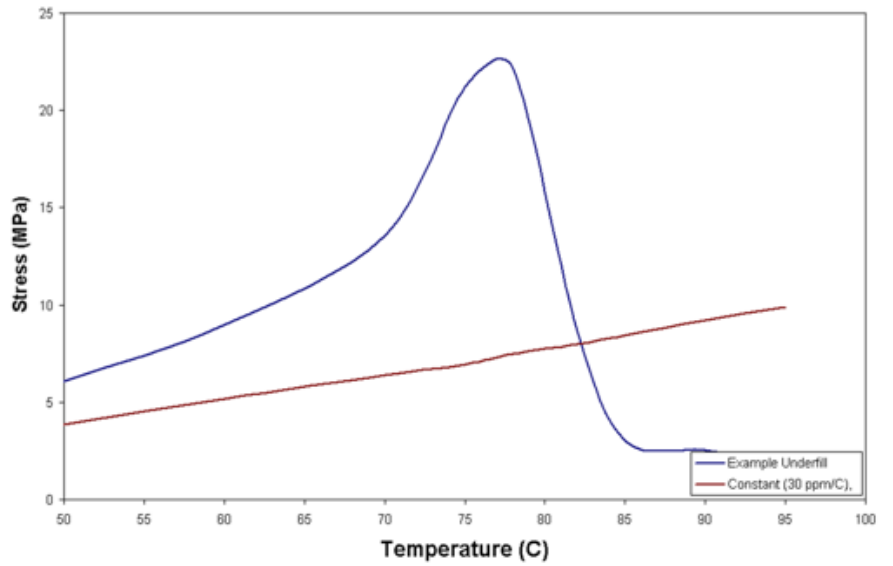

Figure 2. Tensile solder stress—elastic, compatibility of displacements.

to initiate before decreases in modulus because lower levels of energy (temperature) are required to increase free volume compared to increases in movement along the polymer chains.

Once the underfill has a high CTE and a high modulus, increases in temperature will induce a high tensile stress since the stiff underfill is now expanding at a rate greater than the solder bump (see Figure 2). However, as the temperature reaches the Tg, the modulus now begins to drop by orders of magnitude. This results in a very soft material that, even though the CTE is still high, does not have the stiffness to maintain stress on the solder bump. This behavior means that there is a very narrow window in which low Tg underfill would cause failure in electronic devices.

In fact, a change in operating temperature of just 5˚C can reduce (or increase) times to failure by up to 5X to 10X. This is partially due to the narrow window in which CTE and modulus is high and also partially due to the unique nature of tensile and compressive stresses on thermo-mechanical fatigue behavior. Previous research on solder has shown that when the mean stress changes from tensile to neutral (not tensile or compressive), the cycles to failure can change between 10X to 100X. (This is when the stress range is the same for both conditions.) And when the mean stress changes to compressive, time to failure can be almost infinite. This infinite condition is what happened when initial testing seemed to show that devices with low Tg underfill were bullet-proof.

So, what have we learned, and where do we go from here? First, in regards to low Tg underfill, all tests based on JESD22-A104 are WORTHLESS. Let me repeat that: WORTHLESS. Second, the industry may soon reach a decision point. The immediate response to the low Tg underfill fiasco was to ban low Tg underfill from all products (assuming the OEM customers knew about it). The result is that there are relatively few companies still using low Tg underfill. Or, if they are, they are making a more concerted effort to ensure the operating temperature is far away from Tg. This has resulted in a number of mid-Tg products, where the Tg is not as low as the 70˚C that caused failures but not as high as the original 125-150˚C.

However, these higher Tg underfills cause problems not only for low-K dielectrics, but also in regards to warpage of the flip chip. The larger the silicon die, the larger the warpage. If the warpage reaches a critical limit, it cannot attach to a lid or some other thermal solution. The tipping point seems to be when the die size exceeds 25x25. Many ASIC designs and devices for telecom/enterprise applications are reaching this limit. Will they go back to low Tg blindly? Will they make an effort to understand low Tg and apply it correctly? Or will they go in a completely different direction (except TSV; that has been pushed out for another three years). Time will tell.

http://jdrewscott.wordpress.com/2009/08/24/intellectual-property-woes/

Craig Hillman is CEO and Managing Member for DfR Solutions. Dr. Hillman's specialties include best practices in Design for Reliability (DfR), Pb-Free strategies for transitioning to Pb-free, supplier qualification (commodity and engineered products), passive component technology (capacitors, resistors, etc.), and printed board failure mechanisms. Dr. Hillman has over 40 Publications and has presented on a wide variety of reliability issues to over 250 companies and organizations.