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Challenges with Package on Package (PoP): Part 1, Manufacturability

Craig Hillman, Cheryl Tulkoff and Greg Caswell

5110 Roanoke Place, Suite 101, College Park, Maryland 20740 | Phone: (301) 474-0607 | Fax: (866) 247-9457 | www.dfrsolutions.com

Introduction

The future of electronic package is 3D. From stacked die to Intel's recent introduction of the 3D transistor[1], the continued progression in Moore's Law is being accomplished by going 'up'. For the majority of design engineers, nowhere is this trend more concrete then the increasing utilization of components offered with a package-on-package (PoP) architecture.

Package on package is a configuration where two packaged integrated circuits are placed directly on top of each other (aka, stacked packages). The interconnects, or solder joints, are between the top package and the bottom package and the bottom and the PCB (note, some PoP configurations have more than two packages in the stack[2]). The top package is traditionally thicker, containing multiple or stacked die, while the bottom package is thinner, with either smaller or thinner die. While various patents, and some commercial product, have focused on PoP with leaded devices, the overwhelming configuration is with ball grid array (BGA) technology. Implementation of the PoP concept took off in the 2003-2005 timeframe, with the first JEDEC package outlines defined in 2006[3]

As with all new technology[4] introduced into the electronics marketplace, the prevalence of PoP has been greatly exaggerated. PoP recent ascendancy has been primarily been through a few high volume manufacturers in the mobile and memory space. However, as PoP becomes a more common solution, it will become important for companies in low volume, high rel applications to understand the technology's limitations in regards to manufacturability and reliability.

Benefits

The benefits of PoP are well known. They include

- Less board real estate
- Better performance (shorter communication paths between the micro and memory)
- Lower junction temperatures (at least compared to stacked die)
- Greater control over the supply chain (opportunity to upgrade memory and multiple vendors)
- Easier to debug and perform F/A (again, compared to stacked die or multi-chip module or system in package)
- Ownership is clearly defined: Bottom package is the logic manufacturer, the top package is the memory manufacturer, and the two connections (at least for one-pass) are the OEM

[1] http://www.eetimes.com/electronics-news/4215729/Intel-to-use-tri-gate-transistors-at-22-nm
[2] http://www.hcdcorp.com/products/tech/techdocs/040702%20HCD%20576Mb-based%20RDRAM%20NexMod%20Datasheet%20Rev%201.5.pdf
[3] JEDEC JEP95 Section 4.22; MO-266A: Bottom; MO-273A: Top
[4] http://www.dfrsolutions.com/uploads/courses/2010_Nistec_Next_Gen.pdf

To experience the benefits of PoP, the risks of PoP, especially in regards to manufacturability and reliability, must be effectively managed. These two requirements cannot always be completely separated and therefore must be managed concurrently. Most critically, the designer must realize when and how to modify standard BGA packaging design or process guidelines.

Warpage

One of the greatest challenges in assembling PoP is managing out-of-plane warpage[5]. For the purposes of this paper, it will be assumed that the OEM has no control over the design of the PoP construction. Therefore, the OEM must somehow deal with the warpage that is intrinsic with the PoP delivered by the part manufacturer. The bottom PoP packages are especially susceptible due to their construction, thin body, and low-profile solder balls. The direction of warpage, concave or convex, is also not necessarily intuitive and is based on a complex interaction between the die, molding compound, and substrate (and, to a lesser extent, the underfill/die attach).

Therefore, a critical first step in any DfM / DfR activity is to characterize[6] the warpage behavior of the PoP part over the expected reflow profile. Within the bounds of a nominal reflow profile (ramp rates, hold times, peak temperature), the warpage is not expected to vary dramatically[7]. The primary control the OEM can have over PoP warpage is to select either a one-pass or two-pass[8] assembly.

One pass assembly involves mounting and reflowing the top and bottom packages at the same time. The bottom package is first placed on the board. The top package is then dipped in flux or solder paste and then placed on the bottom package. Both packages are then run through the reflow oven in a single pass. For a two pass assembly, the top and bottom packages are assembled in a separate process (either at the outsourced semiconductor assembly and test OSAT) manufacturer or at the contract manufacturer (CM)).

While there are logistical and cost drivers that influence one or two-pass assembly, the influence of the stackup on warpage behavior should be taken into consideration. This is especially true if the measured warpage during one-pass, the preferred assembly method, is close to or exceeds industry specifications (see Table 1). Industry best practice is to typically aim for 0.05 mm of warpage at the reflow temperatures (or, at least, less than the coplanarity requirements). The actual warpage of the PoP, in terms of separation and shape (convex or concave) can potentially have a strong influence on bond pad design.

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[5] Experimental studies by KIC and RIT have shown that the root cause for more than 90 percent of the PoP assembly defects is package warpage (Reflow significance on Package on Package assembly by S Manian Ramkumar, PhD, Rochester Institute of Technology and Brian O'Leary, KIC)

[6] This can be performed using a number of interference techniques, including digital interference contrast (DIC), fringe projection, and a number of moire techniques (shadow moire, projection moire, etc.)

[7] Though, the PoP will tend to have a relatively large mass and is at risk of cold solder joints if the process is not re-optimized

[8] Also known as single or double pass

Table 1

Ball Pitch (mm)	Ball Diameter (mm)	Maximum Coplanarity (mm)[9]			Maximum Coplanarity (mm)[10,11]	Maximum Warpage (mm)[12]
		≤10	10-14	≥14	All	All
1.27	0.75	N/A	N/A	N/A	0.20	N/A
1.27 / 1.00	0.60	N/A	N/A	N/A	0.20	0.25
1.00	0.55	N/A	N/A	N/A	0.20	N/A
1.00 / 0.80	0.50	0.12	0.12	0.12	0.20	0.22
0.80 / 0.65	0.45	0.12	0.12	0.12	0.20	N/A
0.80 / 0.65	0.40	0.08	0.10	0.12	0.10	0.17
0.80 / 0.65	0.35	0.08	0.10	0.12	0.10	0.17
0.80 / 0.65 / 0.50	0.30	0.08	0.10	0.12	0.08	0.14
0.50 / 0.40	0.25	0.08	0.10	0.12	0.08	0.11
0.40	0.20	0.08	0.10	0.12	0.08	0.10

Bond Pad Design

The warpage of the PoP will play a key role in determining if the board bond pads will be solder mask defined (SMD) or non-solder mask defined (NSMD). This is a surprisingly complex decision and there are a number of advantages and disadvantages to both approaches in regards to manufacturability and reliability.

NSMD is the traditional board bond pad design for BGA packages and there are several advantages to this approach. A NSMD solder joint will typically last longer than a SMD solder joint when subjected to temperature cycling and vibration because of the additional attachment around the edge of the bond pad. A NSMD pad is also smaller, allowing more space for routing of traces between pads, and provides more uniformity because the copper etching process is more controlled than solder mask. However, finer pitch offerings (down to 0.3mm) start to make it difficult to maintain the soldermask webbing.

SMD pads allow for a thicker web, but less room for routing. SMD bond pads have a larger surface area attachment to the laminate, which can prevent pad cratering that can occur due to excessive flexure during manufacturing or operation (e.g., drop). SMD solder joints also have a higher standoff. This provides greater compliance, making for a more robust solder joint during

[9] JEDEC Publication 95 (JEP95), Design Registration 4.22, Fine-pitch, Square Ball Grid Array Package (FBGA) Package-on-Package (PoP), March 2010
[10] JEDEC Publication 95 (JEP95), Design Guide 4.5, Fine Pitch Square Ball Grid Array (FBGA) Package, January 2009
[11] JEDEC Publication 95 (JEP95), Design Registration 4.14, Ball Grid Array Package, April 2011
[12] JEITA ED-7306, Measurement methods of package warpage at elevated temperature and the maximum permissible warpage, March 2007

shock or drop events[13], and allows easier access for cleaning. It is the ability of SMD to provide a higher standoff that can be crucial in mitigating the out-of-plane warpage experienced in PoP packages.

Because SMD has less of a collapse than NSMD, some companies have implemented SMD bond pads on PoP packages as a way to mitigate warpage. When faced with more challenging warpage behavior and tight production deadlines, a non-standard solution has been a hybrid of NSMD and SMD to temporarily maximize assembly yield. An example of resolving a difficult concave warpage in a PoP is to populate the peripheral bond pads with a SMD design with a minimum solder mask opening and to slowly open the solder mask to a standard NSMD bond pad in the center of the array.

Other bond pad design attributes tend to have a more moderate effect on manufacturability. Board bond pad diameters should be equivalent to package bond pad dimensions (typically about 70% of the ball diameter; see Table 2). Smaller bond pad diameters can reduce the degree of collapse, but will also introduce asymmetry which can greatly reduce time to failure in temperature cycling and vibration environments.

Few, if any studies, are available on the effect of bond pad geometries on PoP manufacturability. Some BGA designs currently use a non-circle geometry, such as square or octagon, to improve manufacturability and this same modification may provide some value in a PoP assembly process.

Table 2

Ball Pitch (mm)	Ball Diameter (mm)	Bond Pad Diameter (mm)					
		PBGA		Fine Pitch BGA / CSP		PoP	
		SMD	NSMD	SMD	NSMD	SMD	NSMD
1.27	0.75	0.55	0.60				
1.27 / 1.00	0.60	0.45	0.50				
1.00	0.55					0.35	0.35
1.00 / 0.80	0.50	0.40	0.35	0.35	0.35	0.35	0.35
0.80 / 0.65	0.45	0.35	0.30	0.30	0.30	0.30	0.30
0.80 / 0.65	0.40			0.30	0.30	0.28	0.30
0.80 / 0.65	0.35			0.25	0.25	0.25	0.25
0.80 / 0.65 / 0.50	0.30			0.20	0.20	0.20	0.20
0.50 / 0.40	0.25			0.17	0.17	0.20	0.20
0.40	0.20			0.14	0.14		

[13] It is important to note here that concerns with flexure and drop can also be resolved through other means, including plating materials (no ENIG), solder materials (e.g., SAC105), location, and the use of staking/underfill materials.

Stencil Design / Solder Materials

Of course, solder mask and bond pad design is just one aspect of PoP design for manufacturability. Stencil design and solder materials also play a critical role.

Many component manufacturers and other sources recommend that for PoP assembly the stencil aperture should be slightly larger than the bond pad to induce an overprint. This provides a slightly better paste release and, more importantly, increases the volume of solder paste to mitigate any coplanarity / warpage issues. This approach, which should only be used for NSMD pads, can be challenging as it can lead to solder splash, solder balling, and potential bridging, especially for fine pitch designs.

For a lead-free process, the typical aperture / bond pad ratio is 1:1. There is some debate within the electronics community about the geometry of the aperture. Some prefer a square aperture for its release characteristics, especially for smaller openings. Others will claim round apertures provide a more uniform deposit of paste. Some design of experiments may be required, especially at 0.4mm and 0.3mm pitch.

Finally, the choice of assembly materials is just as an important DfM activity as board-based geometries. The paste used for the interconnection between the bottom package and the printed board should be optimized for slump and wetting characteristics, especially at elevated temperatures. Anti-head in pillow formulations are recommended given PoP susceptibility to this phenomenon. For the connection between top and bottom package, there is a choice of paste or tacky flux. Tacky flux is typically preferred in high volume applications. When applied, the coverage of the flux should be to at least half-way up the solder ball. The application of solder paste is more challenging (screen printing is typically not an option), but provides more margin in terms of warpage / coplanarity issues.

Next: Part 2, Reliability

Analysis Information

This white paper may include results obtained through analysis performed by DfR Solutions' Sherlock software. This comprehensive tool is capable of identifying design flaws and predicting product performance. For more information, please contact DfRSales@dfrsolutions.com.

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