Integrated Circuit Reliability Prediction Based on Physics-of-Failure Models in Conjunction With Field Study

Avshalom Hava, Edward Wyrwas, Jin Qin, Lloyd Condra, Joseph B. Bernstein

Abstract—Reliability models, based on physics-of-failure mechanisms, have been developed for dynamic random access memories (DRAM), microcontrollers and microprocessors using a new software tool. Field data from a large fleet of mobile communications products, that were deployed over a period of 8 years, were analyzed to validate the tool's accuracy. Strong correlation of 80% is demonstrated between measured and predicted values.

Index Terms—Failure Rate, Physics-of-Failure, Reliability, Simulation

I. INTRODUCTION

THE continued scaling down of semiconductor feature sizes raises challenges in using and developing electronic circuit reliability predictions. Smaller and faster circuits cause higher current densities, lower voltage tolerances and higher electric fields, which make the devices more vulnerable to early failure. Emerging new generations of electronic devices require improved tools for reliability prediction in order to investigate new manifestations of existing failure mechanisms, such as Negative Bias Temperature Instability (NBTI), Electromigration (EM), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB).

Reliability prediction simulations are the most powerful tools developed over the years to cope with these challenging demands. Simulations may provide a wide range of predictions, starting from the lower-level treatment of physics-of-failure (PoF) mechanisms up to high-level simulations of entire devices [1]-[2]. As with all simulation problems, primary questions need to be answered: "How accurate are the simulation results in conjunction to the real world? What is the confidence level achieved by the simulations?" Hence, the

validation and calibration of the simulation tools becomes a most critical task. Reliability data generated from field failures best represents the electronic circuit reliability in the context of the target system or application. Field failure rates represent competing failure mechanisms' effects and include actual stresses, in contrast to standard industry accelerated life tests.

In this paper, we present a thorough reliability analysis of field failure data recorded from 2002 to 2009 in order to generate real failure rates for various device process technologies and feature sizes (or "technology nodes"). The results of this analysis are used to verify PoF models and a competing failure approach, as implemented in new reliability prediction methods - *FaRBS* (Failure rate based SPICE) and *MaCRO* (Maryland Circuit Reliability-Oriented) combined into one software tool [3]. Comparison of actual and simulated failure rates shows a strong correlation of 80%. The validation process and its data sources are illustrated in Figure 1.
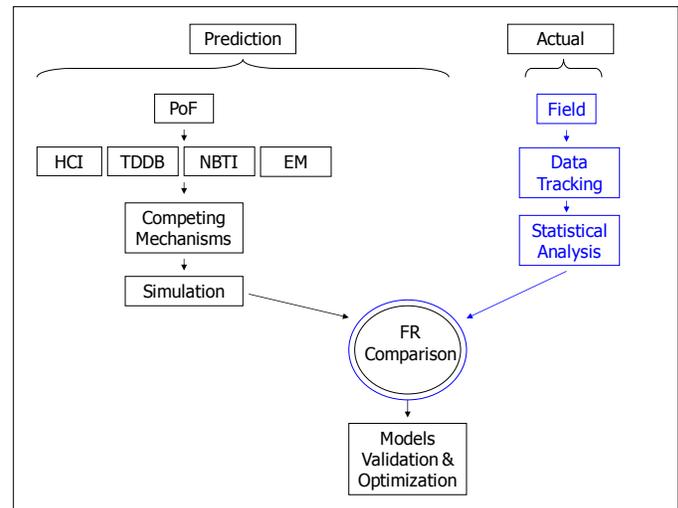

Figure 1. The data sources used for IC reliability prediction based PoF models and simulation validation. Actual field data is confronted with two primary approaches used by industry to predict failure rates.

II. RELIABILITY MODELING AND SIMULATION

A. History

There has been steady progress over the years in the development of a physics-of-failure understanding of the effects that various stress drivers have on semiconductor structure performance and wearout. This has resulted in better modeling and simulation capabilities. Early investigators sought correlations between the degradation of single device

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parameters (e.g. V_{th}, V_{dd} or I_{sub}) and the degradation of parameters related to circuit performance such as the delay between read and write cycles. It was quickly realized that the degradation of a broad range of parameters describing device performance had to be considered, rather than just a single parameter [1]. Most of the simulation tools tend to simulate a single failure mechanism such as Electromigration (EM) [4]-[5], Time Dependent Dielectric Breakdown (TDDB) [7], Negative Bias Temperature Instability (NBTI) [7]-[8] and Hot Carrier Injection (HCI) [9]. System-level simulators attempting to integrate several mechanisms into a single model have been developed as well. The latest circuit design tools, such as Cadence Ultrasim and Mentor Graphics Eldo, have integrated reliability simulators. These simulators model the most significant physical failure mechanisms and help designers address the lifetime performance requirements. However, inadequacies, such as complexity in the simulation of large-scale circuits and a lack of prediction of wearout mechanisms, hinder broader adoption of these tools [10].

B. Validation Concerns

Reliability simulations are commonly based on a combination of PoF models, empirical data and statistical models developed over the years by different research groups and industries. The inevitable consequence of a wide range of models and approaches is a lack of confidence in the obtained predictions for any given model. From the point of view of a real-world end-user, single failure mechanism modeling and degradation simulations are less meaningful then system level reliability.

Validation and calibration of simulations are both accomplished by comparing simulation predictions with empirical data obtained from lab tests or by analyzing field data. To evaluate the reliability of their devices, semiconductor manufacturers use lab tests such as environment stress screens (ESS), highly accelerated lifetime testing (HALT), HTOL and other accelerated life tests (ALT).

III. Failure Mechanisms Models

The dominant failure mechanisms in Si-based microelectronic devices that are most commonly simulated are EM, TDDB, NBTI and HCI. Other degradation models do exist but are less prevalent. These mechanisms can be generally categorized as Steady State Failure Modes (EM and TDDB) and Wearout Failure Modes (NBTI and HCI) [12]. Steady state (random) failure modes are normally considered to be random cases of "stress-exceeding-strength". The hazard functions generated by random failure modes are constant over time and may produce failures during all bathtub curve stages. On the contrary, the wearout failure modes generate increasing hazard function and are predominated in later stages of the device life. Wearout failure modes at sub-micron nodes are experienced earlier in the anticipated life of a device, within what was once thought to be dominated only by the steady state failure modes. A brief explanation of each failure

mechanism is necessary to understand their contribution to the overall device failure rate.

Electromigration can lead to interconnect failure in an integrated circuit. It is characterized by the migration of metal atoms in a conductor along the direction of the electron flow. Electromigration causes opens or voids in some portions of the conductor and corresponding hillocks in other portions [4]-[5], [11].

Time Dependent Dielectric Breakdown is caused by defect generation and accumulation that reaches a critical density in the oxide film. The underlying process might be driven by the applied voltage or the tunneling electrons. Damage caused by the accumulated defects will result in performance degradation and eventual failure of the transistors within a device. The gate dielectric breaks down over a long period of time for devices with larger feature sizes (>90 nm) due to a comparatively low electric field. Core voltages have been scaled down proportionally to feature sizes, but since supply voltages have remained constant, higher electric fields exist at smaller feature sizes. Therefore, field strengths are still a concern since high fields exacerbate the effects of TDDB [7], [11].

Negative Bias Temperature Instability occurs only in pMOS devices stressed with a negative gate bias voltage while at elevated temperatures. Degradation occurs in the gate oxide region allowing electrons and holes to become trapped. Negative bias is driven by smaller electric fields than hot carrier injection, which makes it a more significant threat at smaller technology nodes where increased electric fields are used in conjunction with smaller gate lengths. The interface trap density generated by NBTI is found to be more pronounced with thinner oxides [7]-[8], [11].

Hot Carrier Injection occurs in both nMOS and pMOS devices stressed with drain bias voltages. High electric fields energize the carriers (electrons or holes), which are then injected into the gate oxide region. Like NBTI, the degraded gate dielectric can then more readily trap electrons or holes, causing a change in threshold voltage, which in turn results in a shift in the subthreshold leakage current. HCI is accelerated by an increase in bias voltage and is the predominate mechanism at lower stress temperatures [9], [11]. Therefore, hot carrier damage, unlike the other failure mechanisms, will not be replicated in HTOL tests, which are commonly used for accelerated life testing [13].

IV. The Simulation Tool

A. Mathematical Theory

The simulation tool used for this research is a web-based application based on recent PoF circuit reliability prediction methodologies that were developed by the University of Maryland (UMD) for 130 nm and 90 nm devices [14]. The two methods developed are referred to by the acronyms of

FaRBS (Failure-Rate-Based SPICE [spacecraft, planet, instrument, C-matrix, events]) and *MaCRO (*Maryland Circuit Reliability-Oriented). *FaRBS* is a reliability prediction process that uses accelerated test data and PoF based die-level failure mechanism models to calculate the failure rate of integrated circuit components. As its name implies, it uses mathematical techniques to determine the failure rate of an integrated circuit. *MaCRO* contains SPICE (Simulation Program with Integrated Circuit Emphasis) analyses using several different commercial applications, wearout models, system reliability models, lifetime qualification, and reliability and performance tradeoffs in order to achieve system and device reliability trends, prediction and analysis.

The simulation tool can implement two distinct approaches to compute reliabilities:

- Independent of Transistor Behavior (ITB);
- Dependent on Transistor Behavior (DTB).

These approaches are used to determine each failure mechanism's contribution to circuit level failure through the analysis of transistor stress states (bottom-up approach). The ITB approach makes two assumptions:

(1) In each integrated circuit, each failure mechanism has an equal opportunity to initiate a failure, and

(2) each can be initialized at a random interval during the time of operation.

Conversely, DTB takes place in a SPICE simulation to determine these contributions based on transistor behavior and circuit function. In a circuit model of a functional group, a user can develop mechanism weighting factors by examining the IV curves of each transistor within the circuit. Each failure mechanism is driven by either current or voltage states such as the presence of a gate bias for Bias Temperature Instability. Assessing each transistor using guidelines determines its susceptibility to a particular failure mechanism. After a complete assessment of the circuit, one can tabulate the results by summing the total time that the quantity of transistors is affected by each mechanism and calculate an overall percentage for each mechanism based on the quantity of affected transistors, the total operating time of the analyzed functionality, and the total quantity of transistors within the circuit.

For the validation study presented in Section V of this paper, the ITB approach was used. DTB analysis plays a critical role when analyzing complex functional groups such as processor cores; however, the lower transistor count functional groups utilized for the validation study did not clearly delineate a leader in regards to failure mechanisms during their DTB SPICE analysis.

The software assumes that all the parameters for these models are technology node dependent. It is assumed that the technology qualification (process qualification) has been performed and at least one screening has occurred before a device is packaged. This reliability prediction covers the steady-state random failures and wearout portions of the bathtub curve concept.

B. Failure Rate Calculations

Each failure mechanism described above would have a degradation rate, λ_i, driven by a combination of temperature, voltage, current, and frequency. Each one affects the on-die circuitry in its own unique way; therefore, the relative acceleration of each one must be defined and averaged under the applied condition. The failure rate contribution of each can be normalized by taking into account the effect of the weighted percentage of that failure rate. We ignore interactions between failure mechanisms for practical reasons although deeper studies of potential interactions could be made in the future. This assumption simplifies the device wearout modeling process and eases the calculation of the overall acceleration factor. It is based on the fact that each failure mechanism has its specific degradation region inside the transistor. TDDB causes damage inside the gate oxide, while HCI/NBTI increases interface trap density. HCI will precipitate the occurring of TDDB, but the interrelation is very complex and normally insignificant and negligible [11]. For pMOS, HCI and NBTI have been reported to be independent [12]-[16].

For the four mechanisms of EM, HCI, NBTI and TDDB, the normalized failure rate can be defined as λ_{EM}, λ_{HCI}, λ_{NBTI} and λ_{TDDB} respectively. In order to achieve more accuracy in the overall failure rate estimation, it is useful to split the IC into equivalent function sub-circuits and refer to it as a system of functional group cells, for example: 1 bit of SRAM, 1 bit of DRAM, one stage of a ring oscillator, and select modules within Analog-to-Digital circuitry (ADC) etc. For each functional group type, the failure rate can be defined as a weighted summation of each failure rate type multiplied by a normalization constant for the specific failure mechanism.

$$\lambda_F^1 = \sum \left(K_{i,F} \times \lambda_i \right) \qquad (1)$$

where λ_F^1 is the failure rate of one unit of functional group, F. These failure rates are calculated as proportions of the input ALT failure rate (assuming it is reasonably accurate) and technology node dependent acceleration factors using PoF models, technology node parameters, and several electro-thermal parameters. $K_{i,F}$ is a constant defined by the weight percentage of functional group F as it is affected by the ith failure mechanism and λ_i is the normalized failure rate of any failure mechanism. Normalization is used to combine the failure rate contribution of each failure mechanism per transistor in a functional group across the entire functional group. The $K_{i,F}$ constants are extracted from SPICE simulation in the DTB approach. The SPICE analysis examines the individual transistor stress states (i.e. bias voltage) within each circuit functional group. For example,

the failure rate of electromigration affecting a DRAM group would be $K_{EM,DRAM} \times \lambda_{EM}$, where $K_{EM,DRAM}$ is a constant defining the weight percentage that DRAM has from the normalized electromigration failure rate. The overall DRAM failure rate per functional group, λ^1_{DRAM}, is:

$$\lambda^1_{DRAM} = K_{EM,DRAM} \times \lambda_{EM} + K_{HCI,DRAM} \times \lambda_{HCI} + K_{NBTI,DRAM} \times \lambda_{NBTI} + K_{TDDB,DRAM} \times \lambda_{TDDB} \quad (2)$$

Where $K_{EM,DRAM}$ is a constant defined by the weight percentage that DRAM has from Electromigration, λ_{EM} is the normalized failure rate of Electromigration, $K_{HCI,DRAM}$ is a constant defined by the weight percentage that DRAM has from HCI, λ_{HCI} is the normalized failure rate of HCI, $K_{NBTI,DRAM}$ is a constant defined by the weight percentage that DRAM has from NBTI, λ_{NBTI} is the normalized failure rate of NBTI, $K_{TDDB,DRAM}$ is a constant defined by the weight percentage that DRAM has from TDDB and λ_{TDDB} is the normalized failure rate of TDDB. Considering the probability of a specific functional group operating during the time when failure occurs is a modification to Equation (1):

$$\lambda_F = P_F \times \lambda^1_F = P_F \times \sum \left(K_{i,F} \times \lambda_i \right) \quad (3)$$

where λ_F is the failure rate of a functional group as the contributor to the potential failure of the device under analysis and P_F is the probability that that functional group was accessed at the time of failure (its degraded operation at any point in time would cause immediate failure of the device). This probability factor is either known by the circuit designer, extracted from the DTB SPICE analysis, or are general rules of how the functional group under analysis operates; i.e. random read-write in memory. The total failure rate of a component, λ_T, can be defined as being equal to the summation of the total number of each functional group multiplied by the failure rate of each functional group type.

$$\lambda_T = \sum N_F \lambda_F = N \times \sum \left(N_F / N \right) \times \lambda_F = N \times \sum A_F \times \lambda_F \quad (4)$$

where λ_T is the failure rate of the component under analysis, N_F is the total number of each function group, N is the total number of all types of function groups and A_F is the ratio of the number of units of the nth functional group type to the total number of functional groups that exist in the component under analysis. Equations (1)-(4) explain how the multiple mechanism theory is used in the simulation tool. They can be used when considering any degradation mechanisms. The prediction process is demonstrated in Figure 2.
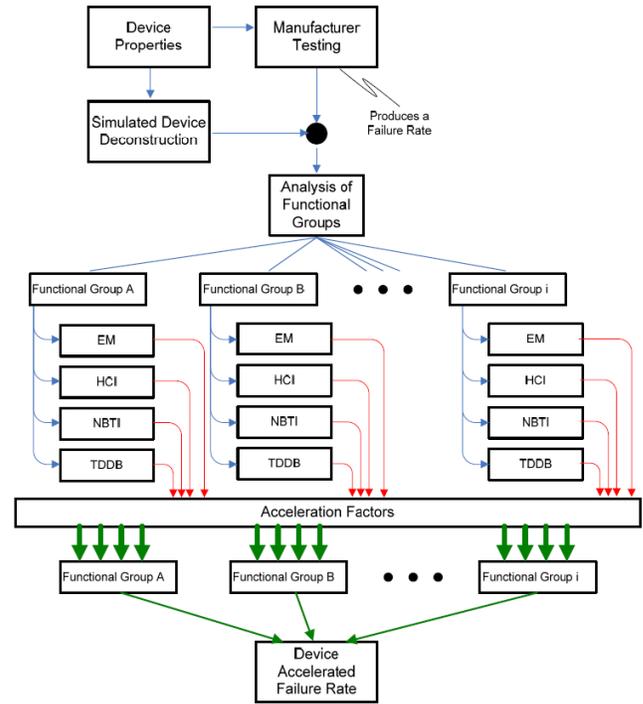

Figure 2. The simulation tool process methodology. The simulated IC is treated as a system having several functional groups affected by different failure mechanisms. The differences in the two approaches, ITB and DTB, would take place in the "Analysis of Functional Groups" process block.

V. FIELD DATA

A. Data Source

An extensive field study was conducted in order to demonstrate the accuracy of the simulation tool and verify its prediction capabilities. Reliability predictions were performed based on field failures of DRAMs, microcontrollers and microprocessors, as shown in Table 1.

Vendor Part Number	Part Description	Vendor	Tech. Node
MT16LSDF3264HG	256MB DRAM	Micron	150 nm
M470L6524DU0	512MB DRAM	Samsung	100 nm
HYMD512M646BF8	1GB DRAM	Hynix	110 nm
MC68HC908SR12CFA	Microcontroller	Motorola/ Freescale	90 nm
RH80536GC0332MSL7EN	Pentium Processor	Intel	90 nm

Table 1. The ICs used for the field study. Different types of ICs and the wide node range exemplify the simulation tool flexibility.

The field data were extracted from a Motorola database, which encompasses shipments and customers' claims. Unique identifiers of each product and failure enabled the detailed statistical field analysis. The ICs were assembled on boards belonging to a family of communication products shipped during 2002-2009. Failure analysis was not carried out due to resource constraints, as it is generally the case in low failure rates. We assume that the failures occurred due to the predominate failure mechanisms mentioned in the beginning of the manuscript. Component complexity and electrical characteristics were extracted from corresponding component documentation.

As the shipping and failures are recorded continuously, several reliability measurements can be held. The first one is the monthly failure rate, which is expressed as:

$$\%Monthly\_F.R. = \frac{Monthly\_Failures}{Cumulative\_Deployed\_Units}100\% \qquad (5)$$

The second one is the average failure rate, which reflects the overall reliability trend over time:

$$\%Average\_F.R. = \frac{Cumulative\_Failures}{Cumulative\_Working\_Months}100\% \qquad (6)$$

Both measurements are independent in the failures time distribution and can describe decreasing, constant and increasing failure rate. In the specific case where the average failure rate is rather constant over time, we can conclude that the integrated circuit is within its useful life period. Traditionally, the exponential distribution is used in this part of life to describe integrated circuits reliability in terms of FIT (one FIT equals one failure per 1E9 hours) as it has great mathematical advantages [16].

Nevertheless, as mentioned above, integrated circuits are exposed to mixture of failure modes with different hazard function behavior (random and wearout). Constant percentage of failure rate calculated in Eq. (6) will imply that the integrated circuit has not reached its wearout period yet but it is expected to be approached in the future when wearout mechanisms will start to be significant. However, it seems that such an end-of-life period is nearly never observed in the field.

B. Field FR Calculation Illustration

The microcontroller is used hereafter to illustrate the process for acquiring environmental information and determining its failure rate based on field data. A similar process was performed for the other four ICs.

A total of 96 microcontrollers were replaced during a cumulative total of 595,412 working months. Figure 3 shows the failed ICs and cumulative months vs. operating time.
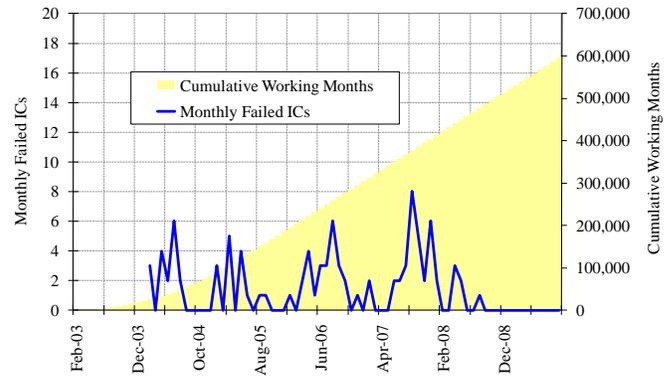

Figure 3. Failed quantity versus cumulative working months. Both parameters are used in calculation of the Monthly Failure Rate and Average Failure Rate .

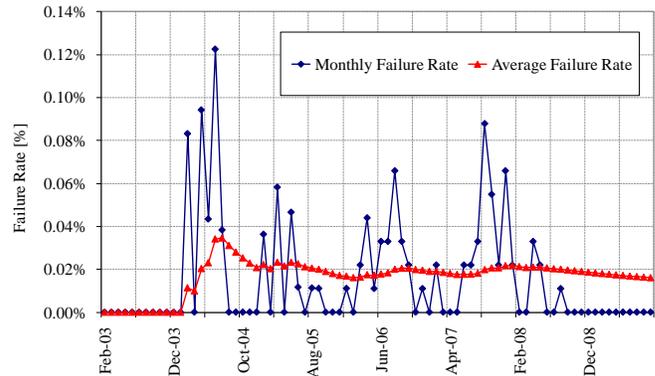The monthly and average failure rates are displayed in Figure 4:

Figure 4. Monthly and Average Failure Rates for the microcontroller. Both measurements are necessary to monitor IC reliability: While the Average Failure Rate reflects the overall trend, it is not sensitive to sudden or abnormal events since it accumulates data over time. The Monthly Failure Rate, on the other hand, is rather noisy but enables monitoring instantaneous reliability.

The average failure rate exhibits a steady state failure rate of approximately 0.02%. We then can calculate a rough estimation for the failure rate to be: λ=96/595,412=1.61E-4 Failures/Month, and the mean time to failure to be 6,202 Months. In order to convert the above *MTTF* into Hours units we must estimate how much time the user operate the product each month. Since the microcontroller operates 24 hours a day (730 hours per month), we can roughly estimate the card *MTTF* as 4,527,612 Hours, which corresponds to 220 FIT.

C. Weibull Analysis

Each failed IC is assigned to a single product with a unique serial number. Binding the shipment data by the serial number, on one hand, and the failures data, on the other hand, enabled the following Weibull analysis. We first use the Weibull

distribution since it is a versatile distribution that can take on the characteristics of other types of distributions, such as the Exponential one. Figure 5 presents a Weibull probability plot of the time to failure with 95% confidence interval (time scale is days, not months). Start time for the failed and censored data is considered the shipment date. The failure date is considered the date in which the customer has issued a claim to the depot. The sensitivity of those assumptions were analyzed and found to have a minor effect for the long term on large populations, i.e. considering delay times between shipment and deployment, on one hand, and between claim reporting and failure actual occurrence, on the other hand, has negligible effect on the results.

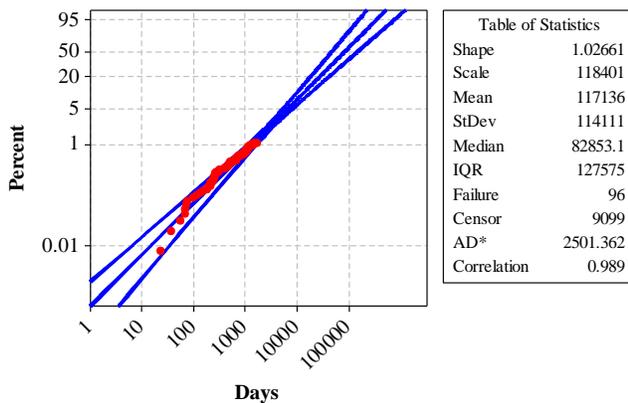| Table of Statistics	
Shape	1.02661
Scale	118401
Mean	117136
StDev	114111
Median	82853.1
IQR	127575
Failure	96
Censor	9099
AD*	2501.362
Correlation	0.989

Figure 5. Weibull probability plot of Time to Failure for the microcontroller with 95% confidence interval. Population of 9099 operational products (censored) and 96 failures were incorporated in the analysis. The points appear to enfold the fitted line well, therefore we can assume that the Weibull distribution is an appropriate choice for the data. The fitted line is based on a Weibull distribution with shape = 1.0266 and scale = 118,401 days. High correlation of 0.989 observed.

Excellent correlation to the exponential distribution was obtained, with β=1.0266. A null hypothesis of β=1 was tested in order to establish the justification for use of the exponential distribution. A Bonferroni test at confidence level of 95% provided lower and upper limits for β of 0.8758 and 1.203 respectively, with a p-value of 0.746. Thus the exponential distribution can be assumed, as shown in the following probability plot (Figure 6):

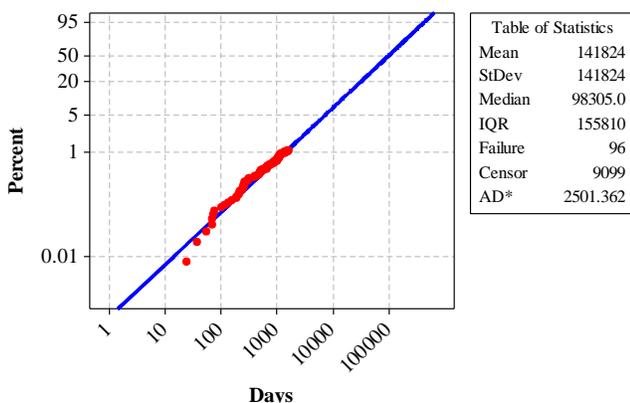| Table of Statistics	
Mean	141824
StDev	141824
Median	98305.0
IQR	155810
Failure	96
Censor	9099
AD*	2501.362

Figure 6. Exponential probability plot of Time to Failure for the microcontroller. The fitted line is based on a exponential distribution with mean (MTTF) of 141,824 days.

Using the exponential distribution, the *MTTF* is 141,824 Days. The lower and upper confidence limits are 119,072, 168,923 respectively. Assuming 24 hours per day, the *MTTF* is 3,403,776 Hours. This corresponds to 293 FIT with lower and upper confidence limits of 247 and 350 FIT respectively. This is slightly above the rough estimate of 220 FIT. Weibull analyses for all the analyzed ICs showed similar justification for the use of the exponential distribution.

VI. VALIDATION RESULTS

The reliability calculations are based on the time domain of the host computer. Except for the microcontroller, which is stressed 24 hours a day, we assume that memory parts and the processor are partly stressed depending on the user profile. A conservative assumption is that a regular user will stress the parts two shifts/day, i.e. 16 hours/day.

Table 2 shows the field failure rates and the corresponding results of the simulations. Each simulated failure rate was calculated using the software tool based on the mathematical theory described in this paper. The simulation tool inputs include the following dataset.

- Process node parameters
- Device complexity by functional group
- Accelerated test information (failure rate)
- Device duty cycle (i.e. diurnal cycling)
- Confidence level
- Field and test conditions (i.e. ambient temperature, operating frequency, core voltage and supply voltage)
- Failure mechanism parameters (i.e. Weibull parameters)

An integrated circuit's datasheet contains basic operating conditions and electrical parameters. Process node parameters were gathered during an academic and industrial literature review. These parameters include but are not limited to the thickness of the gate oxide, the permittivity of the oxide, mobility, and nominal drive current for the average device at said technology node. A generic integrated circuit at 90nm will utilize the generic 90nm set of process parameters. An integrated circuit of known fabrication such as an ASIC can utilize a proprietary set of these parameters when applicable. Device complexity is defined by the functional description and/or block diagram on the datasheet such as 16Mb of SRAM will have 16,777,216 SRAM functional cells. The P_F value for SRAM in this validation study was equal to 1, whereas a memory read error is classified as a failure of the device. Accelerated test information in the form of a failure rate is required. This input assumes that a proper accelerated test which stresses the function of an integrated circuit was performed to assess the reliability of the component. An example of this type of testing is to load-unload a FLASH

memory or perform recursive calculations on a processor at an elevated temperature until failure occurs. Confidence level is associated with this input failure rate data. Field conditions can either be assumed as the nominal electrical parameters on a datasheet – or are known by a design engineer who is using the integrated circuit in his or her system-level circuit. Test conditions can be extracted from either the accelerated test that was performed or taken as the maximum electrical conditions on the datasheet. Failure mechanism parameters were concurrently gathered during the academic and industrial literature review. These parameters include Weibull Beta values and activation energies for each failure mechanism.

Let us provide a simplified walkthrough of the process that determined these failure rates. The acceleration factor for Hot Carrier Injection is provided below. HCI can be accelerated by temperature and by voltage. The technology fitting parameter (γ) for HCI was provided as 45 by Dr. Joseph Bernstein from testing performed on a generation of these memory devices. The other parameters E_a and k are activation energy and Boltzmann's constant, respectively. The corresponding values that were used are -0.15eV and 8.617343E-5eV/K. The sources of failure mechanism equations used to devise the acceleration factors for EM, HCI, NBTI, and TDDB are [17] - [19]

$$AF_{HCI} = e^{\left(\frac{E_a}{k}*\frac{T_1-T_2}{T_1T_2}\right)}e^{\left(\gamma*\frac{V_1-V_2}{V_1V_2}\right)} \quad (7)$$

The calculator uses an acceleration factor for each possible accelerated electrical or thermal parameter of each mechanism to calculate the field failure rate. When the test and field values are the same, the non-accelerated terms are disregarded. The input parameters are discussed for the 256MB DRAM device. As mentioned previously, system and component temperature data for these field returns were taken on physical systems. For an appropriate accelerated test, the temperature of the test chamber was backwards calculated using thermal resistance equations. For the 256MB DRAM device, the junction temperature of the device is 85°C, power dissipation was 0.45W with a theta(j-a) of 51°C/W. The ambient temperature at test is therefore 62°C. The equation used to compute this test temperature value is below. The measured field temperature was 42°C ambient.

$$T_A = T_J - (P_D * \Theta_{J-A}) \quad (8)$$

The voltages used for the calculation were taken for the component's datasheet. These values were 2.5V and 2.7V for nominal and maximum voltages, respectively. Although the component was of the 150nm node, process parameters for 130nm were used. The component was used in a system for two eight hour shifts per day or a 66% duty cycle.

Part Description	Field Failure Rate [FIT]	Simulation Failure Rate [FIT]
256MB DRAM	689	730
512MB DRAM	415	418
1GB DRAM	821	1012
Microcontroller	220	249
Pentium Processor	144	291

Table 2. The ICs used for the research. The simulation failure rates are calculated using the IC intrinsic data and environmental conditions.

Figure 7 shows the comparison of the field failure rates and the simulation results, along with the 95% confidence intervals obtained by the Weibull analysis.
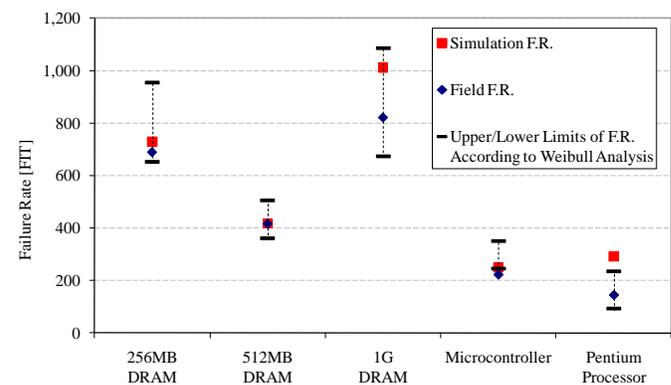

Figure 7. Comparison of the field failure rates and the simulation results, along with the confidence interval obtained by the Weibull analysis. The simulated failure rates lie well within the confidence intervals except for small deviation in the processor.

It should be noted that the DRAM failure rates presented in Table 2 and Figure 7 refer to critical faults which forced the user to replace the part. They do not reflect specific rates of different kind of errors (correctable or non-correctable) but rather a complete part failure rate.

VII. CONCLUSIONS & DISCUSSION

The validation study has shown strong correlation between the field failure rates and the ones obtained by the simulation tool. The results in Figure 7 clearly demonstrate the accuracy and repeatability of the multi-mechanism model to predict the field performance of complex integrated circuits.

The simulated estimates lie well within the confidence intervals except for the Intel processor, where a small deviation of 60 FIT observed. The small deviation between the rough estimates and the point estimations obtained from the statistical plots justify the use of the exponential distribution.

For memories, an average failure rate of 720 FIT was observed with an average deviation of 10% between the field and simulated failure rates. The average interval of the field failure rate (upper limit-lower limit) is 280 FIT. Considering the fact that the 512MB DRAM node technology is quite similar to the 1GB DRAM one (100 nm and 110 nm accordingly), both parts actually exhibit the same failure rate of 0.8 FIT per 1 MB. On the contrary, the 256MB DRAM with 689 FIT does not correspond to this projection which should have led to a failure rate of 205 FIT. This gap is rooted in the higher ambient temperature which the 256MB DRAM is exposed to, relative to the other two memories (~10°C). Nevertheless, components whose predicted failure rate is relatively large compared to similar device types, i.e. 1GB DRAM, might be categorized as more sensitive to electrical and environmental tolerances. They will be subjected to greater stresses at the peripheries of these sensitive operating ranges. Components with large operating ranges are typically operated at an average nominal value. Therefore, small fluctuations away from the mean of these larger ranges will not excessively stress the components. The microcontroller and the processor experienced lower failure rates then the memories. Furthermore, the average failure rate is 220 FIT with interval of 120 FIT.

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