PREDICTING MEMS PACKAGE LEVEL FAILURE MODES IN AUTOMOTIVE APPLICATIONS

Greg Caswell & James McLeish
DfR Solutions
Abstract

• The use of Micro-Electro-Mechanical Systems (MEMS) in sensors for safety critical vehicle systems is increasing.
  • Their use in high stress, safety critical, automotive systems makes ensuring their reliability & durability essential tasks, especially as the Vehicle System Functional Safety requirements of ISO-26262 are being implemented.

• Electronic Packaging technology is constantly evolving & improving to keep up with the advances in silicon & semiconductor technology.
  • MEMS packages can be susceptible to several failure modes that can be predicted as a device is designed using modern Computer Aided Engineering (CAE) software tools that apply Physics of Failure (PoF) methods to evaluate, eliminate or mitigate susceptibilities to failure modes during the design of a new MEMS device.
  • This Design for Reliability (DfR) approach is the most effective & efficient way to achieve Functional Safety levels of reliability-durability.
  • This paper shows a methodology for using the Sherlock ADA CAE APP to rapidly create a high-fidelity model and perform a PoF analysis of a MEMS interposer with all the conductor geometries.
Micro-Electro-Mechanical Systems (MEMS)

MEMS technologies involves the miniaturized mechanical structures and their integration with electronic or electro-mechanical elements

• The main criterion of MEMS is that there are at least some elements having some sort of mechanical functionality.

• MEMS devices can vary from relatively simple structural elements, to complex electromechanical systems with multiple moving elements under the control of integrated microelectronics

• The MEMS die must eventually be integrated into a component package that eventually must be incorporated onto a circuit board or other type of substrate of an E/E device
The Use of Automotive MEMS Applications is Growing - They are Essential in Many Safety Critical Vehicle Functions

Source: MEMS Journal

ST Microelectronics - A3G4250D
3-AXIS Gyroscope Motion Sensor

ST Microelectronics - AIS3624DQ
3-AXIS Accelerometer
Computers programs used to perform engineering analysis tasks

- Expedites the application of scientific principles to determine the properties or performance characteristics of a design, (a.k.a. CAA Computer Aided Analysis).
- Evolved to support many different engineering disciplines & industries:
  - Mechanical, Civil/Structural, Electrical/Electronics, Thermal, Hydraulics . . .
  - Automotive, Aerospace, Naval, Construction, Mining, Power Generation . . .

1. Stress analysis using FEA (Finite Element Analysis)
2. Computational Fluid Dynamics (CFD) for thermal & fluid flow analysis
3. Kinematics & Mechanical event simulation (MES)
4. Process simulation (casting, molding, and die press forming)
5. Product Optimization
6. Circuits & Electromagnetics Analysis
Most CAE programs are model “creation” tools

- Like a blank spread sheet or word document they enable the user to first create every element and then run an analysis.
- But this requires a long model creation effort and requires the user to be:
  - Very experienced with the CAE modeling program.
  - Highly knowledgeable in the specific physics and engineering discipline of the item being analyzed.
  - PhD level expertise is often required.
  - Availability and cost of this level of expertise has sometimes limited the expansion of CAE methods from reaching many areas where they could be beneficial.

A Blank Canvas
An Emerging Trend
- Application Specific CAE Apps

- Application Specific, Customized CAE Solutions.
- Auto guided, specific function, CAE Apps or analysis templates are created to provide a common, reusable semi-automated interface
- Pre-programed, off the shelf ready
  - Similar to smart phone or tablet Apps
  - Regularly needed product optimization
  - Frequently encountered problems.
  - Allows product teams to rapidly perform expert level CAE analysis without a rare, costly, CAE expert
- See Article at:
  http://www.sae.org/mags/SVE/10767
Sherlock ADA – A CAE APP Tool Suite for Physics of Failure Based Durability Simulations & Reliability Assessments of E/E Devices

Fast, Semi-Automated

• Enables rapid model creation & durability simulations runs to be interactive with design creation
• To rapidly evaluate the Durability/Reliability impact of design choices

Sherlock is the backbone to one of the most powerful reliability tools to be released for use not just by the reliability group, but by the entire engineering design and management team. Sherlock is the future of Automated Design Analysis (ADA), the integration of design rules, best practices and a return to a physics based understanding of product reliability.

It is not at the Iphone or Droid App store. But yes there is now a Physics of Failure Durability Simulation App
Physics of Failure Based Durability Simulation & Reliability Assessment

Combines dynamic stress analysis of usage & environmental conditions with failure mechanism models to perform a durability simulation

• Identifies failure susceptibilities & calculates reliability behavior over time.
• Based on Research into “CAUSE & EFFECT” Relationships in Failure Mechanisms & The variable factors that makes them “APPEAR” to be Random Events.
  • Combination of Material Science, Physics & Chemistry with Statistics, Variation Theory & Probabilistic Mechanics.

• Failure of devices or structures (i.e. hardware) are due to:
  • The gradual degradation (wearout) or
  • Rapid disruption (overstress) due to encounters with “Excessive Stresses” from the loads an item is exposed to
    • Thermal, Electrical, Chemical, Moisture, Vibration, Shock, Mechanical Loads . . .
  • Failures can also occur prematurely due to fabrication or assemble defects, excessive variable factors or even design errors that weakens the items to reduced to endurance capabilities

Failure is success if we learn from it.
- Malcolm S. Forbes
Steps in a Sherlock PoF CAE App Analysis

1) **Design Capture** – Device CAD files are loaded & combined with libraries of component & material properties to create a CAE virtual model of an electronic device or circuit board assembly.

2) **Life-Cycle Definition** – Define the reliability/durability objectives and expected environmental & usage conditions (Field or Test) that the device needs to endure.

3) **Load Transformation & Stress Analysis** – Auto creates a Finite Element Analysis to calculate and distribute the environmental and operational loads across a PCBA to the individual parts & features.

4) **PoF Durability Simulation/Reliability Analysis** - Failure Mechanisms algorithms applied to the model & stress conditions to perform a design & application specific durability simulation calculates life expectations, reliability distributions.

5) **Review Results/Risk Assessments** - Multiple views, plots and report formats to evaluate results, prioritizes risks & share results.

*For More info Ref: SAE2014-01-0233 Moving Automotive Electronics from Reliability/Durability Testing to Virtual Validation Modeling Using a Physics of Failure CAE App*
In this example a MEMS device is integrated onto a multilayer organic interposer with other components to form a Multi Chip Module (MCM) suitable for attachment to a PCB. This paper demonstrates a methodology for creating a high-fidelity CAE model of the MEMS MCM interposer with all the conductor geometries.

The failure modes that are explored with this model are package warpage prediction due to actual copper imbalance and filled microvia failure.

- Package warpage due to copper imbalance between the two sides of the MEMS interposer occurs if a Coefficient of Thermal Expansion (CTE) mismatch due to copper imbalance exists between the two sides. The bending of the package during assembly solder can then occur to such a degree that defective or weak solder interconnects are formed.

- Filled microvia failures that occur when either stacked Cu filled microvias delaminate from each other or they experience fracture at their attachment point to their pads that connect to the traces on conductor layers.
Generating the Model

The substrate model was created from the MEMS Multi-Chip Module (MCM) files of a 25 by 25mm substrate.

• Any type of MCM can be Modeled (See Following Examples)

Source: ACME Systems, ARM9 Linux Embedded Module, Aria G25 http://www.acmesystems.it/catalog_a riag25

Source: Rick Grigalunas, “Design Engineers! 1 More Reason To Use Bare Die,” ES Components Blog March 19, 2015

A 15x15mm section of the interposer substrate containing the MEMS device of interest was cut out for the analysis to limit the model size to the area of interest, to reduce model computation time.

- A 3D model of the MEMS interposer was first created using the Sherlock CAE App.
- Every segment of geometry (Traces, Vias & Layer Stack up) is modeled
  - Material properties are assigned automatically from the CAE App’s libraries
  - The microvias structures for every layer are also created
  - The model is then exported to the Abaqus CAE FEA Environment
The Sherlock CAE App Performs a Number of Durability Simulations and Reliability Assessments Internally

- Thermal Cycling Solder Attachment Fatigue
- Thermal Cycling PCB PTH Via Barrel Cracking Fatigue
- Vibration Solder Fatigue
- Shock Solder Fracture
- Actuarial (Constant Failure Rate/MTBF Tabulations)
- Conductive Anodic Filament Risk Assessment
- Stress load in Fracture Risk Assessments
  - ICT Test Stress Analysis
  - Compliant Pin Connector Insertion
- ISO-26262 Functional Safety FMECA Generator
Electronic Device Model Creation in the Sherlock CAE App is Much Faster Than Manual Model Creation in a FEA Tool

Sherlock can export:
• STP file geometry that work in most FEA/CAD tools but export includes only geometry without materials or connectivity.
• Python script for ABAQUS which supports leads and structures such as heat sinks.
• APDL scripts for ANSYS
• FEA Stress Analysis Results can then be exported back into the Sherlock environment to run Physics of Failure Durability Simulations

The Model Characteristics
• The MEMS MCM Interposer model has 2,851,604 nodes & 2,044,465 elements.
• The model includes two materials.
  • The copper material applied to the traces and vias is isotropic (properties are the same in each axis) and linearly elastic
  • The interposer material is orthotropic (properties differ in each axis)
The model can then be modified to perform predictions for several different phenomena because each trace and via has a selectable geometrical entity.

- The figure shows a single trace in the model after it has been meshed.
- The laminate and resin material is invisible.
Predicting Package Warpage

• The MCM package warpage is caused by copper imbalance between the two sides of the MEMS MCM interposer

• Excessive warpage during solder can hinder the creation of proper solder joints during assembly soldering either when a MEMS device is attached to a MCM interposer, or when the completed MCM is attached to a circuit board in an application.

• Weakened or malformed solder joints can lead to a higher probability of defective premature failure while in service.

• Prediction of package warpage can be performed using effective properties and simple models *

• The detailed model can also provide information about localized stress effects on each via

Examples of Possible MCM to PCB Solder Issues Due to Warpage

MCM BGA

Non-Wet Open

Head on pillow

Stretched joint

Head-on-Pillow Open

Source: Raiyo Aspandiar (Intel), “FCBGA Package Warpage” HDP User Group meeting
This figure illustrates the displacement magnitude across the MEMS interposer.

- The warpage analysis was plotted across a temperature range of -55°C and 260°C, with a reference temperature of 25°C.
Predicted Diagonal Warpage

At the peak solder temperature of 260°C, the peak diagonal warpage across the 15x15mm section (a span of 21 mm) is calculated to be 55µm (or 2.1 mils).
For a MEMS Accelerometer in a 6x6mm QFN-24 IC package

- The diagonal span of this Quad Flat No-lead IC is 8.5mm
- The standoff solder thickness of a QFN-24 is 35-55 um (1.4-2.2 mils)
- Depending on the location of the QFN-24 on the Interposer substrate
  - The max warpage across the MEMS component solder joint could be 5 to 45 um (see plot on previous page).
  - A 5 um warpage at the QFN-24 during soldering would be tolerable
  - But a warpage >30% of the solder thickness could skew the MEMS package, resulting in a weaken elongated or stressed solder joint
Physical Conformation of the model’s results can later be obtain on prototype parts using:

- Digital Image Correlation and Tracking (DIC/DDIT)
- An optical method that employs tracking & image registration techniques for accurate 2D and 3D measurements of changes in images.
- Often used to measure material deformations, CTE displacement, strain, and optical flow.
Example of how DIC Images across a Thermal cycle can be sequenced into an animation and plotted at each temperature of interest

<table>
<thead>
<tr>
<th>2015-09-10 DfR</th>
<th>Visualization</th>
<th>Displacement Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>25 degC</td>
<td></td>
</tr>
<tr>
<td>min / max</td>
<td>0.000000um / 0.000000 um</td>
<td></td>
</tr>
</tbody>
</table>

[μm]

- Convex
- Concave

Global Diagonal1

Click to Activate Animation
Via and Microvia Delamination and Cracking Stresses

Vias & Microvias are the structures that provide the electrical connections between the conductive copper planes and pads in substrates.

- Microvias are small (dia. \( \leq 150 \, \mu m \)), laser drilled vias, used in high I/O density packages.
- They can be copper filled or unfilled, They can be stacked, staggered or buried.

Thermal Expansion Stress can result in Microvia failures.

- The location of the microvias and the shape of the stack has been shown to have an effect on microvia stress fracture of fatigue reliability. Stress analysis using finite element models have been used to calculate these stresses.*

* Ning, Yan, Michael H. Azarian, and Michael Pecht. "Influence of Plating Quality on Reliability of Microvias" IPC APEX Expo, 2015
This analysis is to calculate the stresses & the resulting mechanical performance of vias and microvias, the structures that provide the electrical connections between copper planes and pads in substrates.

- Note: The model of the via and trace structures could also be used to perform other simulation such as electromagnetic, thermal and multi-physics simulations if needed.
- The image illustrates the detailed cross section of several vias & microvia types.

The level of detail shows:
- Flanges
- Buried vias
- Different copper layer thicknesses
- Stacked vias
- This example is of via and stacked microvia structures without staggered vias.
**Analysis Results – Pad Fracture Related Microvia Stresses at the Substrate Surfaces**

- **Red circles** are Vias above the ultimate stress of electroplated Copper that are susceptible to cracking.
- Also note that traces have a higher stress than the substrate underneath.
- Dog-boned solder ball pads, no vias underneath (Deep Blue) are at lower stress than Pad with vias.
Microvia Pad Design Considerations

The dog-bone leg pad that hold the escape routing vias or microvia experience higher stresses than the solder ball attachment pads

• This is the reason why dog-bone pad design is a standard escape routing pattern for high density substrates for this reason
Analysis Results – Microvia Stack Delamination Stresses

For Stacked microvias that go into the substrate the stresses can be higher in the middle of the stack than the flanges.

- The stress field induced by differential thermal expansion in the via is three-dimensional in nature.*
- We need to compare the Von-Mises Stress with the first principal stress in order to evaluate the stresses at the bonding interfaces of the stacked vias.
- The Von-Mises stress is appropriate when looking at the ductile failure of copper at the flanges and barrel bonding point.
- Although the bonding interfaces between copper foil pad flanges and electroplated Copper on the barrel walls are more susceptible to brittle fracture**.

The stacked micro via stress distributions are shown in the stress simulation above.

- The high stress regions are found at 2 inner interface and at the pad flanges.


** Ming-Han Wang, Mei-Ling Wu “Thermo-mechanical Stress of underfilled 3D IC packaging” IEEE EuroSimE, 7-9April, 2014
Myers, Alan M., et al

• “As a result of different thermal expansion coefficients of the metal interconnects, vias, and insulating layers, the via connections are subjected to large amounts of stress as the device is temperature cycled”.

• “Various residues consisting of fluorides and oxides, formed during the via etch process, are generally left at the interface prior to via metallization”.

• “These fluorides and oxides are generally brittle materials and when subjected to large amounts of thermal stress, crack and cause via delamination.”

**Therefore Via interfaces are more susceptible to**

• brittle fracture cracking an overstress condition

• than cyclical fatigue a wearout condition

How Does this Help Designers

The 3D stress plots for interposer substrates enable the board designers to assess many reliability risk issues.

The high-fidelity model provides the predictive capability that allows designers to adjust the layout before any manufacturing has taken place.
The stresses in the filled microvias are shown to be affected by the stack up and properties of the substrate interposer.

- Both ductile and brittle failures can be predicted using this modeling method.
- The Von-Mises stresses at the flange of the vias are indicative of the ductile cracks.
- The first principal stress at the via & pad interfaces predict that the initial design has a high probability of delamination due to brittle fracture.
- The stresses in the traces are also used to optimize the substrate design by decreasing localized stresses using different copper trace geometries.
- All three copper stress predictions were made possible by the high fidelity model quickly created by the Sherlock CAE App.
Making a full 3D FEA CAE model used to be a difficult & lengthy process

- A detailed trace via modeling approach used to be prohibitively expensive for large packages & substrates with many metal levels.*
- Expert modelers used to spend many hours to create such models.

The Sherlock CAE App quickly creates HI Fidelity E/E device CAE models & can perform a number of Physics of Failure Durability Simulations & Reliability Assessments.

- This Automation allows product designers & reliability experts, who are not modeling experts, to interact & benefit with CAE models.
- This enables the reliability & durability of products to be optimized without the time and cost of building and testing prototype parts.
- The App can also export the CAE model it creates into FEA tools like Abacus where custom analysis can be performed.

Thank you for your attention.
Any questions?

For More Information or Copies of the Presentation Slides Contact:

jmcleish@dfrsolutions.com

gcaswell@dfrsolutions.com

askdfr@dfrsolution.com

301-474-0607