Upgrading the Component Derating Process

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In the early stages of product development, effective design-for-reliability (DFR) approaches can have critical impact to the final product integrity. DFR's goal is to assure adequate product strength against lifecycle stresses proactively. At the component level, identifying and controlling critical reliability factors can take place in schematics and prototype stage (as well as later) and component derating is one popular DFR approach for assuring that individual component will be able to operate robustly against major stress elements.

Component derating is the practice of reducing stresses on electronic components to improve the end product reliability. There have been a number of derating standards established by government and industry bodies. Examples include Air Force AFSC Pamphlet 800-27, MIL-HDBK-1547, NAVSEA SD-18, NASA Johnson Space Center SSP 30312, NASA Goddard MSFC-3012, NASA Jet Propulsion Lab JPL-D-8545, Boeing MF0004-400 and RIAC Quanterion. These derating approaches will mostly improve product robustness when properly implemented. However, there are improvement and upgrading opportunities as discussed below.

First of all, the starting point for component derating is often based on the manufacturer's datasheets or specifications. However, the typical specifications provided by manufacturers are mostly functionality focused and often do not include the critical reliability and durability parameters. As a consequence, most of the derating parameters are limited to voltage, current, power, and temperature. In our view, stress evaluation in component derating can include additional considerations such as:

- Types of stresses in addition to the electrical and operating temperatures such as mechanical and chemical
- Attributes of stresses such as transient voltages, temperature spatial and temporal distributions
- Lifecycle consideration beyond operating stresses such as manufacture process effects
- Multi-stress effects (e.g., Fretting corrosion, electro-chemical migration)

Take a laser-trimmed precision resistor as an example (Figure 1), its resistance values can be adjusted finely with laser trimming. When operated under constant high temperature stress within specified limits, there is usually minimal variation of the resistance over, e.g., 30 years. However, actual power-on conditions when running these resistors often result in transient pulses that induce hot spots with much higher temporary temperature (Red area in Figure 1). These hot spots will cause gradual increase in resistance values exceeding the "precision" requirements corresponding to reliability failures. In this case, "derating" can be implemented by obtaining stress-strength relationship under peak pulsing conditions, taking into account the "trimming" variations of the given resistor population.

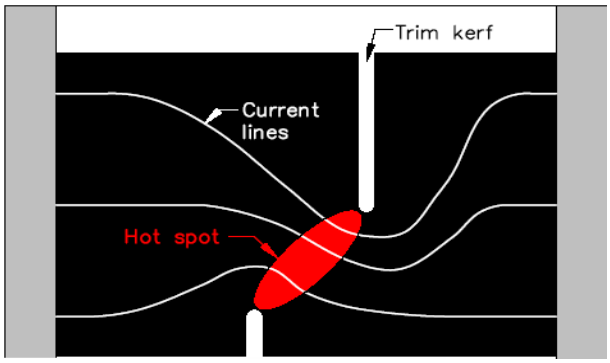

Figure 1: Illustration of the cross-section of a laser trimmed precision resistor

As another "lifecycle-stress" consideration example, when a high resistance chip resistor is mounted onto a printed circuit board, its resistance value can be "interfered" by the board surface cleanliness, such as when no-clean flux is used. The surface insulation resistance (SIR) of the board can "short-change" the actual resistor. In this case, the "derating" process should understand the process related chemical stress/effect and either restrict the maximum values of the resistors that can be mounted on such surfaces or require guard banding or cutouts to minimize the board surface SIR effects. Similar "derating" need to be considered for fine pitch components, e.g., the large area, multi-I/O and low standoff quad flat no-lead (QFN) package, where potential electric field across adjacent leads is a strong driver for dendritic growth.

The impact of derating should be evaluated scientifically when feasible, such as based on the physics-of-failure (PoF) knowledge. As an example, certain temperature-related derating rules implicitly assume that failure is always driven by elevated temperature and can be modeled by Arrhenius equation. This is the case when derating the junction temperature for semiconductor devices. Reducing the junction temperature mostly helps the device operation reliability, but there are questions worth asking when implementing the junction temperature derating rule, e.g.:

- What are the failure mechanisms that are addressed by the junction temperature derating and how is the activation energy obtained if Arrhenius equation is used? For example, hot carrier injection in a CMOS structure is not "accelerated" by increasing temperatures.

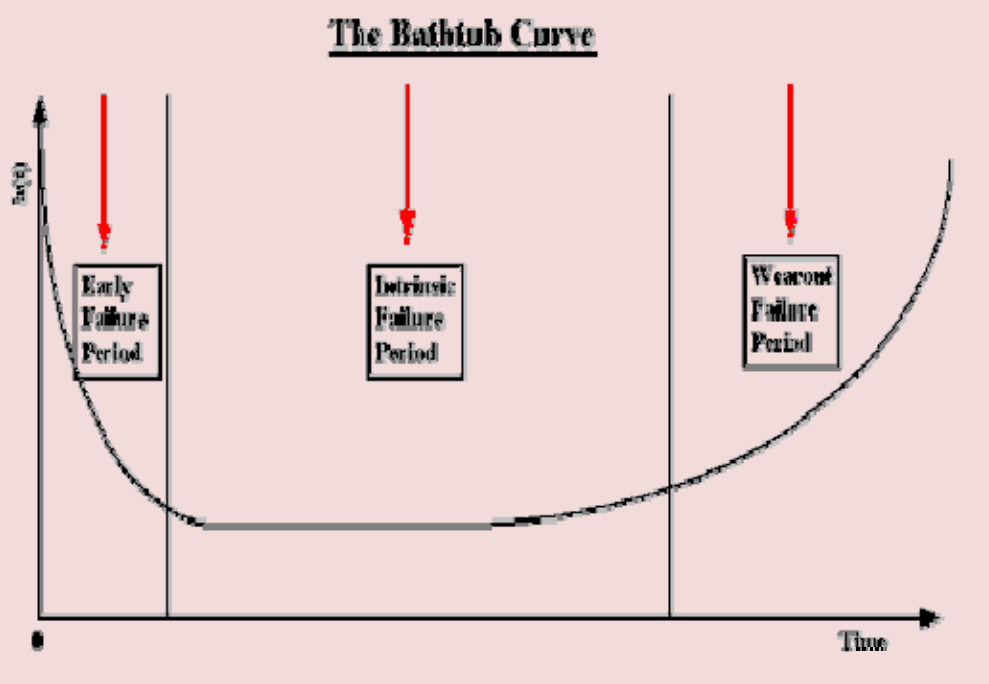

Figure 2: A typical bathtub curve

- How is the derating helping with the wearout life vs. overstress failure rates? These two attributes correspond to the different segments of a typical bathtub curve depicting reliability cycles, i.e., the wearout region vs. the intrinsic failure period in Figure 2. Reducing the semiconductor operating temperature will typically both help the high temperature related wearout performance (e.g., temperature-dependent dielectric breakdown and electro-migration) and reduce thermal runoff possibilities such as related to latch-up events.
- Junction temperature is a "macro" description of the junction temperature, which can have a spatial and temporal distribution dependent on the device structure and operating parameters. There can be local hot spots that cause early failures, which is an increasing concern as devices scale down to ever smaller feature sizes.
- Is the generic derating rule applicable to the specific IC package and system it's embedded? For example, system-in-package (SiP) could drive a different extent of derating to reach a specified performance than a, e.g., QFN package style
- Derating is not always "the more, the better", as different failure modes can emerge under different stress levels. Hot carrier injection can become critical at reduced temperature levels and a proper derating should be considered.
- Upon device scaling, leakage current will also play an important role. When leakage related power consumption is no longer negligible, the junction temperature will have an additional dependency on the leakage current, which is proportional to ~$e^{(-Ea/kT)}$, where Ea is the activation energy, k is Boltzman constant and T is the temperature in Kelvin. In this case, the junction

temperature cannot be simplistically treated as only dependent on ambient temperature anymore, thermal runoff can result from the temperature activated leakage current increase

Derating rules are not set in stone, and they should evolve with the advances in component technologies in addition to any application specific requirements and vendor capability assessments. For example, older MnO_2 based Tantalum capacitor technology can be susceptible to ignition and requires aggressive derating, while newer, polymeric based Tantalum capacitors have little risk of ignition thus less derating is needed. In the real world, derating is not always feasible either because of poor understanding of the relevant failure mechanisms (e.g., tin whisker) or demanding applications (e.g., military and aerospace). In the later cases, uprating rather than derating is sometimes pursued.

It is DfR's belief that there are opportunities for more proactive, quantitative, and comprehensive "derating" approaches. Derating should be treated as a continuous process of assuring component strength against ALL stresses in the system and lifecycle context. While the rules-of-thumb for derating are useful, their impacts cannot be ascertained without the corresponding failure physics understanding. In certain cases, rather than a simplistic percent reduction derating rule, a more cost-effective approach can come from understanding the precise functional shape of stress-strength dependency. Finally, derating effectiveness should be examined and verified with simulation, tests, and even field data where feasible.

As a summary, we propose the following four step process for an upgraded derating approach:

1. Start with quantitative, system-focused, lifecycle stress profile analysis
2. Analyze part strength impacts and system performance implications (e.g., via PoF-based acceleration models)
3. "Derate" accordingly
    a. Worst-case analysis for overstress derating
    b. Accurate stress profile and impact analysis for wear-out derating
    c. Derate at both high and low "ends"
4. Verify, validate and continuous improvements