An Engelmaier Model for Leadless Ceramic Chip Devices with Pb-free Solder

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ABSTRACT

As the transition to Pb-free progresses from consumer and computer electronics to applications with longer life requirements and more extreme use environments, there is a rising concern regarding the long-term reliability of Pb-free interconnections. In response, several publications have recently presented Pb-free solder joint reliability models. All of these models, while useful, have severe limitations. Strain rate equations and damage models allow for the use of finite element modeling (FEM) to predict solder joint reliability, but this is a specialized tool that requires the use of scarce resources. A modified Norris-Landzberg equation provides a correlation between test results and field performance, but there is a strong impetus to ensure robustness during the design stage, rather than identify potential issues after thousands of hours of testing. Extending work done by Engelmaier [3] and available experimental results from literature, DfR proposes a Pb-free first-order solder joint reliability model based upon cyclic strain energy density. The maximum strain range of the solder joint is determined using formulas developed by Engelmaier. The stresses on the solder joint are determined by using a simplified structural model that accounts for the various stiffnesses of the structure. These strain and stress results are then used to determine the strain energy dissipated by the solder joint. The strain energy was then used to make life predictions using equations developed by Syed [6] and Dasgutpa [7]. These time-to-failure predictions are then compared to existing accelerated test data, which allowed for the calibration of model constants.

INTRODUCTION

One of the original assumptions of simple distance to neutral point solder reliability models is that of complete stress relaxation, i.e. the differential expansion between the part and the printed wiring board is directly related to the shear strain in the solder joint. After many years of experience with SnPb solders it has been proven to provide fairly good thermal cycling fatigue predictions. However, due to the increased stiffness of SnAgCu solder this is unlikely to provide adequate and may yield overly conservative life predictions. The primary goal of this study is to generate a simplified DNP model that accounts for the increased stiffness of the Pb-free solder.

The model is broken down into four portions, a solder shear stress equation, a solder strain range computation, a strain energy computation and a solder fatigue equation. The solder shear stress equation is used to determine the amount of shear stress available to drive the deformation of the solder joint during temperature cycling. The solder strain range computation is then used to convert that stress, along with the thermal cycling details (temperature, dwell times) to determine the strain energy per thermal cycle. This strain energy is used in a solder fatigue equation to determine the number of cycles to failure.

MODEL DEVELOPMENT

Solder Shear Stress Computations

The structure of the component attached to the printed wiring board is represented by a combination of axial and shear springs, consisting of:

- Component axial stiffness
- Solder shear stiffness
- Bond-pad shear stiffness
- Printed wiring board bond pad interface stiffness (foundation stiffness)
- Printed wiring board axial stiffness

A schematic representation of the structure is shown in Figure 1. To this structure the global deformation due to the CTE mismatch is applied and the stress in the solder joint is determined using compatibility of displacements. Bending of the substrate and component are ignored since the members are very short (aspect ratios less than 10), and will have axial and shear deformations dominating.

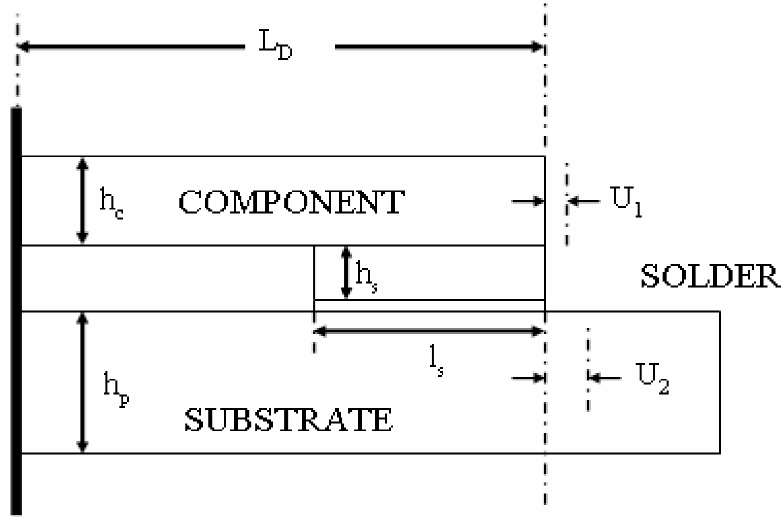

Figure 1: Simplified Structure

The component displacement due to a temperature rise is shown in Equation 1.

$$U_1 = \alpha_1 \cdot \Delta T \cdot L_D + \frac{FL_D}{E_1 A_1}$$

Equation 1: Component displacement equation

Where U_1 is the displacement, α_1 is the coefficient of thermal expansion (CTE), ΔT temperature change, L_D is one-half the component length, F is the force, E_1 is the elastic modulus of component and A_1 is the cross-sectional area of the component. The cross-sectional area of the component is its thickness, h_c multiplied by its width.

The board displacement due to a temperature rise is shown in Equation 2.

$$U_2 = \alpha_2 \cdot \Delta\theta \cdot L_D - \frac{FL}{E_2 A_2}$$

Equation 2: Board displacement

Where U_2 is the displacement, α_2 is the CTE, ΔT temperature change, F is the force, E_2 is the elastic modulus of printed wiring board, and A_2 is the cross-sectional area of the printed wiring board. The area of the board is calculated by multiplying the thickness, h_p by two times the bond pad width.

Deformation of the interconnect for a given shear force - F, the interconnect includes the effect of the solder, copper and board interface stiffness and is computed using Equation 3.

$$U_i = \frac{Fh_s}{A_s G_s} + \frac{Fh_b}{A_b G_b} + F\left(\frac{2-\nu}{9 \cdot G_p a}\right)$$

Equation 3: Interconnect displacement equation

Where U_i is the displacement, h_S is the solder joint thickness (assumed to be 4 mils), A_S is the effective solder joint area, G_S is solder shear modulus, A_b is the copper bond pad area, h_b is the copper thickness (0.035 mm), G_b is the copper shear modulus. The additional equation represents the effective foundation stiffness of the bond-pad to PWB interface and is the shear stiffness of a rigid square on a half space [1, 2], where ν is the Poisson's ratio and G_p is the shear modulus of the printed wiring board and a is one half the side length of the bond pad.

The force F can then be solved for using the following compatibility equation shown in Equation 4.

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L_D = F \cdot \left(\frac{L_D}{E_1 A_1} + \frac{L_D}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_b}{A_b G_b} + \left(\frac{2-\nu}{9 \cdot G_b a}\right)\right)$$

Equation 4: Displacement compatibility equation

The shear stress on the solder is then calculated by dividing the force by the effective area of the solder joint. The effective solder joint area, A_S is assumed to be 75% of the pad area.

Solder Strain Calculations

The shear strain in the solder is computed using equations developed by Werner Engelmaier for leadless components. This is then multiplied by the previously calculated shear stress to determine the cyclic strain energy. The basic calculation for strain range is shown in Equation 5.

$$\Delta\gamma = C \frac{L_D}{h_s} \Delta\alpha \Delta T$$

Equation 5: Strain range calculation [3]

Where C is 0.5, an empirical correction factor, L_D is ½ the length of the component, h_s is the solder joint height (assumed to be 0.1016 mm or 4 mils), and $\Delta\alpha\Delta T$ is the differential thermal expansion between the component and substrate. This strain is assumed to be the maximum strain that can be developed in the solder joint.

Solder Strain Energy Calculations

The strain energy density dissipated during the thermal cycle is assumed to be approximately equal to the formula shown in Equation 6.

$$\Delta W \cong \Delta\gamma \cdot \tau$$

Equation 6: Strain energy density

Life Predictions

The energy dissipated per thermal cycle is used to make fatigue life predictions using damage laws developed by Syed [6]. Syed developed two damage equations for strain energy density based upon two different creep strain rate equations. The one used in this study is based upon the double power law creep model shown in Equation 7.

$$N_f = \left(0.0015 w_{acc}\right)^{-1}$$

Equation 7: Strain energy damage equation [6]

Additional calculations using an energy damage law developed by Zhang and Dasgupta [7] were also done as a comparison. The damage law they proposed is shown in Equation 8.

$$N_f = \left(\frac{w_{acc}}{5920}\right)^{-\frac{1}{1.3}}$$

Equation 8: Strain energy damage equation [7]

VALIDATION

Validation of the model was performed by comparing predictions to experimental findings from available publications.

Failure Data

Data on the thermal cycling behavior of leadless chip resistors attached with SnAgCu is outlined in Table 1. This data was plotted and is displayed as a function of component size and temperature cycle in Figure 2 through Figure 4. All datasets cited in Table 1, except for Franhofer used a SnAgCu alloy with an elevated silver content (3.9 or 3.8). Based on recent data published by IPC, providing that the SnAgCu composition is between Sn3.9Ag0.7Cu and Sn3.0Ag0.5Cu, the time to failure behavior during temperature cycling seems to be relatively insensitive to the exact alloy content.

Comparing the information retrieved from the various papers can be difficult as a number of experimental designs were setup to assess the influence of parameters separate from the component, interconnect or environment. For example, the dataset from Woodrow (reference 9) included varying the Pb-free solderability plating between immersion silver (ImAg), organic solderability preservative (OSP), and electroless nickel/immersion gold (ENIG). A similar effort was made by Schubert (reference 17). Other non-environmental drivers investigated included cooling rates (reference 13) and the number of reflows (reference 16).

Table 1: Time to failure data for thermally cycled leadless chip resistors attached with SnAgCu solder

Organization	Ref	Size	Min Temp	Max Temp	Ramp	Dwell	Eta	Beta
Auburn	8	2512	-40°C	125°C	20 min	20 min	5114	2.839
Auburn	8	2512	-40°C	150°C	20 min	20 min	2158	2.819
Boeing	9	1206	-55°C	125°C	25 min	15 min	3866	1.975
Boeing	9	1206	-55°C	125°C	25 min	15 min	5015	2.201
Boeing	9	1206	-55°C	125°C	25 min	15 min	4523	2.274
Motorola	10	2512	0°C	100°C	15 min	15 min	3063	2.836
Motorola	10	2512	-40°C	125°C	15 min	15 min	752	4.391
Motorola	10	2512	-55°C	125°C	10 sec	5 min	681	3.950
Sanmina	11	2512	-40°C	125°C	15 min	5 min	1374	1.696
U. of Toronto	12	2512	0°C	100°C	7 min	5 min	3634	3.823
U. of Toronto	12	2512	0°C	100°C	1 min	5 min	3993	3.909
U. of Toronto	12	2512	-40°C	125°C	1.5 min	5 min	1089	5.646
U. of Toronto	13	2512	0	100°C	7 min	5 min	5958	3.484
U. of Toronto	13	2512	0	100°C	7 min	5 min	4425	2.548
U. of Toronto	14	2512	0	100°C	10 min	6 min	3350	4.65
NPL	15	2512	-55°C	125°C	N/A	N/A	1450	2.4
NPL	16	1206	-55°C	125°C	18 min	5 min	3403	3.528
NPL	16	1206	-55°C	125°C	18 min	5 min	2513	5.033
Franhofer	17	1206	-40°C	150°C	12 min	12 min	5072	3[1]
Franhofer	17	1206	-40°C	150°C	12 min	12 min	5440	3

[1] Estimated. Eta not provided in original paper

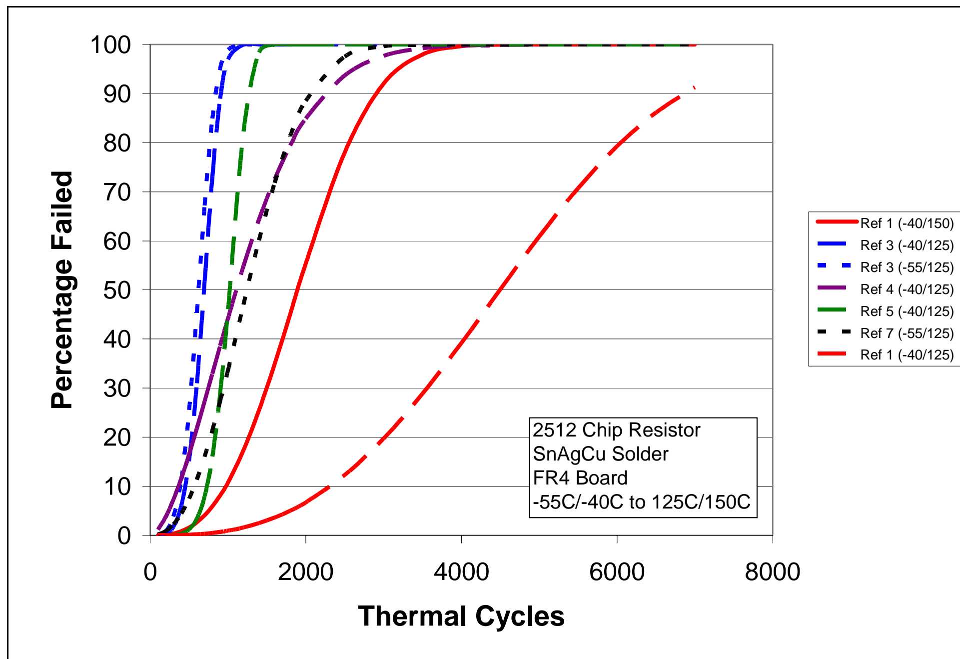

Figure 2: Time to failure for 2512 chip resistors attached with SnAgCu solder and subjected to severe temperature cycles

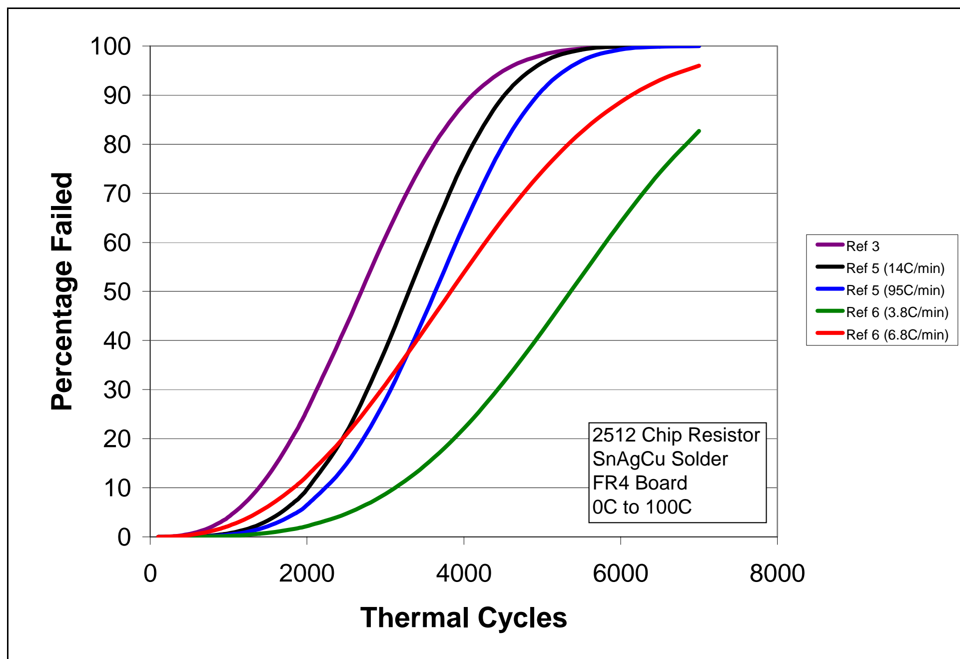

Figure 3: Time to failure for 2512 chip resistors attached with SnAgCu solder and subjected to moderate temperature cycles

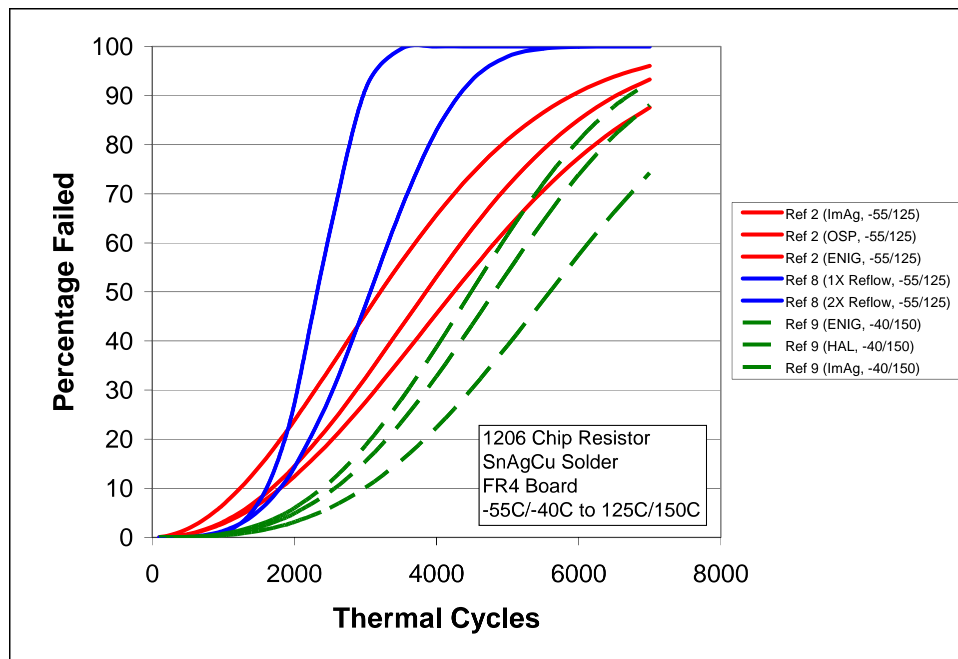

Figure 4: Time to failure for 1206 chip resistors attached with SnAgCu solder and subjected to severe temperature cycling

Several preliminary findings were derived from an initial review of the validation data. Ramp rates were found to have a relatively negligible impact on time-to-failure when compared across several datasets. In addition, thermal cycles with a maximum temperature above 125°C did not consistently result in a shorter lifetime. This may suggest that the current standard of maintaining temperatures below 125°C during accelerated testing of SnPb solder interconnections may also be valid for SnAgCu solder interconnections. In the same regards, thermal cycles with minimum temperatures below -40°C did also not seem to reduce the time to failure significantly. Other drivers, such as solderability plating and cooling rates, were also found to have a negligible or secondary effect when compared to environmental and component parameters.

These findings should only be considered preliminary as there are two major limitations to the datasets that were identified. The first limitation was that none of the publications provided all test parameters necessary to assess the relevancy of the time to failure information. Data that was found to be absent included board thickness, board coefficient of thermal expansion (CTE), procedure for monitoring failure, number of samples tested, number of samples failed, and validation that failures were not at other locations (such as vias). And almost all the publications failed to provide details on the solder volume, such as board bond pad dimensions, stencil thickness, or solder joint height. This absence of data can be critical, as all predictive models for long-term reliability of SnAgCu solder depend on test results to validate their output. Lack of reliable data can result in a lack of reliable end-of-life models and should drive professional organizations, such as SMTA, IEEE, IPC, and IMAPS, to consider a global specification on required data formats when reporting the results of reliability testing.

The second limitation was the lack of repeatability. Repeatability and reproducibility (R&R) have become a standard practice in manufacturing to ensure a sufficient level of quality control. While the cost and time associated with temperature cycling to failure can definitively hinder the implementation of R&R, it should be strongly considered as a review of the literature seems to identify several examples of test data that do not correlate with test results from other publications and may not be repeatable.

Validation Example

Two components were studied to compare the model predictions to the failure data, a 2512 and a 1206 ceramic resistor. The material properties for various parts of the assembly were assumed to be the values shown in Table 2, which are typical of values found in literature.

Table 2: Material Properties

Material	Elastic Modulus (MPa)	Shear Modulus (MPa)	Poisson's Ration	Coefficient of Thermal Expansion (°C/ppm)
SnAgCu	50000	21200	0.36	20
Alumina	300000	115400	0.3	6
FR-4	17000	7200	0.18	16
Copper	120000	44117	0.3	21

The geometric variables (component dimensions) used in the model are shown in Table 3.

Table 3: Geometric Variables

Variable	2512 Resistor	1206 Resistor
Component		
Length	6.35 mm	3.05 mm
Width	3.05 mm	1.52 mm
Thickness	1.5 mm	1.2 mm
Copper Bond Pad		
Thickness	0.035 mm	0.035 mm
Length	2 mm	1.5 mm
Width	3.05 mm	1.52 mm
Printed Wiring Board		
Thickness	1.6 mm	1.6 mm
Solder Joint		
Length	1.5 mm	1.125 mm
Width	3.05 mm	1.52 mm
Thickness	0.1016 mm	0.1016 mm

Some typical results for the solder shear stress, inelastic strain energy and life predictions are shown in Table 4 for a -55 to 125°C thermal cycle.

Table 4: Model Results

Component	2512	1206
ΔT	180	180
$\Delta\gamma$	0.0225	0.0108
τ	20.3 MPa	19.9 MPa
ΔW	0.572	0.269
N_f [6]	1315 cycles	2792 cycles
N_f [7]	1382 cycles	2468 cycles

As shown in the table the maximum stress developed in the solder joint only decreases slightly as the component size shrinks.

A comparison of predictions from the DfR reliability model and experimental data from Table 1 is displayed in Figure 5. The data shows a very strong fit to the predictive results, especially considering that no iterative fitting to the data was performed before this comparison was performed. Three data points lie outside the 2X banding, two of which correspond to thermal cycling that were conducted up to 150°C, which may be close to or beyond the glass transition temperature of the circuit board; the one data point that falls well away from the 2X band is from reference 1. Comparing the results from this reference to other results from other organizations, as shown in Figure 2, seems to suggest that some unknown aspect of the test setup or conditions resulted in unexpectedly much longer times to failure.   Both the energy models gave adequate life predictions.

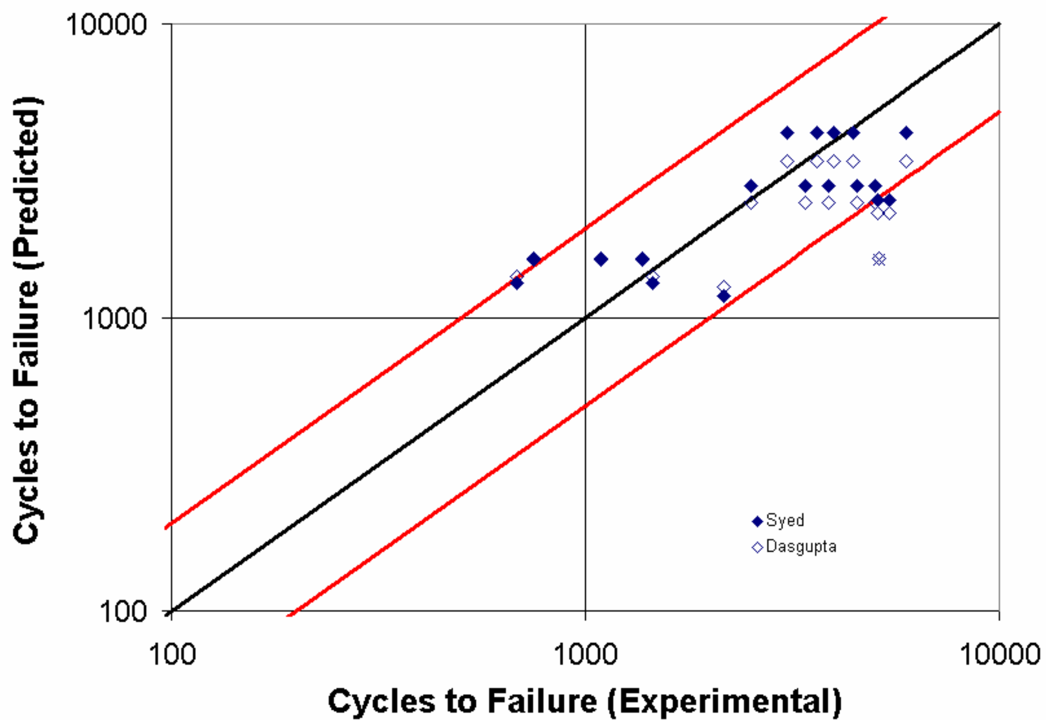

Figure 5: Validation of DfR end-of-life model for thermally cycled leadless chip components (red lines indicate 2X bands)

DISCUSSION

As shown by the results the model provides a relatively good estimate of the fatigue behavior of the leadless chip resistors as a function component size and thermal cycle for SnAgCu using calculations that can be easily implemented into a spreadsheet or simple calculator. This model adds in the effect of the printed wiring board to solder bond pad by using a foundation shear stiffness equation. An example of the life predictions for a 2512 resistor at various temperature deltas is shown in Figure 6.

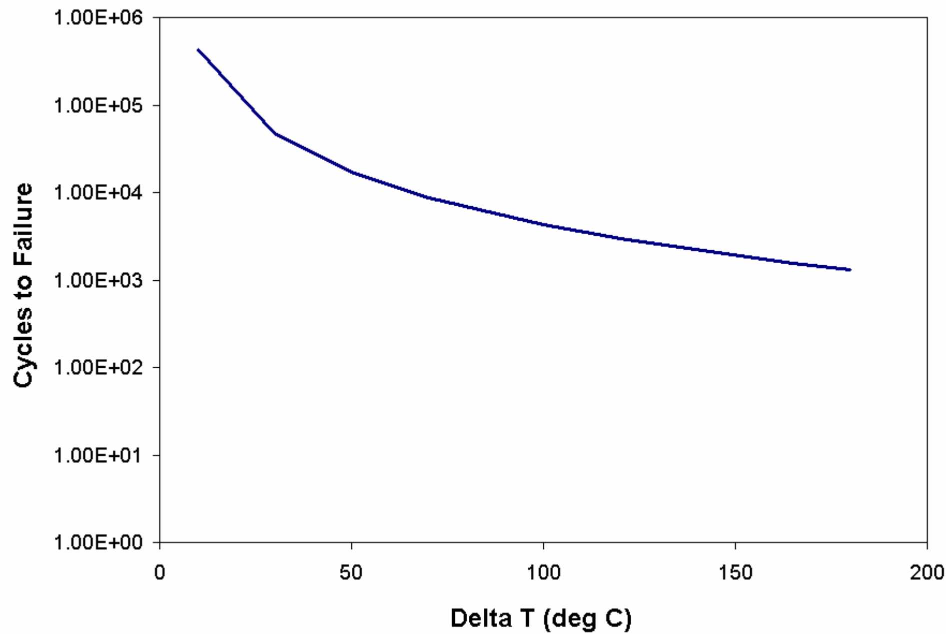

Figure 6: Life predictions for 2512 resistor as a function of delta T

The model is currently undergoing minor modifications to account for dwell times. Additional work is being done to check the sensitivity of the model to various geometric parameters and some modification to the strain range calculation may be implemented. Additional work in using the stress calculation for doing 2nd order predictions is also planned so that stress strain hysteresis loops can be generated for improved strain energy calaculations.

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