Manufacturing and Reliability Challenges With QFN

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What is ‘Next Generation’ Technology?
- Materials or designs currently being used, but not widely adopted (especially among hi-rel manufacturers)

Carbon nanotubes are not ‘Next Generation’
- Not used in electronic applications

Ball grid array is not ‘Next Generation’
- Widely adopted
Introduction (cont.)

- Why is knowing about ‘Next Generation’ Technologies important?
- These are the technologies that you or your supply chain will use to improve your product
  - Cheaper, Faster, Stronger, ‘Environmentally-Friendly’, etc.
- And sooner then you think!
One of the most common drivers for failure is inappropriate adoption of new technologies
- The path from consumer (high volume, short lifetime) to high rel is not always clear

Obtaining relevant information can be difficult
- Information is often segmented
- Focus on opportunity, not risks

Can be especially true for component packaging
- BGA, flip chip, QFN
Most of us have little influence over component packaging

- Most devices offer only one or two packaging styles

Why should you care?

- Poor understanding of component qualification procedures
- Who tests what and why?
Reliability testing performed by component manufacturers is driven by JEDEC
- JESD22 series (A & B)

Focus is almost entirely on die, packaging, and 1st level interconnections (wire bond, solder bump, etc.)

Only focus on 2nd level interconnects (solder joints) is JESD22-B113 Cyclic Bend Test
- Driven by cell phone industry
- They have little interest in thermal cycling or vibration!
IPC has attempted to rectify this through IPC-9701

Two problems
- Adopted by OEMs; not by component manufacturers
- Application specific; you have to tell them the application (your responsibility, not theirs)

The result
- An increasing incidence of solder wearout in next generation component packaging
Solder Wearout in Next Gen Packaging

Performance Needs

- Higher frequencies and data transfer rates
  - Lower resistance-capacitance (RC) constants
- Higher densities
  - More inside less
- Lower voltage, but higher current
  - Joule heating is $I^2R$
- Has resulted in less robust package designs
Solder Wearout (cont.)

- Elimination of leaded devices
  - Provides lower RC and higher package densities
  - Reduces compliance

Cycles to failure
-40 to 125°C

QFP: >10,000

BGA: 3,000 to 8,000

CSP / Flip Chip: <1,000

QFN: 1,000 to 3,000
- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)
Solder Wearout (cont.)

- Hotter devices
  - Increases change in temperature ($\Delta T$)

\[ t_f = \Delta T^n \]

- $n = 2$ (SnPb)
- $n = 2.3$ (SnNiCu)
- $n = 2.7$ (SnAgCu)
Industry Response to SJ Wearout?

- **JEDEC**
  - Specification body for component manufacturers
- **JEDEC JESD47**
  - Guidelines for new component qualification
  - Requires **2300** cycles of 0 to 100°C
  - Testing is often done on thin boards
- **IPC**
  - Specification body for electronic OEMs
- **IPC 9701**
  - Recommends **6000** cycles of 0 to 100°C
  - Test boards should be similar thickness as actual design
BIG PROBLEM

- JEDEC requirements are 60% less than IPC
- Testing on a thin board can extend lifetimes by 2X to 4X

What does this mean?
- The components you buy may only survive 500 cycles of 0 to 100°C

What must you do?
- Components at risk must be subjected to PoF-based reliability analysis
Quad Flat Pack No-Lead (QFN)
QFN: What is it?

- **Quad Flat Pack No Lead or Quad Flat Non-Leaded**
  - ‘The poor man’s ball grid array’
  - Also known as
    - Leadframe Chip Scale Package (LF-CSP)
    - MicroLeadFrame (MLF)
    - Others (MLP, LPCC, QLP, HVQFN, etc.)

- Overmolded leadframe with bond pads exposed on the bottom and arranged along the periphery of the package
  - Developed in the early to mid-1990’s by Motorola, Toshiba, Amkor, etc.
  - Standardized by JEDEC/EIAJ in late-1990’s
  - Fastest growing package type
Availability
- 1 x 2 mm (3 leads) to 14 x 14 mm (120 leads)
- Dual row may increase I/O count to above 150

Expected to dominate lead counts between 8 to 68
- Obsolescence of QFP and SOP?

Numerous package outline versions (JEDEC)
- MO-196 (1998)
- Available in two and four-sided

Other variations
- Singulated and sawed
- Single row and dual row
QFN Advantages: Size and Cost

- Smaller, lighter and thinner than comparable leaded packages
  - Allows for greater functionality per volume

- Reduces cost
  - Component manufacturers: More ICs per frame
  - OEMs: Reduced board size

- Attempts to limit the footprint of lower I/O devices have previously been stymied for cost reasons
  - BGA materials and process too expensive
Advantages: Manufacturability

- Small package without placement and solder printing constraints of fine pitch leaded devices
  - No special handling/trays to avoid bent or non planar pins
  - Easier to place correctly on PCB pads than fine pitch QFPs, TSOPs, etc.
  - Larger pad geometry makes for simpler solder paste printing
  - Less prone to bridging defects when proper pad design and stencil apertures are used.

- Reduced popcorning moisture sensitivity issues – smaller package
Advantages: Thermal Performance

- More direct thermal path with larger area
  - Die → Die Attach → Thermal Pad → Solder → Board Bond Pad

- $\theta_{Ja}$ for the QFN is about half of a leaded counterpart (as per JESD-51)
  - Allows for 2X increase in power dissipation

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Body Size (mm)</th>
<th>Leads</th>
<th>Height (mm)</th>
<th>Max Die Size</th>
<th>PCB Area</th>
<th>$\theta_{Ja}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN</td>
<td>7 x 7</td>
<td>48</td>
<td>1.00 max</td>
<td>203 x 203 mils</td>
<td>49 mm$^2$</td>
<td>27</td>
</tr>
<tr>
<td>TQFP</td>
<td>7 x 7</td>
<td>48</td>
<td>1.20 max</td>
<td>190 x 190 mils</td>
<td>81 mm$^2$</td>
<td>55</td>
</tr>
<tr>
<td>QFN</td>
<td>5 x 7</td>
<td>38</td>
<td>1.00 max</td>
<td>124 x 202 mils</td>
<td>35 mm$^2$</td>
<td>34</td>
</tr>
<tr>
<td>TSSOP</td>
<td>4.4 x 9.7</td>
<td>38</td>
<td>1.10 max</td>
<td>108 x 207 mils</td>
<td>62 mm$^2$</td>
<td>73</td>
</tr>
<tr>
<td>QFN</td>
<td>5 x 5</td>
<td>16</td>
<td>1.00 max</td>
<td>124 x 124 mils</td>
<td>25 mm$^2$</td>
<td>37</td>
</tr>
<tr>
<td>QSOP</td>
<td>3.9 x 4.9</td>
<td>16</td>
<td>1.75 max</td>
<td>86 x 120 mils</td>
<td>31 mm$^2$</td>
<td>112</td>
</tr>
</tbody>
</table>
Advantages: Inductance

- At higher operating frequencies, inductance of the gold wire and long lead-frame traces will affect performance.

- Inductance of QFN is half its leaded counterpart because it eliminates gullwing leads and shortens wire lengths.

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Table 1. Comparison of inductance components for a QFN and SOIC.

<table>
<thead>
<tr>
<th>Component</th>
<th>QFN 7 mm, 48 Lead</th>
<th>TQFP 7 mm, 48 Lead</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>0.067</td>
<td>0.871</td>
</tr>
<tr>
<td>Die size 4.5 x 4.5 mm</td>
<td>0.867</td>
<td>0.837</td>
</tr>
<tr>
<td>Center lead</td>
<td>0.934</td>
<td>1.708</td>
</tr>
<tr>
<td>Center wire</td>
<td>0.085</td>
<td>1.010</td>
</tr>
<tr>
<td>Corner lead total (lead + wire)</td>
<td>1.081</td>
<td>0.964</td>
</tr>
</tbody>
</table>

QFN: Why Not?

- QFN is a ‘next generation’ technology for non-consumer electronic OEMs due to concerns with
  - Manufacturability
  - Compatibility with other OEM processes
  - Reliability

- Acceptance of this package, especially in long-life, severe environment, high-rel applications, is currently limited as a result
QFN Manufacturability (Bond Pads)

- Non Solder Mask Defined Pads Preferred (NSMD)
  - Copper etch process has tighter process control than solder mask process
  - Makes for more consistent, strong solder joints since solder bonds to both tops and sides of pads

- Use solder mask defined pads (SMD) with care
  - Can be used to avoid bridging between pads, especially between thermal and signal pads.
  - Pads can grow in size quite a bit based on PCB mfg capabilities

- Can lose solder volume through vias in thermal pads
  - May need to tent vias to keep sufficient paste volume
  - Tenting vias is often not well controlled and can lead to placement and chemical entrapment issues
  - Exercise care with devices placed on opposing side of QFN
  - Can create placement issues if solder “bumps” are created in vias
  - Can create solder short conditions on the opposing device
Bond Pads (cont.)

- Extend bond pad 0.2 – 0.3 mm beyond package footprint
  - May or may not solder to cut edge
  - Allows for better visual inspection

- Really need X-ray for best results
  - Allows for verification of bridging, adequate solder coverage and void percentage
  - Note: Lacking in good criteria for acceptable voiding
Manufacturability (Rework)

- Can be difficult to replace a package and get adequate soldering of thermal / internal pads.
  - Mini-stencils or rebump techniques can be used to get sufficient solder volume

- Not directly accessible with soldering iron and wire
  - Portable preheaters used in conjunction with soldering iron can simplify small scale repair processes

- Close proximity with capacitors often requires adjacent components to be resoldered / replaced as well
Stencil thickness and aperture design can be crucial for manufacturability

- Excessive amount of paste can induce float, lifting the QFN off the board
- Excessive voiding can also be induced through inappropriate stencil design

Follow manufacturer’s guidelines

- Goal is 2-3 mils of solder thickness

Rules of thumb (thermal pad)

- Ratio of aperture/pad ~0.5:1
- Consider multiple, smaller apertures (avoid large bricks of solder paste)
- Reduces propensity for solder balling
QFN solder joints are more susceptible to dimensional changes

Case Study: Military supplier experienced solder separation under QFN

QFN supplier admitted that the package was more susceptible to moisture absorption that initially expected
- Resulted in transient swelling during reflow soldering
- Induced vertical lift, causing solder separation

Was not popcornning
- No evidence of cracking or delamination in component package
Area array devices are known to have board flexure limitations
- For SAC attachment, maximum microstrain can be as low as 500 ue

QFN has an even lower level of compliance
- Limited quantifiable knowledge in this area
- Must be conservative during board build
- IPC is working on a specification similar to BGAs
Reliability (Thermal Cycling)

- Order of magnitude reduction in time to failure from QFP
  - 3X reduction from BGA
- Driven by die / package ratio
  - 40% die; tf = 8K cycles (-40 / 125C)
  - 75% die; tf = 800 cycles (-40 / 125C)
- Driven by size and I/O#
  - 44 I/O; tf = 1500 cycles (-40 / 125C)
  - 56 I/O; tf = 1000 cycles (-40 / 125C)
- Very dependent upon solder bond with thermal pad

QFP: >10,000
BGA: 3,000 to 8,000
QFN: 1,000 to 3,000
Thermal Cycling (Conformal Coating)

- Care must be taken when using conformal coating over QFN
  - Coating can infiltrate under the QFN
  - Small standoff height allows coating to cause lift
- Hamilton Sundstrand found a significant reduction in time to failure (-55 / 125°C)
  - Uncoated: 2000 to 2500 cycles
  - Coated: 300 to 700 cycles
- Also driven by solder joint sensitivity to tensile stresses
  - Damage evolution is far higher than for shear stresses

Wrightson, SMTA Pan Pac 2007
Low degree of compliance and large footprint can also result in issues during cyclic flexure events.

Example: IR tested a 5 x 6mm QFN to JEDEC JESD22-B113

- Very low beta (~1)
- Suggests brittle fracture, possible along the interface
Reliability (Dendritic Growth)

- Large area, multi-I/O and low standoff can trap flux under the QFN
- Processes using no-clean flux should be requalified
  - Particular configuration could result in weak organic acid concentrations above maximum (150 – 200 ug/in²)
- Those processes not using no-clean flux will likely experience dendritic growth without modification of cleaning process
  - Changes in water temperature
  - Changes in saponifier
  - Changes to impingement jets
The electric field strength between adjacent conductors is a strong driver for dendritic growth
  - Voltage / distance

Digital technology typically has a maximum field strength of 0.5 V/mil
  - TSSOP80 with 3.3VDC power and 16 mil pitch

Previous generation analog / power technology had a maximum field strength of 1.6 V/mil
  - SOT23 with 50VDC power and 50 mil pitch

Introduction of QFN has resulted in electric fields as high as 3.5 V/mil
  - 24VDC and 16 mil pitch
Some component manufacturers are aware of this issue and separate power and ground

- Linear Technologies (left) has strong separation power and ground
- Intersil (right) has power and ground on adjacent pins
QFN: Risk Mitigation

- Assess manufacturability
  - Degree of reflow profiling
  - Control of board flexure
  - DOE on stencil design
  - Dual row QFN is especially difficult

- Assess reliability
  - Ownership of 2nd level interconnect is often lacking
  - Extrapolate to needed field reliability
  - Some companies have reballed QFN to deal with concerns