Preventing Pad Cratering During ICT Using Sherlock

DfR Solutions Webinar

November 21, 2013
Pad Cratering

- Pad cratering is defined as cracking which initiates within the laminate during a dynamic mechanical event such as In Circuit Testing (ICT), board depanelization, connector insertion, and other shock and vibration inducing activities.

- Simulation can be used to prevent this serious but prevalent failure. Pad cratering was first recognized in BGA packages but newer leadless, bottom termination components are also vulnerable.
Pad Cratering: Strain & Flexure

- Cracking initiating within the PCB laminate during a dynamic mechanical event
  - In circuit testing (ICT), board depanelization, connector insertion, shock and vibration, etc.
Laminate Cracking Leads to Trace Fracture

Trace routed externally

Functional failure will occur

Bending Force
Pad Cratering

- **Drivers**
  - Finer pitch components
  - More brittle laminates
  - Stiffer solders (SAC vs. SnPb)
  - Presence of a large heat sink
  - Location
  - PCB thickness
  - Component size & rigidity
  - Temperatures & cooling rates

- **Difficult to detect using standard procedures**
  - X-ray, dye-n-pry, ball shear, and ball pull
Is Pad Cratering a Pb-Free Issue? No, but…

Table 4. Board displacements until solder joint open failure as a function of joint material combination.

<table>
<thead>
<tr>
<th>Solder ball</th>
<th>SnPb</th>
<th>SnAgCu</th>
<th>SnAgCu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder paste</td>
<td>SnPb</td>
<td>SnAgCu</td>
<td>SnPb</td>
</tr>
<tr>
<td>Avg.</td>
<td>0.808</td>
<td>0.740</td>
<td>0.783</td>
</tr>
<tr>
<td>Max.</td>
<td>0.898</td>
<td>0.854</td>
<td>0.960</td>
</tr>
<tr>
<td>Min.</td>
<td>0.669</td>
<td>0.617</td>
<td>0.630</td>
</tr>
</tbody>
</table>

Speed: 5mm/min (or 2.5mm/min)
BGA Mechanical Loading Failure Modes

- Weakest link in the system fails first

**Different Failure Modes**

- **Legend**
  - A: Package Pad Lift/Crater
  - B: Pkg Metal/IMC Interface Fracture
  - C: Pkg IMC/Solder Interface Fracture
  - D: Bulk Solder Fracture
  - E: PWB IMC/Solder Interface Fracture
  - F: PWB Metal/IMC Interface Fracture
  - G: PWB Pad Lift/Cratering

- **Diagram**
  - Package Substrate
  - Solder Ball
  - PCB
**IPC 9708**

- **Failure Modes Defined**

<table>
<thead>
<tr>
<th>Mode</th>
<th>Type</th>
<th>Description</th>
<th>Illustration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ductile Failure [Not Desired for Pad Cratering Testing]</td>
<td>Solder ball fracture at or above the surface of the solder mask within the bulk solder material. This failure mode is not desirable for this test method, because it does not include pad cratering failure in the test sample.</td>
<td><img src="image1.png" alt="Illustration" /></td>
</tr>
<tr>
<td>2</td>
<td>Pad Lift [Not Desired for Pad Cratering Testing]</td>
<td>Solder pad lifts with solder ball; lifted pad may include ruptured base material. This failure mode is an adhesive type of failure, as opposed to pad cratering, which is a cohesive failure mode within the dielectric.</td>
<td><img src="image2.png" alt="Illustration" /></td>
</tr>
<tr>
<td>3</td>
<td>Interfacial Separation [Not Desired for Pad Cratering Testing]</td>
<td>The separation is at the solder/intermetallic interface or intermetallic/base metal interface. The interfacial fracture may extend across the entire pad or be the dominant failure mode.</td>
<td><img src="image3.png" alt="Illustration" /></td>
</tr>
<tr>
<td>4</td>
<td>Conductor Cracks</td>
<td>The PBA pad is lifted, but is still partially attached to the conductor.</td>
<td><img src="image4.png" alt="Illustration" /></td>
</tr>
<tr>
<td>5</td>
<td>Crater with Glass Fibers Exposed</td>
<td>The PBA pad is cratered, and the underlying glass fibers are exposed.</td>
<td><img src="image5.png" alt="Illustration" /></td>
</tr>
<tr>
<td>6</td>
<td>Crater with no Glass Fibers Exposed</td>
<td>The PBA pad is cratered, the underlying resin is exposed, but no glass fibers are visible.</td>
<td><img src="image6.png" alt="Illustration" /></td>
</tr>
<tr>
<td>7</td>
<td>Crater with via exposed</td>
<td>The PBA pad is cratered, and a via central to the pad is exposed. This failure mode is only applicable to test pads with plated vias in the pads.</td>
<td><img src="image7.png" alt="Illustration" /></td>
</tr>
<tr>
<td>8</td>
<td>Combined Failures</td>
<td>These are failure modes where partial amounts of Modes 1-7 can be observed. In this case, each failure mode present in a given test pad shall be documented.</td>
<td><img src="image8.png" alt="Illustration" /></td>
</tr>
</tbody>
</table>

Refer to Table 3-8

**NA**
IPC 9704

- No pass / fail limits
- 3 strain limit approaches
  - Component supplier provided
  - Customer specified
  - Rate limited
    - Maximum allowable strain versus rate and PCB thickness
Detecting Pad Cratering

- CalPoly study showing failure of electrical testing to capture all defects

Board Level Failure Analysis of Chip Scale Package Drop Test Assemblies, 2008 International Microelectronics And Packaging Society.
Majority of failures occur at corners of packages: locations of stress & strain concentrations

Board Level Failure Analysis of Chip Scale Package Drop Test Assemblies, 2008 International Microelectronics And Packaging Society.
Pad Cratering Failure Analysis

- Difficult to detect using standard procedures
  - Companies frequently unaware of pad cratering until failure happens
    - Recalls have been common and painful!

- Potential warning signs:
  - Excessive BGA repair rate
  - High percentage of “defective” BGAs
  - High rate of “retest to pass” at in circuit test (ICT)

- New X-ray potential with 3D m-CT inspection
- Precision cross-sections are required to confirm
Potential Mitigations to Pad Cratering

- Design
  - Non-critical pads
  - Solder mask defined vs. non-solder mask defined
  - Pad Geometry
  - Layout & PCB thickness

- Corner Glue

- More compliant solder
  - SAC305 is relatively rigid, SAC105 and SNC are possible alternatives

- New laminate acceptance criteria and materials

Best Mitigation! – Avoid the problem by not overstressing the interconnect

- Limitations on board flexure
  - Simulation to predict the strains induced during ICT and highlight potential problems
  - 750 to 500 microstrain, component and layout dependent
  - Process Control & Validation
ICT Strain: Fixture & Process Analysis

- Review/perform ICT strain evaluation at fixture supplier and in process:
  - 500 µs rule of thumb, critical for BTCs, CSP, and BGA packages

  - To reduce the pressures exerted on the PCB:
    - First and simplest solution: reduce the probe forces when possible.
    - Secondly, optimize position of the fingers/stoppers to control probe forces.
    - Often difficult to achieve. Mechanically, the stoppers must be located exactly under the pressure fingers to avoid the creation of shear points.
Eliminate potential bed of nails (ICT) damage by:

- Identifying components on the circuit card that could experience cracking or failure during bed of nails testing.
- Prior to the ICT, the designer can optimize the process:
  - Change test points
  - Change pogo pin pressure, or
  - Add / move board supports

Sherlock analysis is component-specific, allowing for more precise identification of at-risk areas.
Designers can identify potential bed of nails damage early in the layout process, before a bed of nails tester is ever designed.

Allows for tradeoff analyses, saving costly board damage and redesign.
Setup Test Points and Fixtures

- Test points are automatically loaded if defined in pick and place or the odb++ archive
- Fixture locations can also be imported
Test Point Modification
ICT Fixtures

- Guide Pins (mount hole) constrained in-plane (x,y) but can move up and down
- Support pin just constrained in the Z direction
Finite Element Mesh
Displacement
Strain Results
Component Risk
Pad Cratering Conclusions

- Pad Cratering is an increasingly common failure mode
  - Catastrophic and non-reworkable
- Easy to avoid detection and difficult to diagnose
  - Partial cracks riskiest since they escape and expand in the field
- Multiple paths for mitigation
  - Few for true prevention
  - Best mitigation is to reduce board level strains
- No hard, fast rules for avoidance
  - Dependent on design, component, layout, process...
  - Simulation can be used to quantify the strains associated with ICT