THE RELIABILITY CHALLENGES OF QFN PACKAGING

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ABSTRACT
The quad flat pack no lead or quad flat non-leaded (QFN) is one of the fastest growing package types in the electronics industry today. While the advantages of QFNs are well documented, concerns arise with its reliability and manufacturability. Acceptance of this package, especially in long-life, severe-environment, high-reliability applications, is currently limited. One of the most common drivers for reliability failures is inappropriate adoption of new technologies, such as the case with QFN. In this presentation, we will review and discuss QFN related reliability concerns and challenges, and propose Physics-of-Failure (PoF) based approaches to allow the confident introduction of QFN components into electronics products.

Key words: QFN, reliability, physics-of-failure

INTRODUCTION
One of the most common drivers for electronics product failure is inappropriate adoption of new technologies. Such technologies may initially appear in high volume consumer industries and later migrate to the high reliability products. However, the migration path is not always clear to achieve the necessary reliability confidence. This is especially true for new component packaging technology. Obtaining relevant information can be difficult since data often are segmented and the focus is on design opportunities not reliability risks.

In order to proactively introduce design-in product robustness, the end-to-end reliability program should start with technology insertion risk assessment. When there is a lack of information, especially due to insufficient industry experiences, Physics-of-Failure (PoF) approach can be particularly advantageous in identifying risks related to next gen technology.

In the present paper, we discuss the reliability challenges associated with quad flat pack no lead (QFN) package, which is one of the fastest growing package types in the electronics industry. While the advantages of QFNs are well documented, they can be considered as a next-generation technology for non consumer-sector OEMs, mostly due to concerns with design and manufacturability, compatibility with other OEM processes, and reliability. Acceptance of this package type, especially in long-life, severe-environment, high-reliability applications, is currently limited as a result. The present paper will focus on reliability discussions.

QFN PACKAGE
The quad flat pack no lead or quad flat non-leaded (QFN) package has been referred to as the poor man's ball grid array (BGA) and is also known as a leadframe chipscale package (LF-CSP), micro-leadframe (MLF), and other names such as MLP, LPCC, QLP, and HVQFN.

As shown in Figure 1, it comprises an overmolded leadframe with bond pads exposed on the bottom and arranged along the periphery of the package in one or two rows. Commonly available in two- or four-sided configurations with either sawed or punched leads, it was developed by multiple component manufacturers in the 1990s and standardized late in the decade by JEDEC/EIAJ.

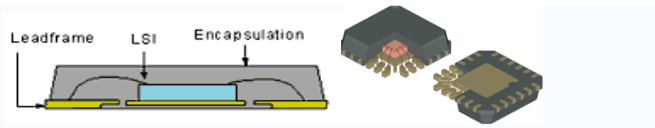

Figure 1. Quad flat pack no lead or quad flat non-leaded (QFN) package

QFN RELIABILITY SITUATION
First of all, there are some quality/reliability advantages associated with QFN. It is a small package without placement and solder printing constraints like fine pitch leaded devices. Thus, there will be no special handling/trays to avoid bent or non planar pins; it is easier to place correctly on PCB pads than, e.g., fine pitch QFPs. It is less prone to bridging defects when proper pad design and stencil apertures are used. The small package also reduces popcorning related to moisture sensitivity issues. In thermal-related reliability, there is more direct thermal path with larger contact area from Die → Die Attach → Thermal Pad → Solder → Board Bond Pad. The typical QFN package thermal impedance is about half of a leaded counterpart.

However, there are major quality and reliability challenges associated with QFN. In a typical thermal cycling test between -40^{o}C to 125^{o}C, a quad flat pack (QFP) package

can stand over 10000 cycles whereas QFN tends to fail between 1000 to 3000 cycles. Most OEMs have little influence over component packaging; most devices offer only one or two packaging styles. Reliability testing performed by component manufacturers is driven by JEDEC (JESD22 series A & B) and the focus is almost entirely on die, packaging, and first-level interconnections (wire bond, solder bump, etc.) The only focus on second-level interconnect (solder joints) within JEDEC is the JESD22-B113 Cyclic Bend Test, which is driven by the cell phone industry.

There has been some attempt to rectify this absence of information through IPC-9701. Unfortunately, the results have been limited, as most component manufacturers are not interested in performing thermal cycling or vibration tests of second-level interconnects. This is either because their primary markets (consumer, computer) are not concerned with these stress environments or they view these issues as "application-specific," which can be translated as "this is your problem, not mine."

It is true there are application specific issues, but industry standard acceptance criteria would help in establishing a baseline for new component selection and qualification purposes. Even when there are test "standards" defined, confusions arise due to different test specifications and execution details. For example, JEDEC JESD47 requires ~**2300** cycles of 0 to 100°C, which is typically carried out on thin boards. However, IPC 9701 would recommend **6000** cycles of 0 to 100°C and the test boards should be similar thickness as the end product. Thus, the JEDEC requirements are 60% less than IPC and testing on a thin board can extend lifetimes by 2X to 4X. The problem is if the selection and qualification are based on a "standard" JEDEC test, the components one acquires may only survive 500 cycles of 0 to 100°C in your actual board.

What can one do? In our view, components at risk can be subjected to Physics-of-Failure (PoF) reliability analysis, which starts with failure mechanism understanding

POF ASSESSMENTS

The PoF approach applies the life-cycle stress and component strength understanding to identify potential failure mechanisms and to prevent operational failures through robust design and manufacturing practices. Reliability assessments based on PoF incorporate reliability into the design process providing a scientific basis for assessing reliability risks under actual operating conditions. For QFNs, we will highlight thermal, mechanical, and chemical stresses and evaluate how QFN reacts under such stresses.

Thermal Stress

An assembly stage thermal stress the QFN will be exposed to is the reflow profile during the soldering process. Here, the QFN package strength is related to its moisture sensitivity, as there are increasing indications that moisture absorption in the thinner QFN package can drive excessive warpage during reflow. In one case study, a military supplier experienced solder separation under QFNs. The QFN supplier admitted that the package was more susceptible to moisture absorption than initially expected. This resulted in transient swelling during reflow soldering, which induced vertical lift and caused solder separation. This was not a popcorning phenomenon since no evidence of cracking or delamination in the component package was seen. To minimize this potential, larger and thinner QFNs should be treated as an MSL of 3 or higher and reflow profiles should be carefully controlled with a slow, steady ramp rate.

A more challenging thermal issue is the thermal cycling stress a QFN component may experience during its operational life. Multiple package design changes have resulted in the increase for solder joint failure in the current generation of electronic parts. The elimination of leads reduces overall joint compliance. As package sizes shrink, there is more silicon and less plastic, increasing the mismatch in the coefficients of thermal expansion (CTE) between the part and printed circuit board (PCB). Parts are running hotter, which increases the change in temperature (ΔT) at the joint.

QFNs are a good example of reduced robustness of second-level interconnects. For example, under standard thermal cycling environments, QFNs can experience an order of magnitude reduction in time to failure (TtF) from quad flat packs (QFPs) and a 3× reduction from ball grid arrays (BGAs)[1]. This reliability reduction is driven by the die-to-package ratio, package size and I/O count, and the integrity of the thermal pad solder joint. In general, as die size, package size, and number of I/O increase, the number of cycles to fail will decrease — sometimes quite dramatically.

Thermal cycling takes on greater significance when QFNs are conformally coated. When coating material infiltrates under the QFN, the small standoff can result in a high stress state in the solder joint when the conformal coating expands during temperature cycling. A recent study[2] found a significant reduction in mean cycles to failure from a -55° to 125°C cycle, with uncoated QFNs failing in ~2,500 cycles and coated QFNs failing in as little as 300 cycles. A number of companies have responded to this by fencing off QFNs during the conformal coating process.

Mechanical Stress

An assembly related mechanical stress is board flexure. Area array devices are known to have board flexure limitations. For SAC alloy attachment, the maximum microstrain can be as low as 500. QFNs have an even lower level of compliance and may be more susceptible to flex-induced joint and laminate cracks. Since there is currently limited quantifiable knowledge in this area, be very conservative during board builds. Special focus should be placed on any in-circuit test (ICT) and depanelization

processes and on hand assembly operations, since these areas typically induce the most strain. The IPC is currently working on a QFN strain specification similar to the one in use for BGAs.

Another likely mechanical stress is cyclic flexure such as experienced during bend cycling and vibration, which may result in issues due to the low degree of lead compliance and relatively large footprint of QFNs. For example, International Rectifier tested a 5 × 6 mm QFN to JEDEC JESD22-B113 (Figure 2). While the characteristic life demonstrated an extensive number of cycles to failure, the very low beta (~1) suggested brittle fracture, which could be an issue for certain environments. Unfortunately, very little test data or analysis is currently available to assess the robustness of QFN packages in these environments.

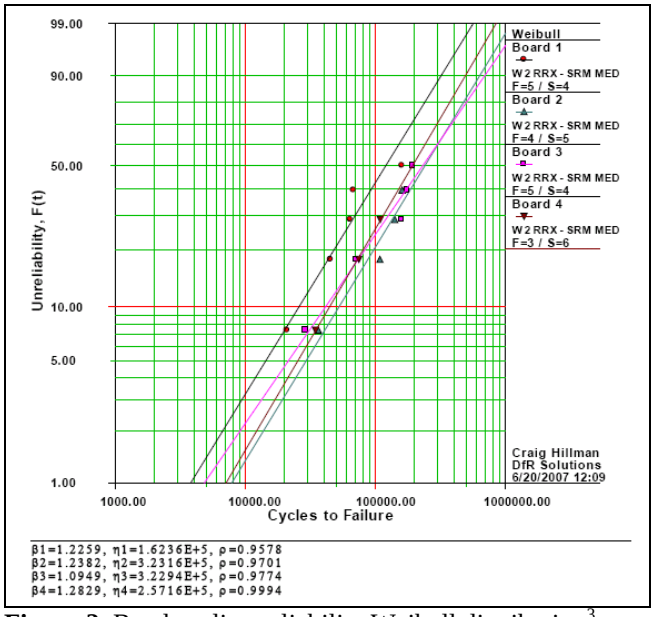

Figure 2. Bend cycling reliability Weibull distribution[3]

Chemical Stress

Large component area, multiple I/Os, and low standoff height can combine to trap flux under QFNs post-reflow. Processes using no-clean fluxes should be re-qualified, since particular design and process configurations could result in weak organic acid concentrations above a maximum (>150 µg/in^2) desired level. Processes not using no-clean fluxes are vulnerable to dendrite growth without cleaning process modifications such as changes in water/solvent temperature, changes in use or style of saponifiers and surfactants, and changes to pressure and location impingement jets.

The electric field strength between adjacent conductors (voltage/distance) is also a strong driver for dendritic growth. Digital technology typically has a maximum field strength of 0.5 V/mil. Previous generation analog/power technology tended to limit field strength to 1.6 V/mil. The introduction of QFNs has increased these maximum electric field strengths, with some components having field strengths as high as 3.5 V/mil. Some component manufacturers are aware of this issue and have modified their designs to maximize the distance between power and ground, while other manufacturers continue to have power and ground on adjacent pins.

CONCLUSION

To create a path for the reliable introduction of QFN components in high-reliability/severe environment applications, designers, component engineers, and reliability personnel must be aware that heuristic rules may be insufficient and more comprehensive testing and analysis are required such as based on PoF. Application-specific reliability analyses and evaluation can be established based on the lifecycle stress and QFN strength assessments. Mitigation strategies and guidelines can then be developed to support desired product reliability.

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