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White Paper

Failure Mechanisms in High Voltage Printed Circuit Boards

By Craig Hillman, PhD, Robert Esser, PhD, and Jim McLeish

5110 Roanoke Place, Suite 101 College Park, Maryland 20740
Phone (301) 474-0607 Fax (240) 757-0053
www.DfRSolutions.com

1. Description of Failure Mechanisms

There are two classes of failure mechanisms that become important under conditions of high voltage and reduced conductor spacing: metal migration and electric breakdown.

1.1 Metal Migration

The minimum electrical conductor spacing defined in IPC-2221 is not based upon metal migration failure mechanisms. However, research has shown that metal migration can be a critical failure mechanism in high-voltage, high-density printed circuit boards. For this reason the issues effecting metal migration should be addressed.

Metal migration includes electrochemical migration [1,2], tarnish creepage [3], and tin whiskering [4]. Electrochemical migration is the loss of insulation resistance between two conductors (trace, pad, plated-through-hole) due to the growth of conductive metal filaments. The growth of these filaments is dependent upon the presence of an electric field, to drive the metallic ions, and atmospheric moisture, which serves as the transport medium.

Tarnish creepage is migration of corrosion product between two conductors and tin whiskering is the migration of tin filaments due to the application of mechanical stress. Both mechanisms can cause failures between closely spaced conductors, but unlike electromigration, are independent of the strength of the applied electric field and therefore not limited to high voltage applications.

1.2 Electric Breakdown

There are four possible failure mechanisms related the initiation of an electrical arc across or through dielectric material: dust-buildup, air breakdown, surface flashover, and dielectric failure. The path of arc formation primarily differentiates the four failure mechanisms.

Dust-buildup occurs when dust attracted by a DC electric field spans adjacent conductors. The absorption of moisture by the dust over time can result in current leakage and eventually produce a short circuit.

Air breakdown is the condition in which an electrical arc spans the air gap between two conductors. The factors necessary for air breakdown are formulated from Paschen's Law, which states that the arcing potential of a gas is a function of the atmospheric pressure and electrode distance. A schematic of electric breakdown of air at STP is displayed in Figure 1.

Surface flashover is electric breakdown along the surface of the printed circuit board between two conductors. Flashover initiates at the junction of the conductor (trace, pad, plated-through-hole), insulator (laminate material), and gas (air or vacuum) and may or may not cause permanent damage. When the conduction path across the surface is established, called "tracking", degradation of the material can occur, reducing the lifetime of the insulative properties of the printed circuit board.

Dielectric failure is electric breakdown within a solid insulator between two conductors and is often concurrent with visible puncture and decomposition of the insulation material. All materials break down at some level of applied voltage gradient. This level can vary based upon material (thickness and quality of sample) and environmental (temperature and humidity) factors.

2. Failure Probabilities

The absence of atmospheric moisture in the operating environment of the ISS will effectively eliminate those failure mechanisms dependent upon humidity, which include electromigration, tarnish creepage, and dust-buildup. Tin whiskering will only be a factor with the application of tin coatings to the surface of the printed circuit board.

In regards to air breakdown, the IPC standards for external conductors, displayed in Table 1, incorporate a significant safety factor (min. air breakdown strength of 5,000 V/mm vs. max. IPC standard of 770 V/mm). However, the Paschen curve in Figure 1 assumes spherical electrodes suspended in space. This is not the case with etched traces on printed boards and significant increases in the electric field can occur along the square edges and corners of the metallization. Discontinuities in the board coatings, such as pinholes in the soldermask, can also result in result in a decrease in the air breakdown strength.

However, during the operation of printed circuit boards, the values of air breakdown strength are often not used to when determining external conductor spacing. This is because electrical shorts between external conductors generally occur by surface flashover, at field stresses below the air breakdown strength. The actual value of the electric field necessary for surface flashover can be highly variable and is dependent upon the smoothness and cleanliness of the board surface as well as other testing parameters. Published literature reports values ranging from 2 to 8 kV/mm.

Concerns over surface flashover can be addressed by completely encapsulating the exposed electrical conductors (breakdown of polyurethane > 10 kV/mm [5, 6]). However, for assurances of long operating lifetime, care must be taken when applying the coating. The coating should be free of large voids and should be applied so that the height of the conformal coating is equal with height of the highest electrical conductors (which essentially fills the "void" between the conductors).

Under an applied AC voltage, the conformal coating and air will behave as two different capacitors. In the case of polyurethane, the conformal coat will have a dielectric constant five times larger than air. If we assume all other parameters being equal, modeling the conformal coating and air (either as a void or space between conductors) in series results in a voltage concentration across the air gap five times larger than the potential across the polyurethane coating. This can result in partial discharging at average field stresses below surface flashover and eventual failure due to electric breakdown.

Dielectric failure of the polyimide laminate will be dependent upon the direction of the electrical arc. Dielectric strength and dielectric breakdown are the values of electrical field stress that result in dielectric failure. Dielectric strength is measured perpendicular to the lamination direction and is very high (see Table 1). As a result, *interlayer* breakdown is unlikely to be the dominant failure mechanism since it provides a safety factor of 15 above the maximum IPC standard for internal conductors (30,000 V/mm vs. 2,000 V/mm). Dielectric breakdown is measured parallel to the lamination direction. Because the fiber/polyimide interface provides a convenient path for electrical discharge, the electrical field stress necessary for *intralayer* breakdown is much lower than for *interlayer* breakdown.

The composite structure therefore provides a lower margin of safety with regards to *intralayer* dielectric breakdown (2360 V/mm vs. max. IPC standard 2000 V/mm). Since the vacuum atmosphere of the operating environment and application of conformal coating should reduce the likehood of all other failure mechanisms, the primary concern will be dielectric failure lateral to the lamination direction. This assumes no defects, such as large voids, are present

3. Environmental Factors

In determining the robustness of a circuit design that violates IPC standards for intralayer dielectric failure, one must consider the operating and environmental parameters that will affect electric breakdown, such as temperature, humidity, sample thickness, electrode configuration, nature of the electrical stimulus, and desired operating lifetime.

3.1 Temperature

Below room temperature, the dielectric breakdown behavior of polyimide is relatively constant. Above room temperature, the electric field stress necessary for breakdown begins to decrease [7]. For monolithic polyimide, the dielectric strength at 100°C is approximately 80% of the room temperature value; at 200°C, the dielectric strength is approximately 60% of room temperature value. Polyimide laminates might be even more sensitive to temperature because of their complex structure and dependence on the integrity of the glass/polyimide interface.

3.2 Humidity

Because of the vacuum environment during operation, the effect of humidity on dielectric breakdown is not relevant. However, atmospheric moisture can reduce dielectric strength and therefore could lead to accelerated failures if the humidity of the testing environment is different than the humidity of the operational environment.

3.3 Frequency and Duration of Voltage Transients

Dielectric strength is a function of the operating frequency and the duration of the voltage transient. Dielectric strength is reduced with increasing frequency. Since dielectric breakdown voltage and dielectric strength testing is performed at 60 Hz [8], 15-25% derating should be performed to account for frequency effects. This derating has been found to be valid up to 50 kHz [9].

When voltages are applied for short durations, on the order of 10 nS, the dielectric strength of a solid material increases rapidly and approaches the intrinsic breakdown strength of the material. Measurement of breakdown strength is often performed using the step-by-step method, where voltage is applied for 20 to 300 seconds. Schematics of the effect of duration on dielectric strength can be seen in Figures 2 and 3. Observation of breakdown behavior displayed in Figures 2 and 3 shows that the dielectric strength measured using standard testing procedures can provide a conservative limit for breakdown strength in comparison to operating conditions involving transient voltage peaks.

3.4 Sample Thickness

The dielectric strength of a material increases at less than a linear rate for increasing thickness. Therefore, the dielectric strength is higher for a thin sample than for a thick sample. This is important when extrapolating the results of standard test methods to actual operating environments. The intralayer electric breakdown measured for polyimide laminates is performed by placing two electrodes one inch apart. This will result in a conservative value for breakdown strength when compared to electrical conductors placed closer together, such as 0.5 mm apart.

3.5 Electrode Configuration

To ensure high reliability under high voltage conditions, the maximum and average electrical field stress in the printed circuit board should be estimated. The maximum stress is dependent upon the electrode/conductor configuration and can be calculated using utilization curves. An example of a utilization curve is displayed in Figure 5.

The maximum field stress, Es, is equal to the inverse of the per unit voltage derating factor, also known as the utilization factor. As an example, a cylinder -to-cylinder electrode configuration with a distance-to-radius (d/r) ratio of 6 will have a utilization factor of 0.2 and a maximum electrical stress 5 times the average electrical stress.

One published article recommends average voltage stresses no greater than 2 kV/mm because electrode configuration can result in maximum voltage stresses as high as 10 kV/mm. These field gradients can exceed the short-term lifetime of the substrate or conformal coating material and are not recommended for long-life operation.

3.6 Operating Lifetime

The dielectric breakdown values given in the literature are short-time values. Depending upon the magnitude, distribution, and frequency of the voltage transients, it maybe necessary to derate the dielectric breakdown and strength values for long-term operating reliability. This occurs because all laminates, such as polyimides, have a population of voids in their interior. These microscopic voids will tend to suffer from partial discharges in high voltage environments. Above a given voltage, these partial discharges degrade the surrounding material, making the laminate susceptible to dielectric failure. This degradation mechanism can take from a couple of minutes to several years to reach electric breakdown. As one guide, Dunbar and Tjelle [5] recommend reducing the useful dielectric strength to 65% of short-term values to ensure 10,000 hours of operation.

4. Discussion/Conclusion

The absence of humidity and the presence of a vacuum in the operating environment will provide a degree of safety above that provided in the minimum spacing requirements displayed in IPC-2221. Voltage transients of similar duration (10 nS) to the voltage spikes seen in power diode (see CALCE Report "Lifetime Assessment of Wedge Bonds in a High Current Diode") will also provide an additional safety factor above minimum spacings recommended in IPC-2221. Operating temperatures above room temperature and processing defects will lead to a reduction in the electrical field stress necessary to induce dielectric failure.

A thorough physics-of-failure (PoF) approach is recommended to determine the integrity of a printed circuit board that violates IPC-2221. PoF is based upon documenting the assembly architecture, operational environment, and material properties, determining the relevant failure mechanisms, accurate measurement of the environmental loads (average and maximum electrical field stress), and the use of an acceleration factor to take into consideration degradation during operational lifetime. This assessment will provide a more accurate understanding of the reliability of the polyimide printed circuit board than a critical analysis of the spacing requirements defined in IPC-2221.

The electrical conductor spacing requirements defined in Table 6-1 in IPC-2221 are based upon research that was performed by Dr. Charles Jennings of Sandia National Laboratories. The results of Dr. Jennings research was published in IPC-TP-117, *Electrical Properties of Printed Wiring Boards*, in September 1976. IPC-TP-117 focused on dielectric breakdown, current carrying capacity and insulation resistance for 2-sided bare, coated, and encapsulated (epoxy and urethane) FR-5 (glass reinforced Fire-Resistant epoxy) printed wiring boards. Breakdown testing was conducted in air (767 Torr) and at low pressures (500 Torr).

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